# HY2550 Series
# Datasheet

## Protection IC for 3/4/5-cell Li+ Battery

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## 1. General Description

HY2550 Series is a protection IC for safety of 3-cell /4-cell/5-cell lithium ion and lithium polymer rechargeable batteries. The protection IC integrates accurate voltage detection and protection delay circuitry for best battery protection purpose.

## 2. Features

The features that whole series of HY2550 comprised are as follows:

(1) High-accuracy voltage detection for each cell:

- Overcharge detection voltage n (n = 1 to 5) 3.9V to 4.6V (50mV step) Accuracy: ±25mV
- Overcharge release voltage n (n = 1 to 5) 3.8V to 4.6V[*1] Accuracy: ±50mV
- Overdischarge detection voltage n (n = 1 to 5) 2.0V to 3.0V (50mV step) Accuracy: ±80mV
- Overdischarge release voltage n (n = 1 to 5) 2.0V to 3.4V[*2] (100mV step) Accuracy: ±100mV

(2) Charge overcurrent protection:

- Charge overcurrent detection voltage -0.05V to -0.35V Accuracy: ±25mV

(3) Three-level discharge overcurrent protection:

- Overcurrent detection voltage 1 0.05V to 0.35V Accuracy: ±25mV
- Overcurrent detection voltage 2 0.10V to 0.50V (50mV step) Accuracy: ±50mV
- Overcurrent detection voltage 3 VC1 – 0.1V to VC1-1.2V (50mV step) Accuracy: ±100mV

(4) Delay time:

Delay times are set by external capacitors respectively at CCT pin and CDT pin for overcharge detection, /charge overcurrent detection and overdischarge detection/discharge overcurrent detection voltage 1. Delay times are set internally for discharge overcurrent detection voltage 2 (1ms) and discharge overcurrent detection 3 (300μs).

(5) Cell number selection:

SEL pin is used to select either 3 battery cells in use or 4 battery cells in use.

SEL5 pin is used to select 5 battery cells in use when SEL pin is also set to “1”

(6) Charge/discharge operation can be controlled via the CTL pin.

(7) 0V Battery Charge inhibition.

(8) High voltage withstand range: Absolute maximum rated level: 28V

(9) Wide operating voltage range: Maximum operation voltage level: 26V

(10) Wide operating temperature range: -40℃ to +85℃

(11) Low current consumption

- Operation mode — 12μA typ., 30μA max. ($V_{Cn}$ = 3.5V)
- Power-down mode — 1.2μA typ., 2.0μA max. ($V_{Cn}$ = 2.0V)

(12) Small package: 16-pin TSSOP

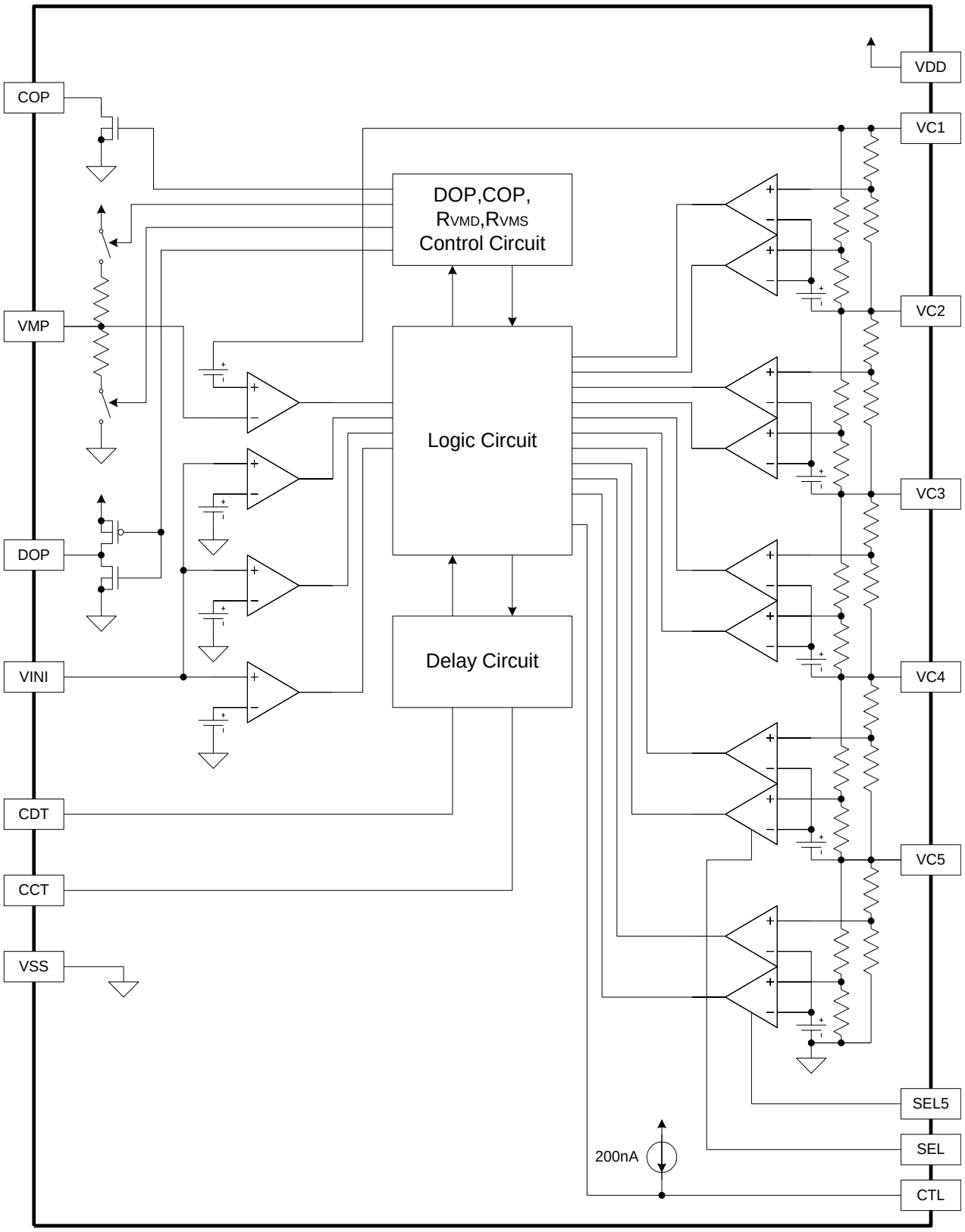
(13) Halogen free green product

Note: *1. Overcharge hysteresis voltage can be selected from 0 to 0.4V in 25mV steps.
(Overcharge hysteresis voltage = Overcharge detection voltage - Overcharge release voltage)
*2. Overdischarge hysteresis voltage can be selected from 0 to 0.7V in 50mV steps.
(Overdischarge hysteresis voltage = Overdischarge release voltage - Overdischarge detection voltage)

## 3. Applications

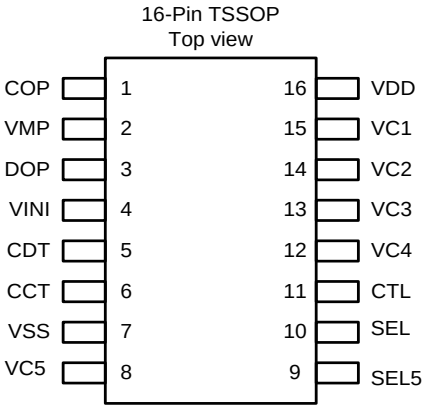
- 3-cell / 4-cell/ 5-cell lithium ion rechargeable battery pack
- 3-cell / 4-cell/ 5-cell lithium polymer rechargeable battery pack

## 4. Block Diagram



## 5. Pin Definition

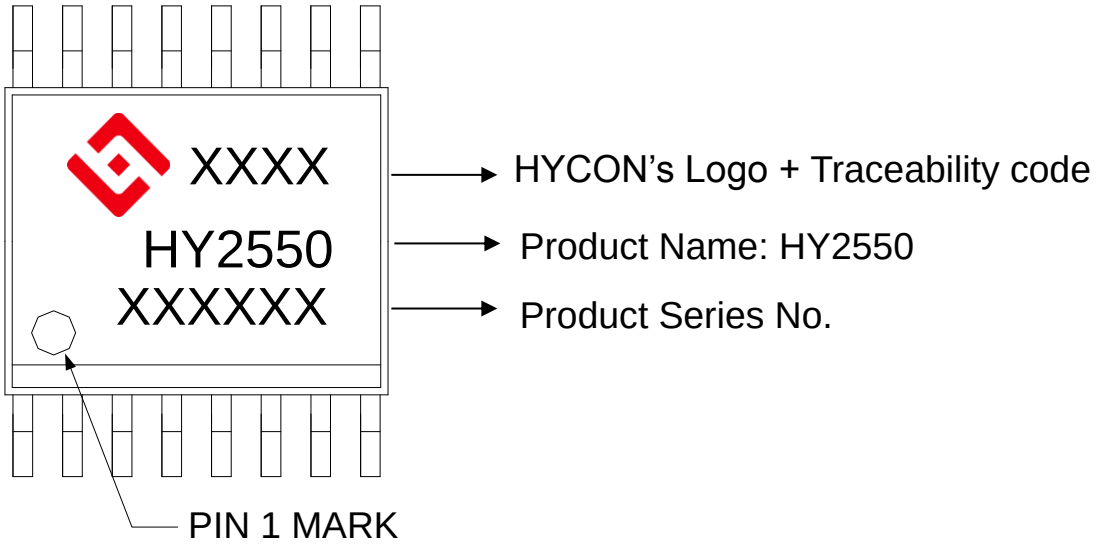
### 5.1 TSSOP-16 Diagram




### 5.2 Pinout I/O Description

| Pin | Symbol | Description |
|---|---|---|
| 1 | COP | FET gate connection pin for charge control (Nch open drain output) |
| 2 | VMP | Pin for voltage detection between VC1 and VMP (Pin for discharge overcurrent detection 3) |
| 3 | DOP | FET gate connection pin for discharge control FET (CMOS output) |
| 4 | VINI | Pin for voltage detection between VSS and VINI (Pin for discharge overcurrent detection 1,2 and charge overcurrent detection) |
| 5 | CDT | Capacitor connection pin for overdischarge delay and discharge overcurrent detection 1 delay. |
| 6 | CCT | Capacitor connection pin for overcharge delay and charge overcurrent detection delay. |
| 7 | VSS | Input pin for negative power supply,<br>Connection pin for battery 5's negative voltage |
| 8 | VC5 | Connection pin for battery 4's negative voltage,<br>Connection pin for battery 5's positive voltage |
| 9 | SEL5 | Pin for selecting 5-series<br>VSS level: 3-series and 4-series cell, VDD level : 5-series cell |
| 10 | SEL | Pin for switching 3-series or 4-series cell<br>VSS level: 3-series cell, VDD level : 4-series cell and 5-series cell |
| 11 | CTL | Control of charge FET and discharge FET |
| 12 | VC4 | Connection pin for battery 3's negative voltage,<br>Connection pin for battery 4's positive voltage |
| 13 | VC3 | Connection pin for battery 2's negative voltage,<br>Connection pin for battery 3's positive voltage |
| 14 | VC2 | Connection pin for battery 1's negative voltage,<br>Connection pin for battery 2's positive voltage |
| 15 | VC1 | Connection pin for battery 1's positive voltage |
| 16 | VDD | Input pin for positive power supply,<br>Connection pin for battery 1's positive voltage |

5.3 Package marking information



## 6. Electrical Characteristics

### 6.1 Absolute Maximum Rating

(VSS = 0V, Ta=25 ℃ unless indicated otherwise)

| Item | Symbol | Specification | Unit |
|---|---|---|---|
| Input voltage between VDD and VSS | $V_{DS}$ | VSS-0.3 to VSS+28 | V |
| VC1 pin input voltage | VC1 | VC2-0.3 to VC2+5.5 | V |
| VC2 pin input voltage | VC2 | VC3-0.3 to VC3+5.5 | V |
| VC3 pin input voltage | VC3 | VC4-0.3 to VC4+5.5 | V |
| VC4 pin input voltage | VC4 | VC5-0.3 to VC5+5.5 | V |
| VC5 pin input voltage | VC5 | VSS-0.3 to VSS+5.5 | V |
| VINI pin input voltage | VINI | VSS-0.3 to VSS+5.5 | V |
| CTL pin input voltage | CTL | VSS-0.3 to VDD+0.3 | V |
| SEL pin input voltage | SEL | VSS-0.3 to VDD+0.3 | V |
| SEL5 pin input voltage | SEL5 | VSS-0.3 to VDD+0.3 | V |
| VMP Input pin voltage | VMP | VSS-0.3 to VSS+28 | V |
| COP pin output voltage | COP | VSS-0.3 to VSS+28 | V |
| DOP pin output voltage | DOP | VSS-0.3 to VDD+0.3 | V |
| Operating Temperature Range | TOP | -40 to +85 | ℃ |
| Storage Temperature Range | TST | -40 to +125 | ℃ |
| Tolerant Power Consumption | PD | 400 | mW |

### 6.2 Electrical Parameters

(VSS = 0V, Ta=25 ℃ unless indicated otherwise)

| Item | Symbol | Condition | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| **Detection Voltage** | | | | | | |
| Overcharge detection voltage n (n = 1 to 5) | $V_{CUn}$ | $V_{CUn}$ = 3.9V ~ 4.6V adjustable | $V_{CUn}$ – 0.025 | $V_{CUn}$ | $V_{CUn}$ + 0.025 | V |
| Overcharge release voltage n (n = 1 to 5) | $V_{CRn}$ | VCRn = 3.8V ~ 4.6V adjustable | $V_{CRn}$ – 0.050 | $V_{CRn}$ | $V_{CRn}$ + 0.050 | V |
| Overdischarge detection voltage n (n = 1 to 5) | $V_{DLn}$ | $V_{DLn}$ = 2.0V ~ 3.0V adjustable | $V_{DLn}$ – 0.080 | $V_{DLn}$ | $V_{DLn}$ + 0.080 | V |
| Overdischarge release voltage n (n = 1 to 5) | $V_{DRn}$ | $V_{DRn}$ = 2.0V ~ 3.4V adjustable | $V_{DRn}$ – 0.100 | $V_{DRn}$ | $V_{DRn}$ + 0.100 | V |
| Overcurrent detection voltage 1 | $V_{IOV1}$ | $V_{IOV1}$ = 0.05V ~ 0.35V adjustable | $V_{IOV1}$ – 0.025 | $V_{IOV1}$ | $V_{IOV1}$ + 0.025 | V |
| Overcurrent detection voltage 2 | $V_{IOV2}$ | $V_{IOV2}$ = 0.1V ~ 0.5V adjustable | $V_{IOV2}$ – 0.05 | $V_{IOV2}$ | $V_{IOV2}$ + 0.05 | V |
| Overcurrent detection voltage 3 | $V_{IOV3}$ | $V_{IOV3}$ = VC1-0.1V ~ VC1-1.2V adjustable | VC1-1.5 | VC1-1.2 | VC1-0.9 | V |
| Charge overcurrent detection voltage | $V_{CIP}$ | $V_{CIP}$ = -0.05V ~ -0.35V adjustable | $V_{CIP}$ – 0.025 | $V_{CIP}$ | $V_{CIP}$ + 0.025 | V |
| Temperature coefficient for overcharge detection voltage | $TC_{OE1}$ | Ta = 0℃~ 50℃ *1 | -1 | 0 | 1 | mV/℃ |
| Temperature coefficient for | $T_{COE2}$ | Ta = 0℃~ 50℃ *1 | -0.5 | 0 | 0.5 | mV/℃ |

| Item | Symbol | Condition | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| overcurrent detection voltage 1 | | | | | | |
| **Delay Time** | | | | | | |
| Overcharge detection delay time | $T_{OC}$ | CCT pin capacitance=0.1μF | 0.5 | 1 | 1.5 | s |
| Overdischarge detection delay time | $T_{OD}$ | CDT pin capacitance=0.1μF | 50 | 100 | 150 | ms |
| Overcurrent detection delay time 1 | $T_{IOV1}$ | CDT pin capacitance=0.1μF | 5 | 10 | 15 | ms |
| Overcurrent detection delay time 2 | $T_{IOV2}$ | | 0.4 | 1 | 1.6 | ms |
| Overcurrent detection delay time 3 | $T_{IOV3}$ | FET gate capacitance = 2000pF. | 100 | 300 | 600 | μs |
| Charge overcurrent detection delay time | $T_{CIP}$ | CCT pin capacitance=0.1μF | 5 | 10 | 15 | ms |
| **0V Battery Charge Function** | | | | | | |
| 0 V battery charge starting charger voltage | $V_{0CHA}$ | 0 V battery charging available | 3.0 | | | V |
| **Internal Resistance** | | | | | | |
| Resistance between VMP and VDD | $R_{VMD}$ | | 0.5 | 1 | 1.5 | MΩ |
| Resistance between VMP and VSS | $R_{VMS}$ | | 0.45 | 0.9 | 1.8 | MΩ |
| **Input Voltage** | | | | | | |
| Operating voltage between VDD and VSS | $V_{DSOP}$ | | 3 | - | 26 | V |
| CTL input voltage “H” | $V_{CTLH}$ | | 4.0 | - | - | V |
| CTL input voltage “L” | $V_{CTLL}$ | | - | - | 2.0 | V |
| SEL input voltage “H” | $V_{SELH}$ | | 4.0 | - | - | V |
| SEL input voltage “L” | $V_{SELL}$ | | - | - | 2.0 | V |
| **Input Current** | | | | | | |
| Current consumption during operation | $I_{OPE}$ | V1=V2=V3=V4=V5=3.5V | | 12 | 30 | μA |
| Current consumption during power-down | $I_{PDN}$ | V1=V2=V3=V4=V5=2.0V | | 1.2 | 2.0 | μA |
| VC1 pin current | $I_{VC1}$ | V1=V2=V3=V4=V5=3.5V | | 3.6 | 6.0 | μA |
| VC2 pin current | $I_{VC2}$ | V1=V2=V3=V4=V5=3.5V | -0.3 | 0 | 0.3 | μA |
| VC3 pin current | $I_{VC3}$ | V1=V2=V3=V4=V5=3.5V | -0.3 | 0 | 0.3 | μA |

| Item | Symbol | Condition | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| VC4 pin current | $I_{VC4}$ | V1=V2=V3=V4=V5=3.5V | -0.3 | 0 | 0.3 | μA |
| CTL pin current “H” | $I_{CTLH}$ | V1=V2=V3=V4=V5=3.5V, CTL=VDD | | | 0.1 | μA |
| CTL pin current “L” | $I_{CTLL}$ | V1=V2=V3=V4=V5=3.5V, CTL=VSS | -0.4 | -0.2 | | μA |
| SEL pin current “H” | $I_{SELH}$ | V1=V2=V3=V4=V5=3.5V, SEL=VDD | | | 0.1 | μA |
| SEL pin current “L” | $I_{SELL}$ | V1=V2=V3=V4=V5=3.5V, SEL=VSS | -0.1 | | | μA |
| SEL5 pin current “H” | $I_{SEL5H}$ | V1=V2=V3=V4=V5=3.5V, SEL5=VDD | | | 0.1 | μA |
| SEL5 pin current “L” | $I_{SEL5L}$ | V1=V2=V3=V4=V5=3.5V, SEL5=VSS | -0.1 | | | μA |
| **Output Current** | | | | | | |
| COP pin leakage current | $I_{COH}$ | $V_{COP}$=26V | | | 0.1 | μA |
| COP pin sink current | $I_{COL}$ | $V_{COP}$=VSS+0.5V | 5 | | | μA |
| DOP pin source current | $I_{DOH}$ | $V_{DOP}$=VDD-0.5V | 5 | | | μA |
| DOP pin sink current | $I_{DOL}$ | $V_{DOP}$=VSS+0.5V | 5 | | | μA |

**Description:**

*1. The parameters within this temperature range are design guarantee values instead of screened values from high, low temperature measurement.

## 7. Test Circuit

7.1 The current at the VSS pin when V1= V2= V3= V4= V5=3.5 V and $V_{VMP}$= VDD is the a current consumption during operation ($I_{OPE}$)

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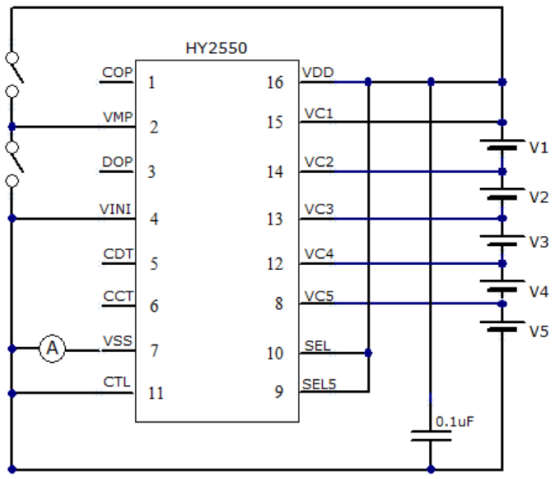
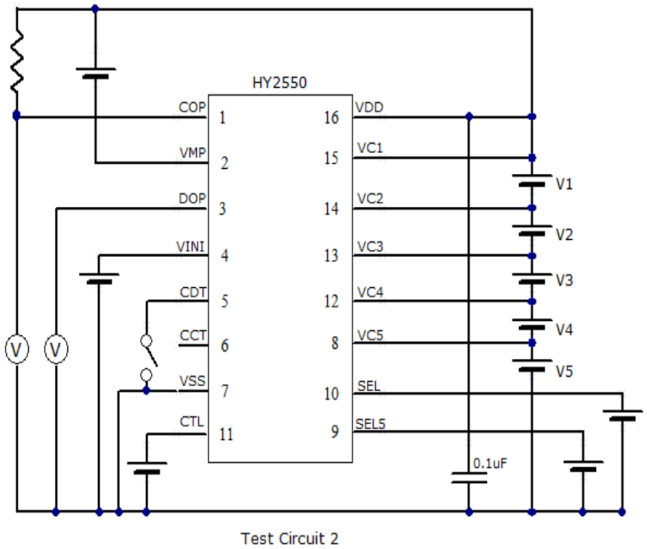
7.2 The current at the VSS pin when V1 = V2 = V3 = V4 = V5= 2.0 V, and $V_{VMP}$ = VSS is the current consumption during power-down ($I_{PDN}$)。




Test Circuit 1

7.3 **Overcharge Detection Voltage** ($V_{CUn}$)、**Overcharge Release Voltage** ($V_{CRn}$)、**Overdischarge Detection Voltage** ($V_{DLn}$)、**Overdischarge Release Voltage**($V_{DRn}$)、**Overcurrent Detection Voltage** 1 ($V_{IOV1}$)、**Overcurrent Detection Voltage**2($V_{IOV2}$)、**Overcurrent Detection Voltage**3($V_{IOV3}$)、**CTL Input Voltage** “H”, **CTL Input Voltage** “L”, **SEL Input Voltage** “H”, **SEL Input Voltage** “L” (Test Circuit 2).

Confirm that the COP pin and DOP pin are low(VDD x0.1 V or lower) when VVMP= VSEL=VDD, VINI=VCTL= VSS, the CCT pin is open, the CDT pin is open, and V1=V2= V3 = V4 = V5=3.5 V.




Test Circuit 2

7.3.1 **Overcharge Detection Voltage** ($V_{CUn}$)、**Overcharge Release Voltage** ($V_{CRn}$)

The overcharge detection voltage (VCUn) is the voltage of V1 when the voltage of the COP

pin is “H” (VDD x 0.9 V or more) after the V1 voltage has been gradually increased starting at the initial status. The overcharge release voltage (VCRn) is the voltage of V1 when the voltage at the COP pin is “L” after the V1 voltage has been gradually decreased.

7.3.2 **Overdischarge Detection Voltage** ($V_{DLn}$), **Overdischarge Release Voltage** ($V_{DRn}$)

The overdischarge detection voltage (VDLn) is the voltage of V1 when the voltage of the DOP pin is after the V1 voltage has been gradually decreased starting at the initial status. The overdischarge。release voltage (VDR1) is the voltage of V1 when the voltage at the DOP pin is “L” after the V1 voltage has been gradually increased。

When the voltage of Vn (n=2 to 5) is changed, the overcharge detection voltage ($V_{CUn}$), overcharge release voltage ($V_{CRn}$), overdischarge detection voltage ($V_{DLn}$), and overdischarge release voltage ($V_{DRn}$) can be determined in the same way as when n =1.

7.3.3 **Overcurrent Detection Voltage** 1 ($V_{IOV1}$)

Overcurrent detection voltage 1 ($V_{IOV1}$) is the voltage of the VINI pin when the voltage of the DOP pin1 ($V_{IOV1}$) is “H” after the VINI pin voltage has been gradually increased starting at the initial status.

7.3.4 **Overcurrent Detection Voltage**2 ($V_{IOV2}$)

Overcurrent detection voltage 2 ($V_{IOV2}$) is the voltage of the VINI pin when the voltage of the DOP pin is “H” after the voltage of the CDT pin was set to $V_{SS}$ following the initial status and the voltage of the VINI pin has been gradually decreased.

7.3.5 **Overcurrent Detection Voltage**3 ($V_{IOV3}$)

Overcurrent detection voltage 3 (VIOV3) is the voltage difference between VVC1 and VVMP (VVC1 -VVMP) when the voltage of the DOP pin is “H” after the VMP voltage has been gradually decreased starting at the initial status.

7.3.6 **Overcharge Current Detection Voltage** ($V_{CIP}$)

Overcharge current detection voltage 1 ($V_{CIP}$) is the voltage of the VINI pin when the voltage of the COP pin1 ($V_{CIP}$) is “H” after the VINI pin voltage has been gradually increased starting at the initial status.

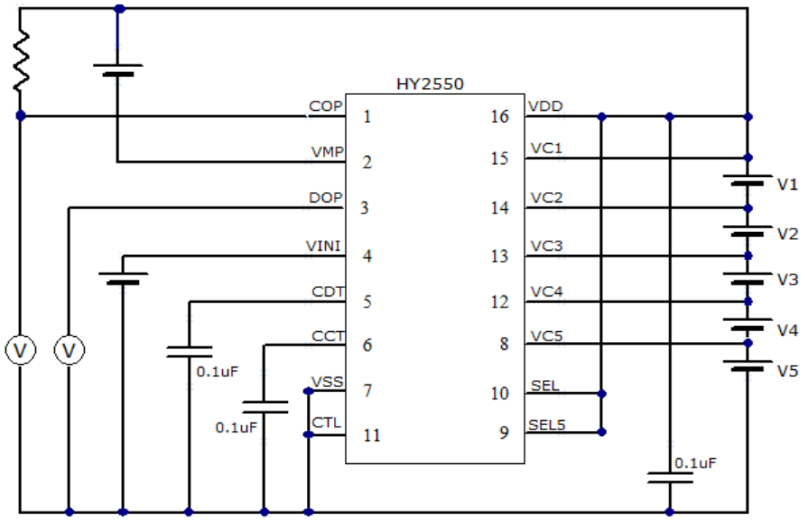
7.4 **CTL Input Voltage** “H” ($V_{CTLH}$)、**CTL Input Voltage** “L” ($V_{CTLL}$)

The CTL input voltage “H” ($V_{CTLH}$) is the voltage of CTL when the voltages at the COP and DOP pins are “H” after the CTL voltage has been gradually increased starting at the initial status. The CTL input voltage “L” ($V_{CTL}$) is the voltage of CTL when the voltages at the COP and DOP pins are “L” after the CTL voltage has been gradually decreased.

7.5 **SEL Input Voltage** "H" ($V_{SELH}$) 、**SEL Input Voltage** "L" ($V_{SELL}$)

Apply 0 V to V4 in the initial status and confirm that the DOP pin is "H". The SEL input voltage "L"(VSELL) is the voltage of the SEL pin when the voltage at the DOP pin is "L" after the SEL voltage has been gradually decreased. The SEL input voltage "H" (VSELH) is the voltage of the SEL pin when the voltage of the DOP pin is "H" after the SEL voltage has been gradually increased.

7.6 **Overcharge Detection Delay Time, Overdischarge Detection Delay Time, Overcurrent Detection Delay Time** 1**, Overcurrent Detection Delay Time** 2, **Overcurrent Detection Delay Time** 3 (**Test Circuit** 3)




Test Circuit 3

Confirm that the COP pin and DOP pin are "L" when VVMP =VDD, VINI =VSS, and V1=V2=V3 =V4= V5=3.5 V (this status is referred to as the initial status.

7.6.1 **Overcharge Detection Delay Time** ($t_{OC}$)

The overcharge detection delay time (tOC) is the time it takes for the voltage of the COP pin to change from "L" to "H" after the voltage of V1 is instantaneously changed to 4.5 V from the initial status.

7.6.2 **Overdischarge Detection Delay Time** ($t_{OD}$)

The overdischarge detection delay time (tOD) is the time it takes for the voltage of the DOP pin to change from "L" to "H" after the voltage of V1 is instantaneously changed to 1.5 V from the initial status.

7.6.3 **Overcurrent Detection Delay Time**1 ($t_{IOV1}$)

Overcurrent detection delay time 1 (tIOV1) is the time it takes for the voltage of the DOP pin to change from "L" to "H" after the voltage of the VINI pin is instantaneously changed to 0.4 V from the initial status.

7.6.4 **Overcurrent Detection Delay Time** 2 ($t_{IOV2}$)

Overcurrent detection delay time 2 ($t_{IOV2}$) is the time it takes for the voltage of the DOP pin to change from “L” to “H” after the voltage of the VINI pin is instantaneously changed to VIOV2 max. +0.2 V from the initial status.

7.6.5 **Overcurrent Detection Delay Time** 3 ($t_{IOV3}$)

Overcurrent detection delay time 3 ($t_{IOV3}$) is the time it takes for the voltage of the DOP pin to change from “L” to “H” after the voltage of the VMP pin is instantaneously changed to VIOV3 min. -0.2 V from the initial status.

## 8. Description of Operation

### 8.1 Normal Status

When the voltage of each of the batteries is in the range from $V_{DLn}$ to $V_{CUn}$ and the discharge current is lower than the specified value (the VINI pin voltage is higher than $V_{CIP}$, the VINI pin voltage is lower than $V_{IOV1}$ and $V_{IOV2}$, and the VMP pin voltage is higher than $V_{IOV3}$), the charging and discharging FETs are turned on.

### 8.2 Overcharge Status

When the voltage of one of the batteries becomes higher than $V_{CUn}$ and the state continues for $T_{OC}$ or longer, the COP pin becomes high impedance. The COP pin is pulled up to the EB+ pin voltage by an external resistor, and the charging FET is turned off to stop charging. This is called the overcharge status. The overcharge status is released when one of the following two conditions holds.

(1) The voltage of each of the batteries becomes $V_{CRn}$ or lower.

(2) The voltage of each of the batteries is $V_{CUn}$ or lower, and the VMP pin voltage is 39 / 40 × VDD or lower (a load is connected and discharging is started via the body diode of the charging FET).

### **8.3** Overdischarge Status

When the voltage of one of the batteries becomes lower than $V_{DLn}$ and the state continues for $T_{OD}$ or longer, the DOP pin voltage becomes VDD level, and the discharging FET is turned off to stop discharging. This is called the overdischarge status.

### 8.4 Power-down Function

When the overdischarge status is reached, the VMP pin is pulled down to the VSS level by the internal $R_{VMS}$ resistor of the IC. When the VMP pin voltage is 2.5V or lower, the power-down function starts to operate and almost every circuit in the HY2550 Series stops working. The conditions of each output pin are as follows.

(1) COP pin : High-Z

(2) DOP pin : VDD

The power-down function is released when the following condition holds.

(1) The VMP pin voltage is 2.5V or higher.

The overdischarge status is released when the following two conditions hold.

(1) In case the VMP pin voltage is 2.5V or higher and the VMP pin voltage is lower than VDD, the overdischarge status is released when the voltage of each of the batteries is $V_{DRn}$ or higher.

(2) In case a charger is connected, the overdischarge hysteresis is released. And the overdischarge status is released when the voltage of each of the batteries is $V_{DLn}$ or higher.

### 8.5 Discharge Overcurrent Status

The HY2550 Series has three overcurrent detection levels ($V_{IOV1}$, $V_{IOV2}$, and $V_{IOV3}$) and three overcurrent detection delay times ($T_{IOV1}$, $T_{IOV2}$, and $T_{IOV3}$) corresponding to each overcurrent detection level. When the discharging current becomes higher than the specified value (the voltage between VINI and VSS is greater than $V_{IOV1}$) and the state continues for $T_{IOV1}$ or longer, the HY2550 Series enters the overcurrent status, in which the DOP pin voltage becomes VDD level to turn off the discharging FET to stop discharging, the COP pin becomes high impedance and is pulled up to the EB+ pin voltage to turn off the charging FET to stop charging, and the VMP pin is pulled up to the VDD voltage by the internal resistor ($R_{VMD}$). Operation of overcurrent detection level 2 ($V_{IOV2}$) and overcurrent detection delay time 2 ($T_{IOV2}$) is the same as for $V_{IOV1}$ and $T_{IOV1}$.

In the overcurrent status, the VMP pin is pulled up to the VDD level by the internal resistor in the IC ($R_{VMD}$ resistor). The overcurrent status is released when the following condition holds.

(1) The VMP pin voltage is $V_{IOV3}$ or higher because a charger is connected or the load (300 KΩ or more) is released.

### 8.6 Charge Overcurrent Status

The HY2550 Series has charge overcurrent detection levels ($V_{CIP}$) and charge overcurrent detection delay times ($T_{CIP}$). When the charging current becomes higher than the specified value (the voltage between VINI and VSS is lower than $V_{CIP}$) and the state continues for $T_{CIP}$ or longer, the HY2550 Series enters the charge overcurrent status, the COP pin becomes high impedance. The COP pin is pulled up to the EB+ pin voltage by an external resistor, and the charging FET is turned off to stop charging.

The charge overcurrent status is released when the following condition holds.

(1) The VMP pin voltage is 39 / 40 × VDD or lower (disconnected the charger and a load is connected, discharging is started via the body diode of the charging FET).

### 8.7 0V Battery Charge Function

Regarding the charging of a self-discharged battery (0 V battery), the HY2550 Series has two functions from which one should be selected.

(1) 0 V battery charging is allowed (0 V battery charging is available.)
When the charger voltage is higher than $V_{0CHA}$, the 0 V battery can be charged.

(2) 0 V battery charging is prohibited (0 V battery charging is unavailable.)
When the battery voltage is $V_{0INH}$ or lower, the 0 V battery cannot be charged.

**Caution: When the VDD pin voltage is lower than the minimum value of $V_{DSOP}$, the operation of the HY2550 Series is not guaranteed.**

### 8.8 Delay Time Setting

The overcharge detection delay time ($T_{OC}$) and charge overcurrent delay time ($T_{CIP}$) are determined by

the external capacitor connected to the CCT pin. The overdischarge detection delay time ($T_{OD}$) and overcurrent detection delay time 1 ($T_{IOV1}$) are determined by the external capacitor connected to the CDT pin. Overcurrent detection delay times 2 and 3 ($T_{IOV2}$, $T_{IOV3}$) are fixed internally.

| | min. | typ. | max. | |
|---|---|---|---|---|
| $T_{OC}$ [s]= | (5.00, | 10.0, | 15.0) x | $C_{CCT}$ [μF] |
| $T_{OD}$ [s]= | (0.50, | 1.00, | 1.50) x | $C_{CDT}$ [μF] |
| $T_{IOV1}$ [s]= | (0.05, | 0.10, | 0.15) x | $C_{CDT}$ [μF] |
| $T_{CIP}$ [s]= | (0.05, | 0.10, | 0.15) x | $C_{CCT}$ [μF] |

8.9 CTL Pin

The HY2550 Series has control pins. The CTL pin is used to control the COP and DOP pin output voltages. CTL pin takes precedence over the battery protection circuit.

**Conditions Set by CTL Pin**

| CTL Pin | COP Pin | DOP Pin |
|---|---|---|
| High | High-Z | VDD |
| Open | High-Z | VDD |
| Low | Normal status *1 | Normal status *1 |

*1. The status is controlled by the voltage detector.

**Caution: Please note unexpected behavior might occur when electrical potential difference between the CTL pin ('L' level) and VSS is generated through the external filter ($R_{VSS}$ and $C_{VSS}$) as a result of input voltage fluctuations.**

8.10 SEL&SEL5 Pin

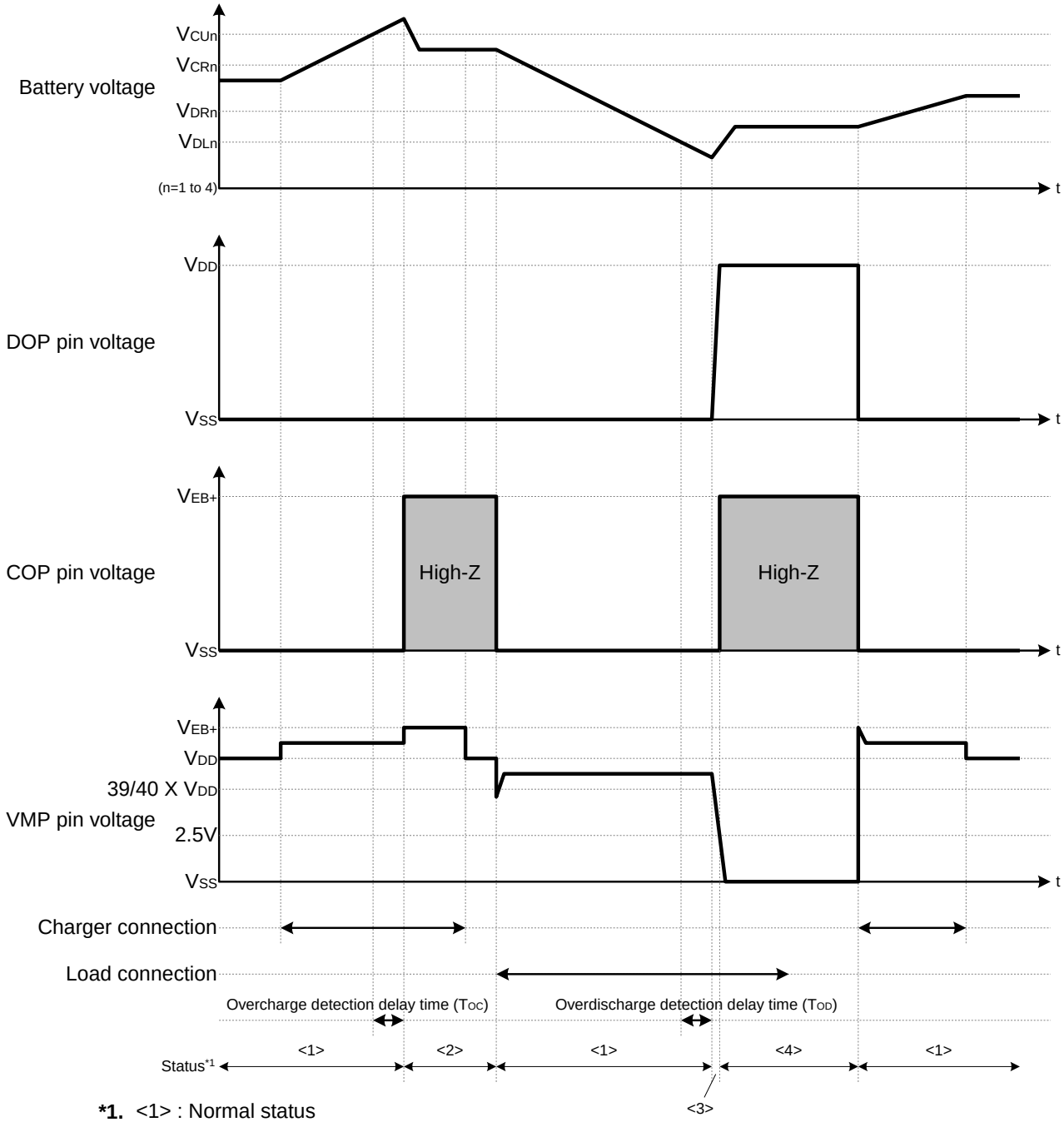
The HY2550 Series has two SELECT pins. The SEL pin is used to switch between 3-cell and 4-cell protection and the SEL5 pin is used to select 5-cell protection. When the SEL pin and SEL5 pin are low, overdischarge detection of the V4 cell is prohibited and an overdischarge is not detected even if the V4 cell is shorted, therefore, the V4 cell can be used for 3-cell protection. The SEL pin and SEL5 pin take precedence over the battery protection circuit. Use the SEL pin & SEL5 pin at high or low.

**Conditions Set by SEL Pin &SEL5 pin**

| SEL Pin | SEL5 Pin | Condition |
|---|---|---|
| High | High | 5-cell protection |
| High | Low | 4-cell protection |
| Low | Low | 3-cell protection |
| Open | Open | Undefined |

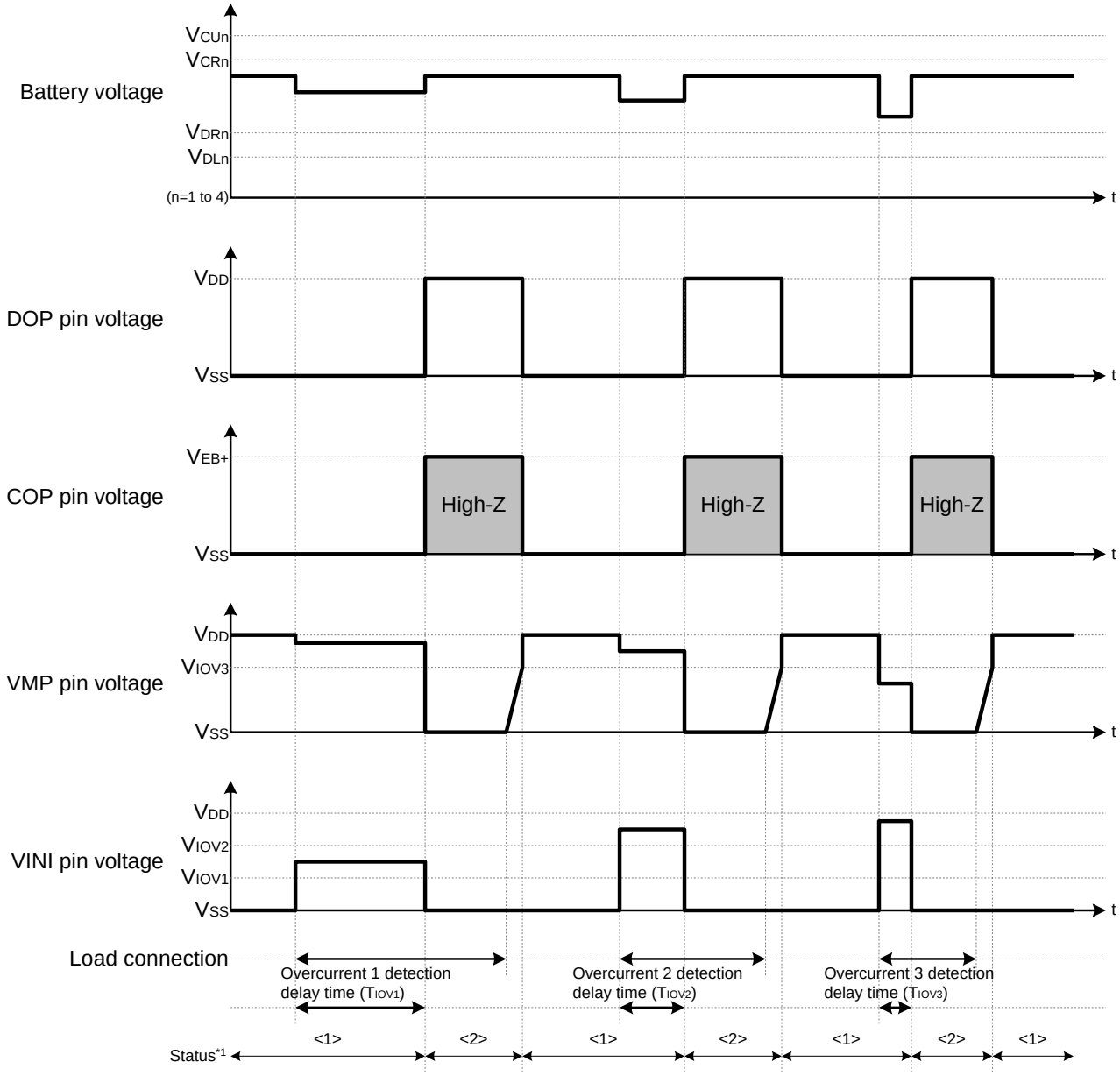
## 9. Timing Diagram

### (1) Overcharge Detection and Overdischarge Detection



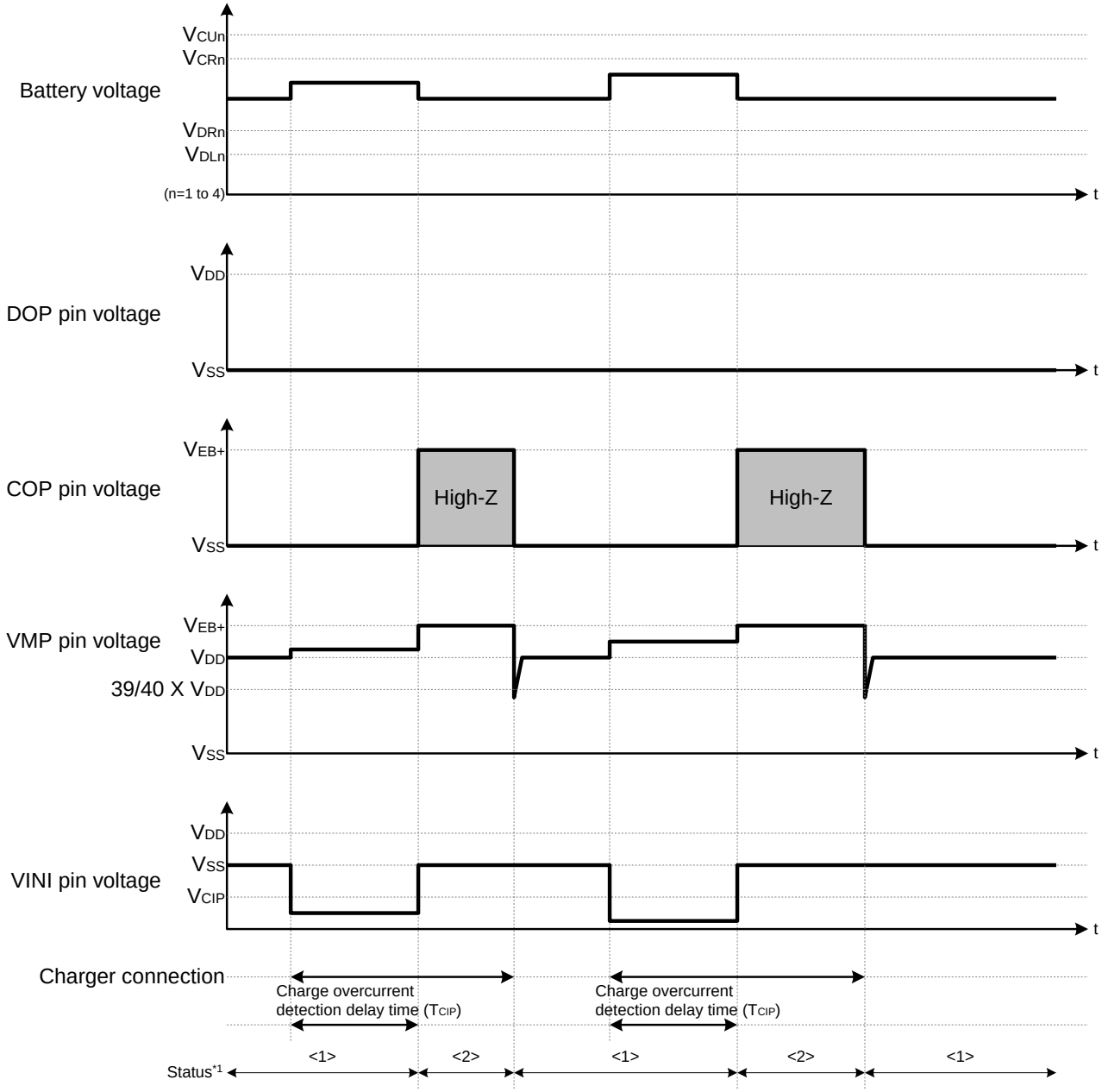

***1.** <1> : Normal status
<2> : Overcharge status
<3> : Overdischarge status
<4> : Power-down status

### (2) Discharge Overcurrent Detection




***1.** <1> : Normal status
<2> : Discharge overcurrent status

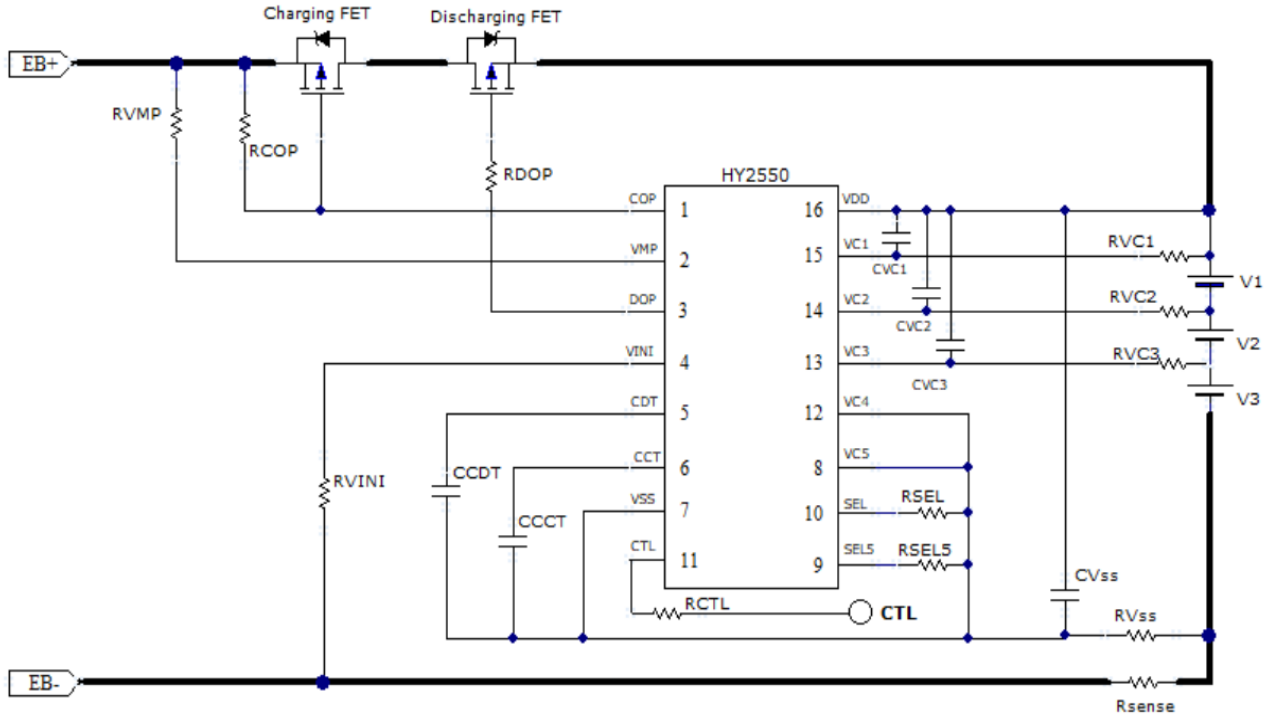
### (3) Charge Overcurrent Detection



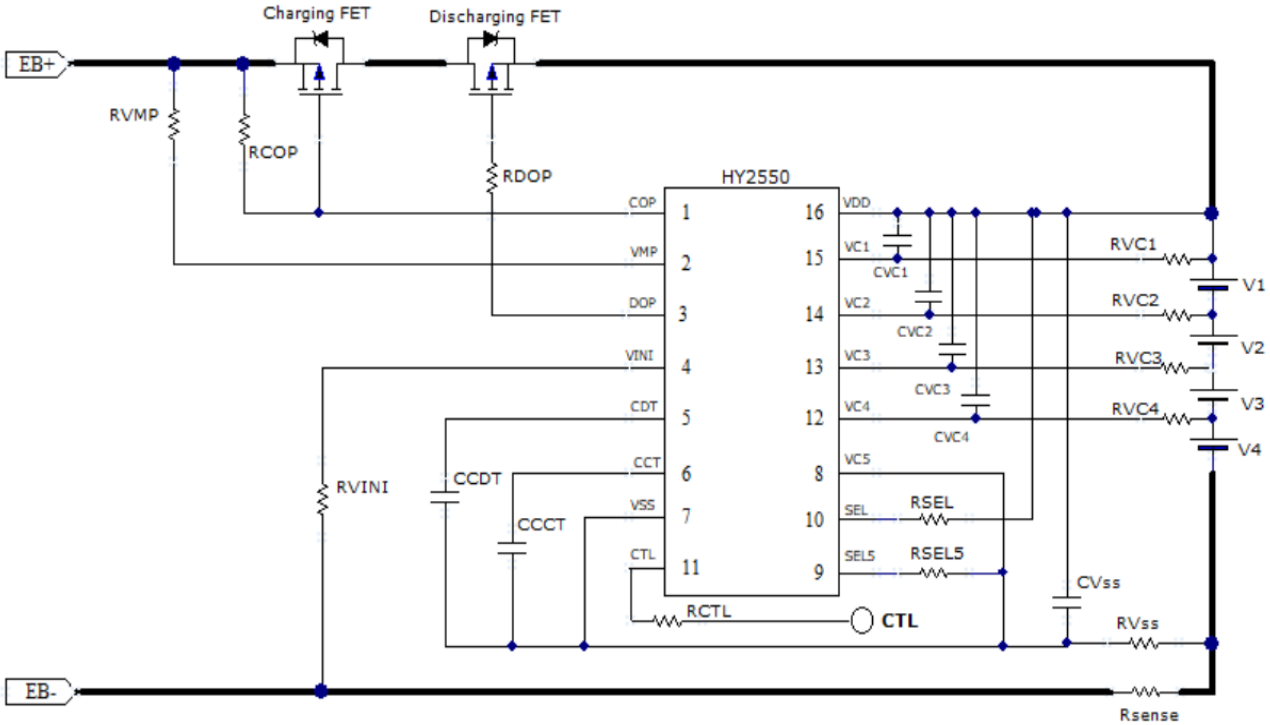

***1.** <1> : Normal status
<2> : Charge overcurrent status

## 10. Example of Application Circuit for Battery Protection IC

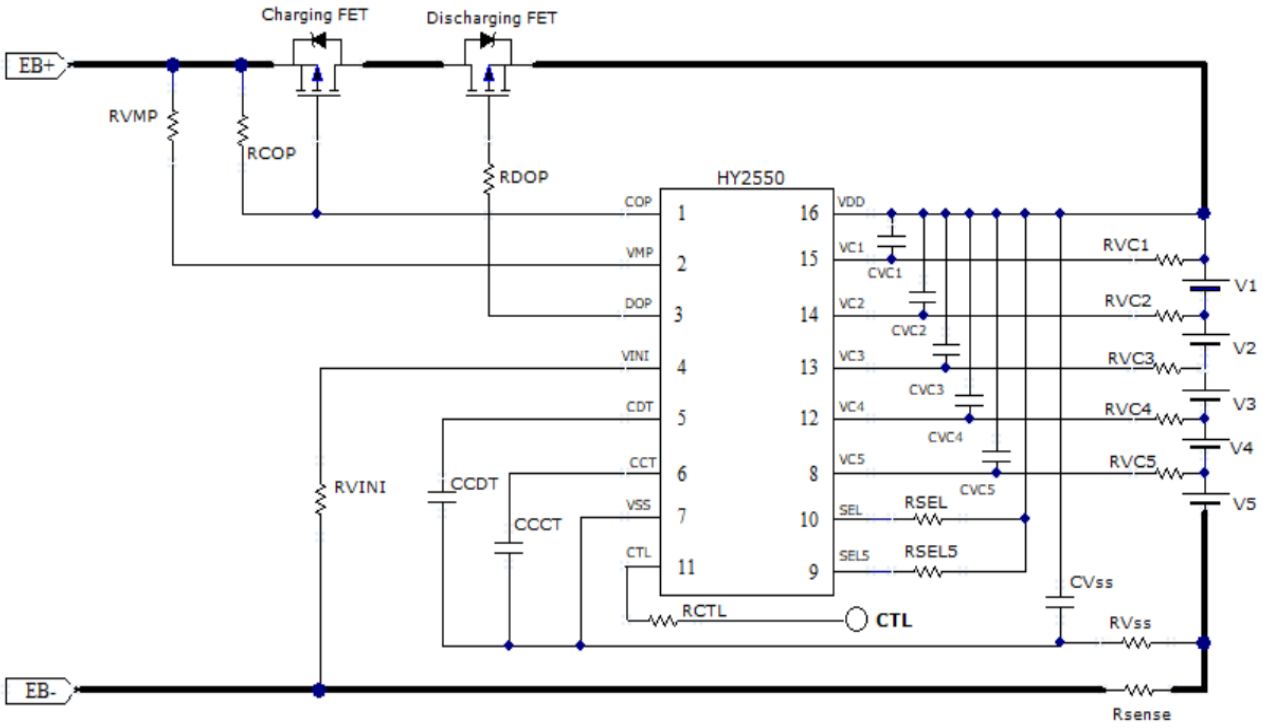
### 10.1 3-serial Cell




### 10.2 4-serial Cell



10.3 5-serial Cell

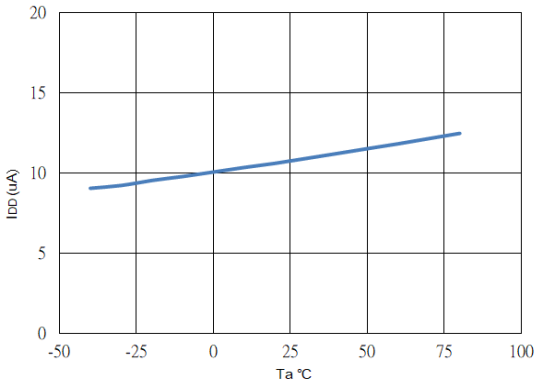


10.4 Parts List

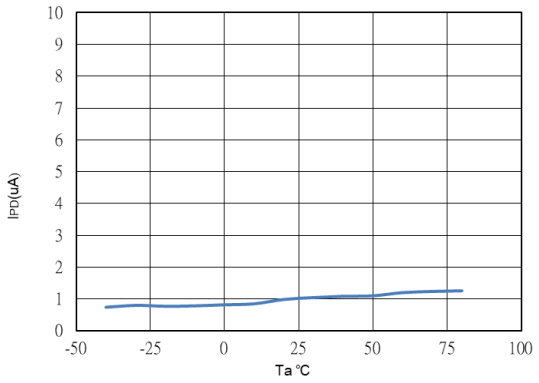
| Symbol | Min. | Typ. | Max. | Unit | Remark |
|---|---|---|---|---|---|
| $R_{VC1}$ | 0 | 1 | 1 | kΩ | |
| $R_{VC2}$ | 0 | 1 | 1 | kΩ | |
| $R_{VC3}$ | 0 | 1 | 1 | kΩ | |
| $R_{VC4}$ | 0 | 1 | 1 | kΩ | |
| $R_{VC5}$ | 0 | 1 | 1 | kΩ | |
| $R_{DOP}$ | 2 | 5.1 | 10 | kΩ | |
| $R_{COP}$ | 0.1 | 1 | 1 | MΩ | |
| $R_{VMP}$ | 1 | 5.1 | 10 | kΩ | |
| $R_{CTL}$ | 1 | 1 | 100 | kΩ | |
| $R_{VINI}$ | 1 | 1 | 100 | kΩ | |
| $R_{SEL}$ | 1 | 1 | 100 | kΩ | |
| $R_{SEL5}$ | 1 | 1 | 100 | kΩ | |
| $R_{SENSE}$ | 0 | - | - | mΩ | |
| $R_{VSS}$ | 10 | 51 | 51 | Ω | |
| $C_{VC1}$ | 0 | 0.1 | 0.33 | μF | |
| $C_{VC2}$ | 0 | 0.1 | 0.33 | μF | |
| $C_{VC3}$ | 0 | 0.1 | 0.33 | μF | |
| $C_{VC4}$ | 0 | 0.1 | 0.33 | μF | |
| $C_{VC5}$ | 0 | 0.1 | 0.33 | μF | |
| $C_{CCT}$ | 0.01 | 0.1 | - | μF | |
| $C_{CDT}$ | 0.07 | 0.1 | - | μF | |
| $C_{VSS}$ | 2.2 | 2.2 | 10 | μF | |

## 11. Temperature Characteristics (Typical Value)

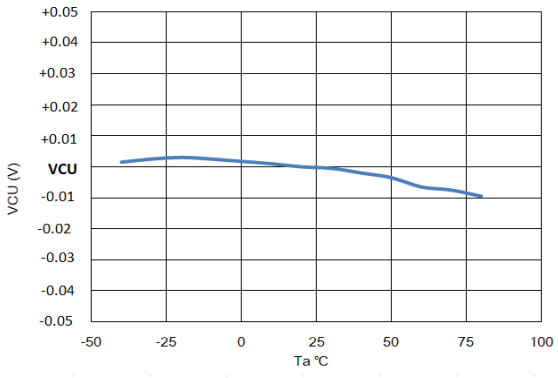
(1) $I_{DD}$ vs. Ta



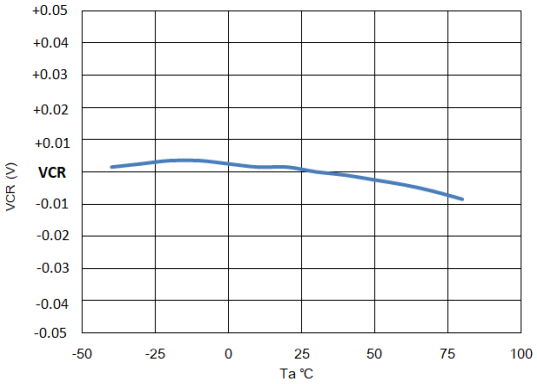

(2) $I_{PD}$ vs. Ta



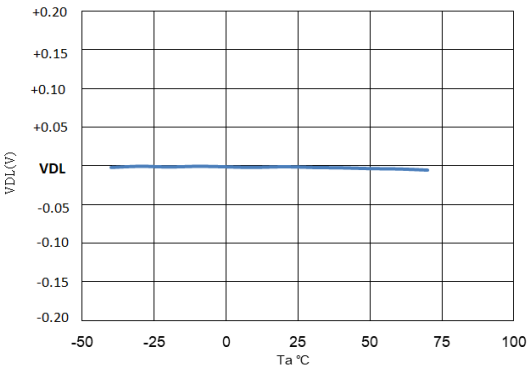

(3) $V_{CU}$ vs. Ta



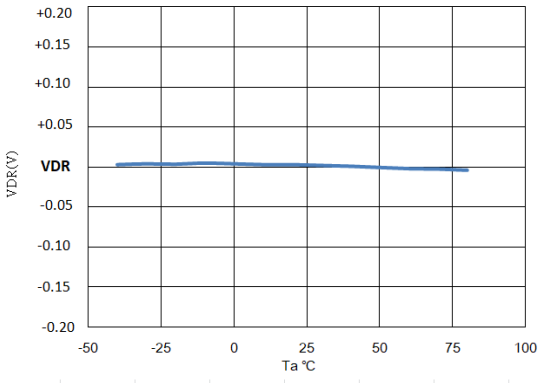

(4) $V_{CR}$ vs. Ta



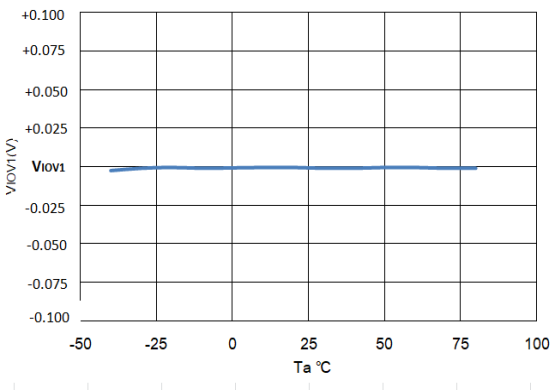

(5) $V_{DL}$ vs. Ta



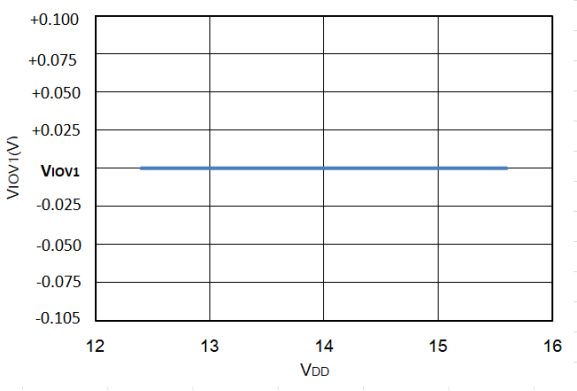

(6) $V_{DR}$ vs. Ta



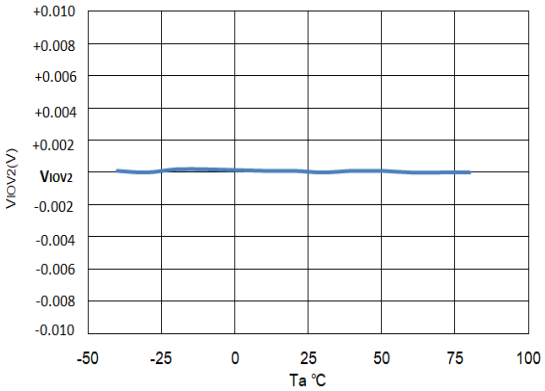
### (7)$V_{iov1}$ vs. Ta



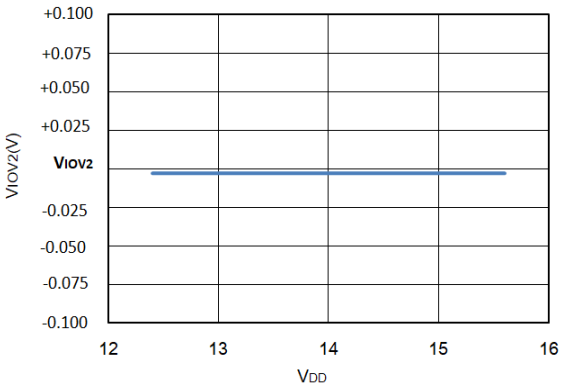

### (8) $V_{iov1}$ vs. VDD



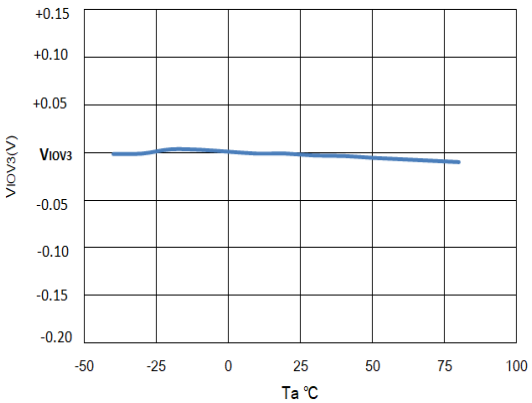

### (9) $V_{iov2}$ vs. Ta



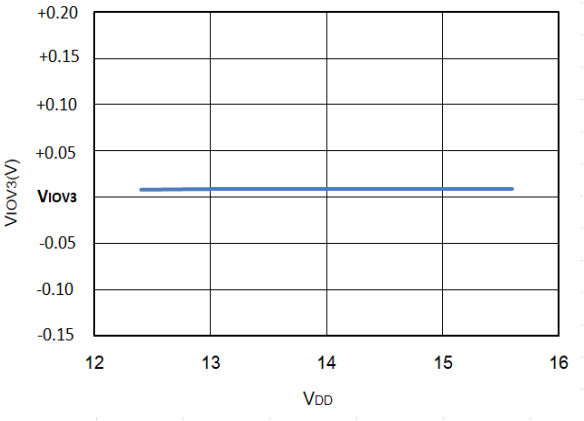

### (10) $V_{iov2}$ vs. $V_{DD}$



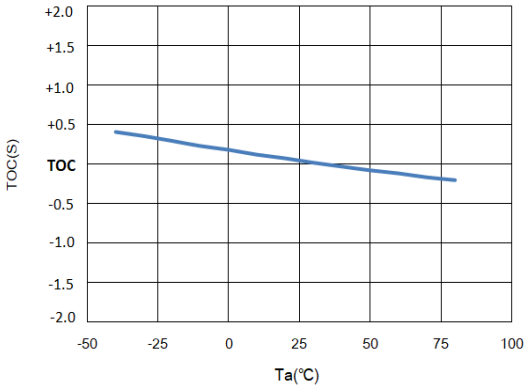

### (11) $V_{iov3}$ vs. Ta



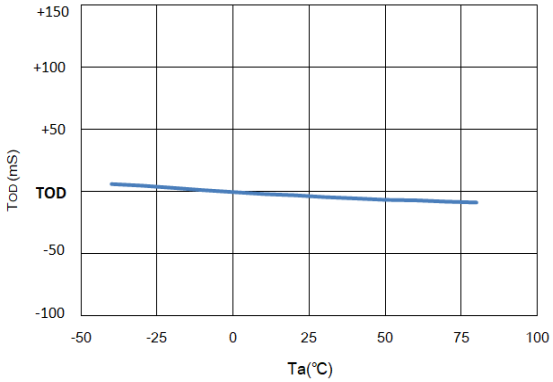

### (12) $V_{iov3}$ vs. VDD



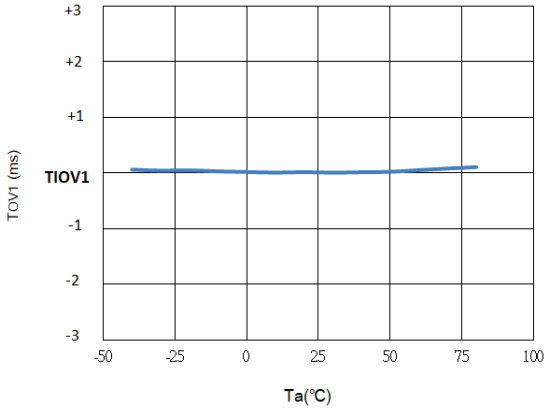
(13) TOC vs. Ta



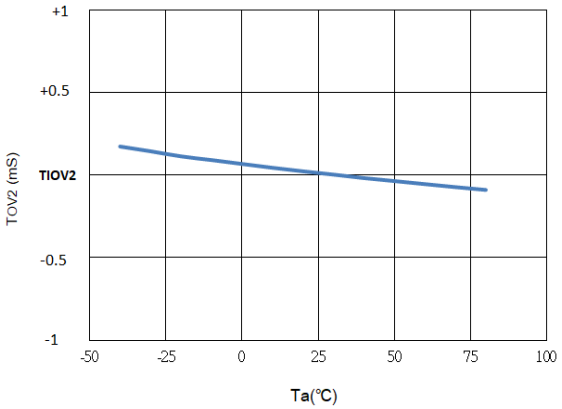

(14)TOD vs.Ta



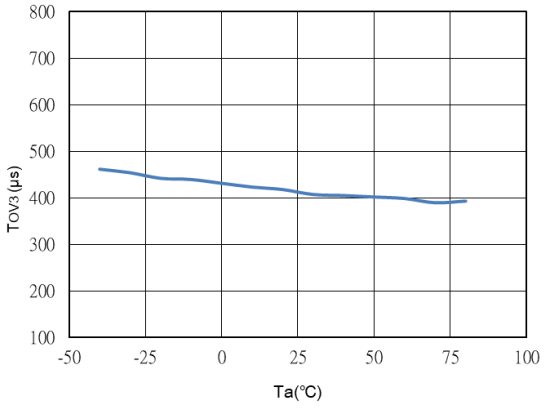

(15) TIOV1 vs. Ta




(16)TIOV2 vs.Ta

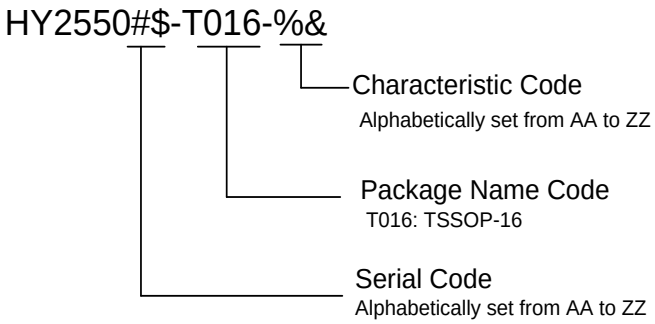



(17)TIOV3 vs.Ta



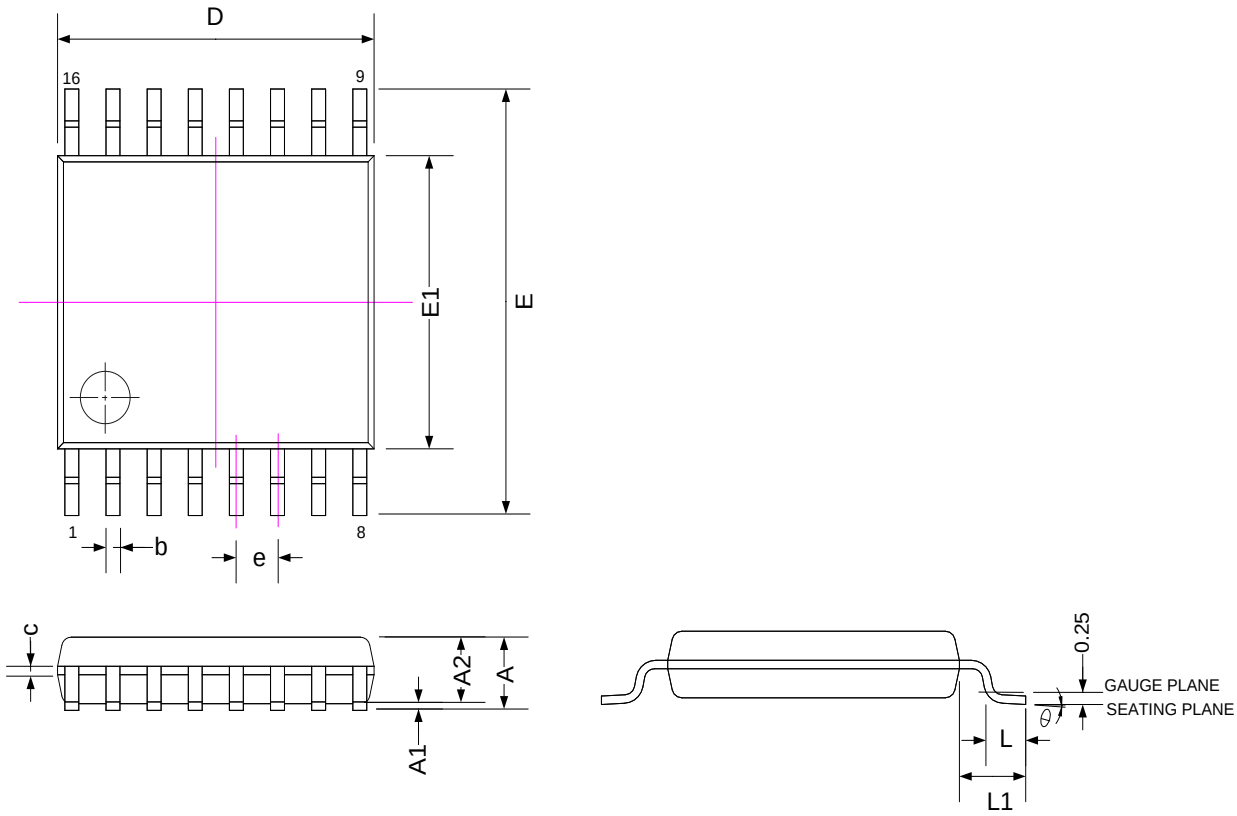
## 12. Ordering Information

- Definition of Product Name



## 13. Package Information

Package Outline Drawing--- TSSOP16 Unit : mm



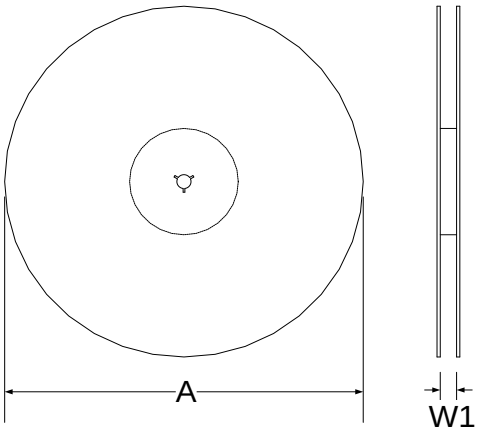

| SYMBOLS | MIN | NOM | MAX |
|---|---|---|---|
| A | - | - | 1.20 |
| A1 | 0.00 | - | 0.15 |
| A2 | 0.80 | 1.00 | 1.05 |
| b | 0.19 | - | 0.30 |
| c | 0.09 | - | 0.20 |
| D | 4.90 | 5.00 | 5.10 |
| E1 | 4.30 | 4.40 | 4.50 |
| E | 6.40 BSC. | | |
| L | 0.45 | 0.60 | 0.75 |
| L1 | 1.0 REF. | | |
| e | 0.65 BSC. | | |
| θ° | 0 | - | 8 |

Note:

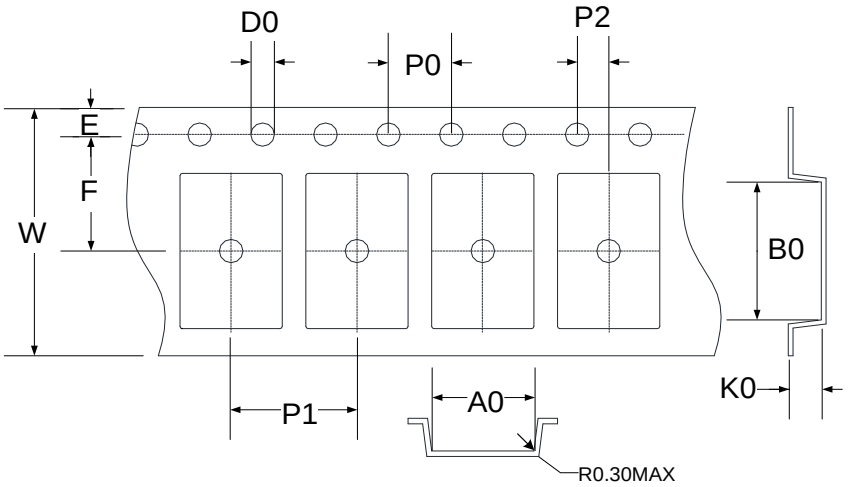
1. All dimensions refer to JEDEC OUTLINE MO -153.
2. Do not include Mold Flash or Protrusions.

## 14. Tape & Reel Information

Reel Dimensions

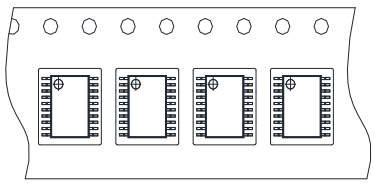



Carrier Tape Dimensions




| SYMBOLS | Reel Dimensions | | Carrier Tape Dimensions | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | A | W1 | A0 | B0 | K0 | P0 | P1 | P2 | E | F | D0 | W |
| Spec. | 330 | 12.5 | 6.80 | 5.40 | 1.50 | 4.00 | 8.00 | 2.00 | 1.75 | 5.50 | 1.50 | 12.00 |
| Tolerance | +6/-3 | +1.5/-0 | ±0.10 | ±0.10 | ±0.10 | ±0.10 | ±0.10 | ±0.05 | ±0.10 | ±0.05 | +0.1/-0 | ±0.30 |

**Pin1 direction**



## 15. Revision Record

The larger modifications of this document are described below, but changes of punctuation marks and fonts are not within the scope of description.

| Version | Page | Summary of Modification |
|---|---|---|
| V01 | - | First release. |