HY2151 Series
Datasheet

Protection IC for 3-cell / 4-cell / 5-cell Lithium Ion/Lithium Polymer Batteries
(For Secondary Protection)

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1. General Description

HY2151 is a secondary protection IC for cell over-voltage protection of 3-cell / 4-cell / 5-cell lithium ion and lithium polymer rechargeable batteries. The device integrates accurate voltage detection and protection delay circuitry for best cell over-voltage protection purpose.

2. Features

The features that whole series of HY2151 comprised are as follows:

(1) High-accuracy voltage detection circuit (n = 1, 2, 3, 4, 5)

- Overcharge detection voltage V_{CUn} 4.0V to 5.0V (50mV step) Accuracy: ±25mV (25°C) Accuracy: ±30mV (-20°C to 60°C)
- Overcharge release voltage V_{CRn} 3.8V to 5.0V Accuracy: ±50mV

(2) Delay time is set by internal circuit (external capacitor is not needed)

- Overcharge detection delay 1/2/4/6 s Accuracy: ±20%

(3) Built-in timer reset delay circuit

(4) Output is CMOS output Active "H"

(5) Output logic active high maximum time: Not Limited

(6) Low current consumption (25°C; n = 1, 2, 3, 4, 5)

- Operation mode (Vcu= 4V) 3.2 μA typ., 5.0μA max.
- Overdischarge mode (Vcu= 2.3V) 0.4 μA typ., 1.0μA max.

(7) High voltage resistant design: the absolute maximum rated value is 32V.

(8) Wide operating temperature range: -40°C to +85°C

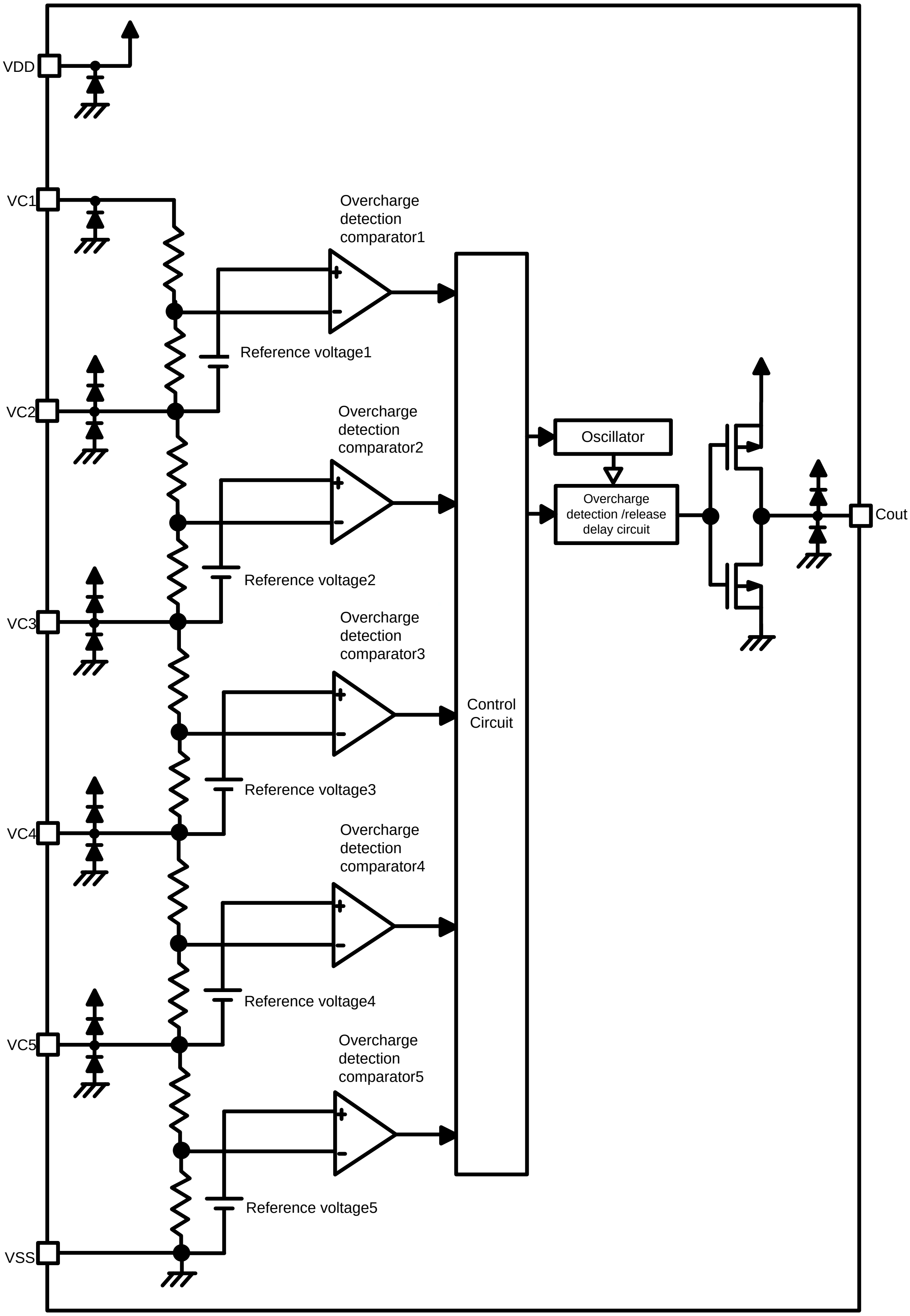
(9) Small package: DFN-1.97*2.46-8L

(10) Halogen free green product

3. Applications

- 3-cell / 4-cell / 5-cell lithium ion rechargeable battery pack (for secondary protection)
- 3-cell / 4-cell / 5-cell lithium polymer rechargeable battery pack (for secondary protection)

4. Block Diagram



5. Ordering Information

- Definition of Product Name

HY2151－#%$&

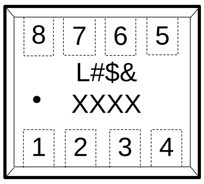
- & : Characteristic Code
  Alphabetically set from A to Z
- $: Delay Time Code
  Numerically set from 1 to 9
- % : Package Name Code
  J：DFN-1.97*2.46-8L
- # : Serial Code
  Alphabetically set from A to Z

6. Pin Configuration and Package Marking Information

- **DFN-1.97*2.46-8L Package**

Table 1

Pin	Symbol	Description
1	VDD	Power end, positive power input pin.
2	V_{C1}	Connection pin for positive the voltage of battery 1.
3	V_{C2}	Connection pin for negative the voltage of battery 1, positive the voltage of battery 2.
4	V_{C3}	Connection pin for negative the voltage of battery 2, positive the voltage of battery 3.
5	V_{C4}	Connection pin for negative the voltage of battery 3, positive the voltage of battery 4.
6	V_{C5}	Connection pin for negative the voltage of battery 4, positive the voltage of battery 5.
7	VSS	Ground end, connection pin for negative the voltage of battery 5.
8	COUT	FET gate connection pin for charging control



L: Product Name.
#: Serial code. Alphabetically set from A to Z
$: Delay time code. Numerically set from 1 to 9
&: Feature code. Alphabetically set from A to Z
XXXX: Traceability code

7. Absolute Maximum Rated Value

Table2 (VSS = 0V, Ta=25°C, unless indicated otherwise)

Item	Symbol	Specification	Unit
Input Voltage between VDD and VSS	VDD	VSS-0.3 to VSS+26	V
V_{C1} Input Voltage	V_{C1}	VC2-0.3 to VC2+5.5	V
V_{C2} Input Voltage	V_{C2}	VC3-0.3 to VC3+5.5	V
V_{C3} Input Voltage	V_{C3}	VC4-0.3 to VC4+5.5	V
V_{C4} Input Voltage	V_{C4}	VC5-0.3 to VC5+5.5	V
V_{C5} Input Voltage	V_{C5}	VSS-0.3 to VSS+5.5	V
COUT Output Voltage	V_{COUT}	VSS-0.3 to V_{DD}+0.3	V
Operating Temperature Range	T_{OP}	-40 to +85	°C
Storage Temperature Range	T_{ST}	-55 to +125	°C
Tolerant Power Consumption	P_D	250	mW

8. Electrical Characteristics

Table 3 (VSS = 0V, Ta = 25°C, unless indicated otherwise)

Item	Symbol	Condition	Min	Typ	Max	Unit
Input Voltage						
Operating Voltage	V_{DSOP}	VDD to VSS.	3.6	-	26	V
Current Consumption						
Operating Current (*C)	I_{DD}	V_{Celln} = 4V (*1)	-	3.2	5.0	μA
Standby Current(*C)	I_{PD}	V_{Celln} = 2.3V (*1)	-	0.4	1.0	μA
VC2 pin Current (*D)	I_{VC2}	VC1=VC2=VC3=VC4=VC5=4V,	-0.3	0	0.3	μA
VC3 pin Current (*D)	I_{VC3}	VC1=VC2=VC3=VC4=VC5=4V,	-0.3	0	0.3	μA
VC4 pin Current (*D)	I_{VC4}	VC1=VC2=VC3=VC4=VC5=4V,	-0.3	0	0.3	μA
VC5 pin Current (*D)	I_{VC5}	VC1=VC2=VC3=VC4=VC5=4V,	-0.3	0	0.3	μA
Detection Voltage						
Overcharge Detection Voltage n (*1) (*A)	V_{CUn}		V_{CU} – 0.02	V_{CU}	V_{CU} + 0.02	V
Overcharge Release Voltage n (*1) (*A)	V_{CRn}		V_{CR} – 0.05	V_{CR}	V_{CR} + 0.05	V
Delay Time						
Overcharge Detection Delay Time(*B)	T_{OCn}	V_{Celln} = 4V (*3) V_{Cell1} = 4V → 4.7V	0.8 x T_{OC}	T_{OC}	1.2 x T_{OC}	s
Overcharge Release Delay Time(*B)	T_{CRn}	V_{Celln} = 4V (*3) V_{Cell1} = 4.7V → 4V	12	16	20	ms
Reset Delay Time of Overcharge Detection Counter(*B)	T_{DTRn}	V_{Celln} = 4V (*3) V_{Cell1} = V_{CU1} + 50mV → V_{CR1} – 100mV → V_{CU1} + 50mV → V_{CR1} – 100mV	6	12	20	ms
Control Pin Output Voltage						
High Voltage of COUT Output	V_{COH}	V_{Celln} = 4V (*3) V_{Cell1} = 4V → 4.7V		VDD		V
Low Voltage of COUT Output	V_{COL}	V_{Celln} = 4V (*1)	-	0.1	0.5	V
Output Source Current of COUT Output	I_{COH}	V_{Celln} = 4V (*3) V_{Cell1} = 4V → 4.7V	-	-	-20	μA
Output Sink Current of COUT Output	I_{COL}	V_{Celln} = 4V (*3) V_{Cell1} = 4.7V → 4V	20	-	-	μA

Description:

*1. n = 1, 2, 3, 4, 5

*2. The parameters within this temperature range are design guarantee values instead of screened values from high, low temperature measurement.

*3. n = 1, 2, 3, 4, 5

*A ~ *D indicates test circuit shown in following page.

Table 4 (VSS = 0V, Ta =-20°C~60°C, unless indicated otherwise)

Item	Symbol	Condition	Min	Typ	Max	Unit
Input Voltage						
Operating Voltage	V_{DSOP}	VDD to VSS.	3.6	-	28	V
Current Consumption						
Operating Current (*C)	I_{DD}	V_{Celln} = 4V (*1)	-	3.2	5.0	μA
Standby Current(*C)	I_{PD}	V_{Celln} = 2.3V (*1)	-	0.4	1.0	μA
VC2 pin Current (*D)	I_{VC2}	VC1=VC2=VC3=VC4=VC5=4V,	-0.3	0	0.3	μA
VC3 pin Current (*D)	I_{VC3}	VC1=VC2=VC3=VC4=VC5=4V,	-0.3	0	0.3	μA
VC4 pin Current (*D)	I_{VC4}	VC1=VC2=VC3=VC4=VC5=4V,	-0.3	0	0.3	μA
VC5 pin Current (*D)	I_{VC5}	VC1=VC2=VC3=VC4=VC5=4V,	-0.3	0	0.3	μA
Detection Voltage						
Overcharge Detection Voltage n (*1) (*A)	V_{CUn}		V_{CU} – 0.025	V_{CU}	V_{CU} + 0.025	V
Overcharge Release Voltage n (*1) (*A)	V_{CRn}		V_{CR} – 0.055	V_{CR}	V_{CR} + 0.055	V
Delay Time						
Overcharge Detection Delay Time(*B)	T_{OCn}	V_{Celln} = 4V (*3) V_{Cell1} = 4V → 4.7V	0.7 x T_{OC}	T_{OC}	1.3 x T_{OC}	s
Overcharge Release Delay Time(*B)	T_{CRn}	V_{Celln} = 4V (*3) V_{Cell1} = 4.7V → 4V	11	16	21	ms
Reset Delay Time of Overcharge Detection Counter(*B)	T_{DTRn}	V_{Celln} = 4V (*3) V_{Cell1} = V_{CU1} + 50mV → V_{CR1} – 100mV → V_{CU1} + 50mV → V_{CR1} – 100mV	5	12	21	ms
Control Pin Output Voltage						
High Voltage of COUT Output	V_{COH}	V_{Celln} = 4V (*3) V_{Cell1} = 4V → 4.7V		VDD		V
Low Voltage of COUT Output	V_{COL}	V_{Celln} = 4V (*1)	-	0.1	0.5	V
Output Source Current of COUT Output	I_{COH}	V_{Celln} = 4V (*3) V_{Cell1} = 4V → 4.7V	-	-	-20	μA
Output Sink Current of COUT Output	I_{COL}	V_{Celln} = 4V (*3) V_{Cell1} = 4.7V → 4V	20	-	-	μA

Description:

*1. n = 1, 2, 3, 4, 5

*2. The parameters within this temperature range are design guarantee values instead of screened values from high, low temperature measurement.

*3. n = 1, 2, 3, 4, 5

*A ~ *D indicates test circuit shown in following page.

Table 5 (VSS = 0V, Ta = -40°C~85°C, unless indicated otherwise)

Item	Symbol	Condition	Min	Typ	Max	Unit
Input Voltage						
Operating Voltage	V_{DSOP}	VDD to VSS.	3.6	-	28	V
Current Consumption						
Operating Current (*C)	I_{DD}	V_{CellN} = 4V (*1)	-	3.2	5.0	μA
Standby Current(*C)	I_{PD}	V_{CellN} = 2.3V (*1)	-	0.4	1.0	μA
VC2 pin Current (*D)	I_{VC2}	VC1=VC2=VC3=VC4=VC5=4V,	-0.3	0	0.3	μA
VC3 pin Current (*D)	I_{VC3}	VC1=VC2=VC3=VC4=VC5=4V,	-0.3	0	0.3	μA
VC4 pin Current (*D)	I_{VC4}	VC1=VC2=VC3=VC4=VC5=4V,	-0.3	0	0.3	μA
VC5 pin Current (*D)	I_{VC5}	VC1=VC2=VC3=VC4=VC5=4V,	-0.3	0	0.3	μA
Detection Voltage						
Overcharge Detection Voltage n (*1) (*A)	V_{CUn}		V_{CU} – 0.06	V_{CU}	V_{CU} + 0.033	V
Overcharge Release Voltage n (*1) (*A)	V_{CRn}		V_{CR} – 0.08	V_{CR}	V_{CR} + 0.062	V
Delay Time						
Overcharge Detection Delay Time(*B)	T_{OCn}	V_{CellN} = 4V (*3) V_{Cell1} = 4V → 4.7V	0.6 x T_{OC}	T_{OC}	1.4 x T_{OC}	s
Overcharge Release Delay Time(*B)	T_{CRn}	V_{CellN} = 4V (*3) V_{Cell1} = 4.7V → 4V	10	16	22	ms
Reset Delay Time of Overcharge Detection Counter(*B)	T_{DTRn}	V_{CellN} = 4V (*3) V_{Cell1} = V_{CU1} + 50mV → V_{CR1} – 100mV → V_{CU1} + 50mV → V_{CR1} – 100mV	4	12	22	ms
Control Pin Output Voltage						
High Voltage of COUT Output	V_{COH}	V_{CellN} = 4V (*3) V_{Cell1} = 4V → 4.7V		VDD		V
Low Voltage of COUT Output	V_{COL}	V_{CellN} = 4V (*1)	-	0.1	0.5	V
Output Source Current of COUT Output	I_{COH}	V_{CellN} = 4V (*3) V_{Cell1} = 4V → 4.7V	-	-	-20	μA
Output Sink Current of COUT Output	I_{COL}	V_{CellN} = 4V (*3) V_{Cell1} = 4.7V → 4V	20	-	-	μA

Description:

*1. n = 1, 2, 3, 4, 5

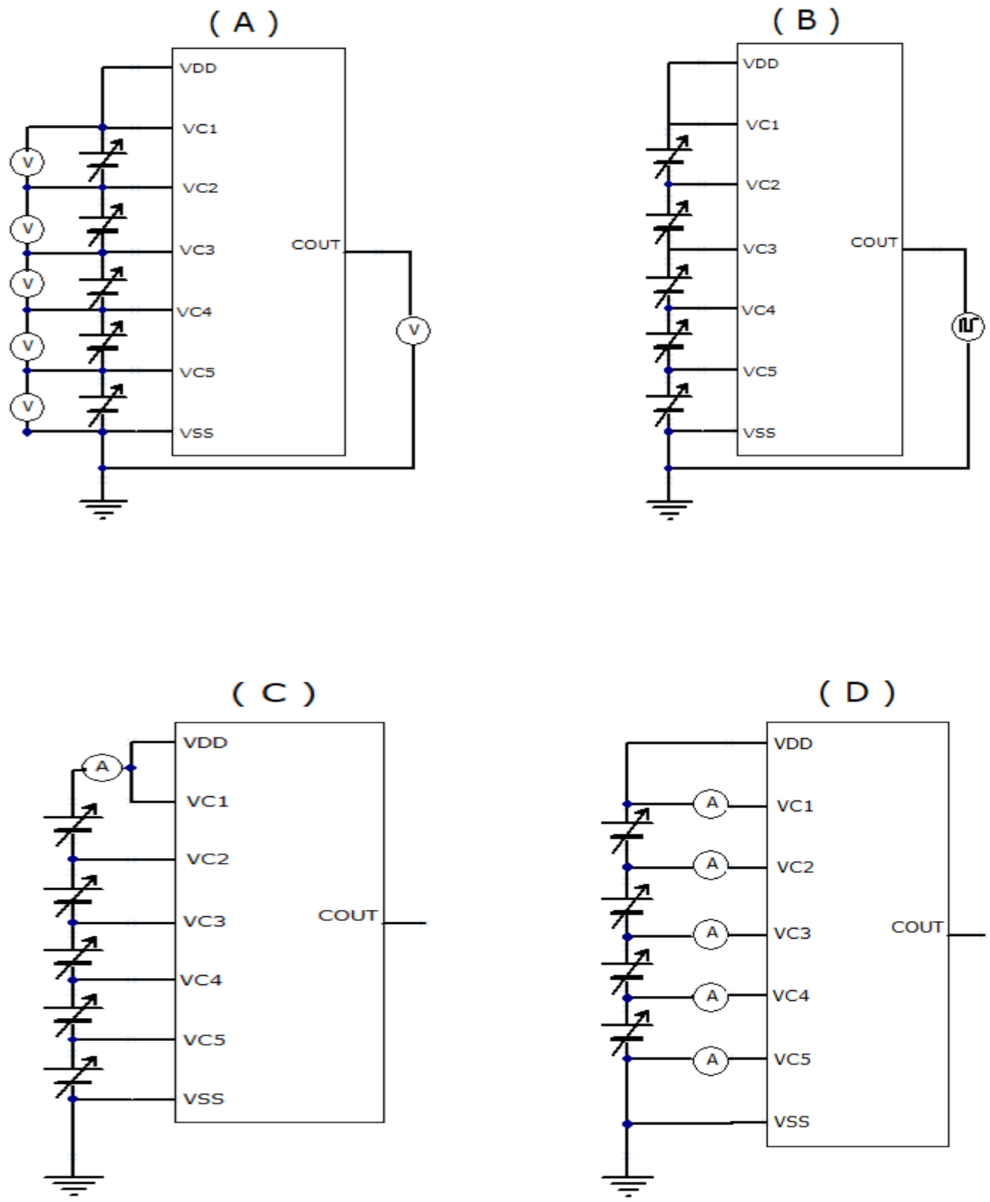
*2. The parameters within this temperature range are design guarantee values instead of screened values from high, low temperature measurement.

*3. n = 1, 2, 3, 4, 5

*A ~ *D indicates test circuit shown in following page.

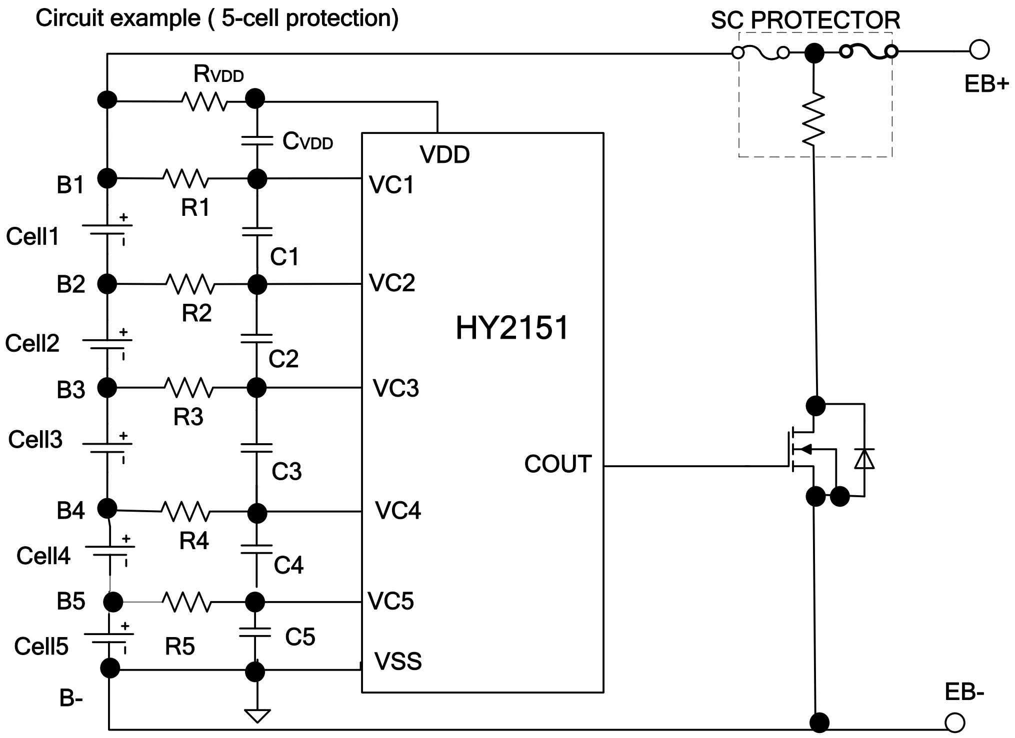
9. Test Circuit

Test Circuit

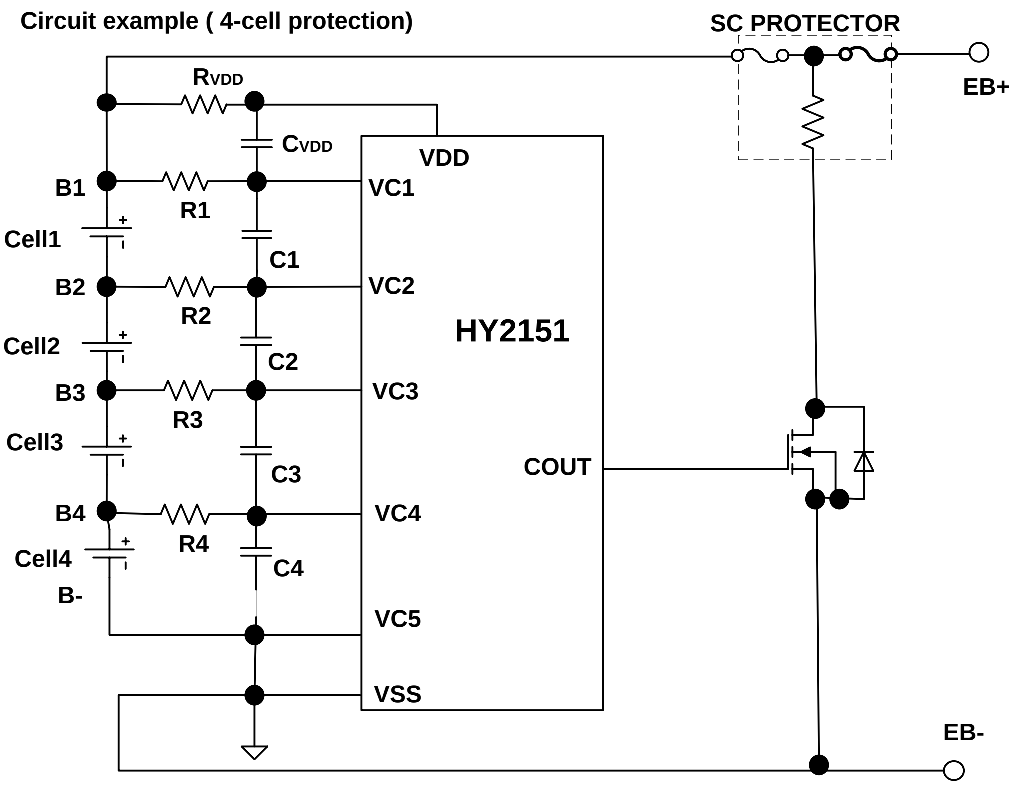


10. Example of Application Circuit for Battery Protection IC

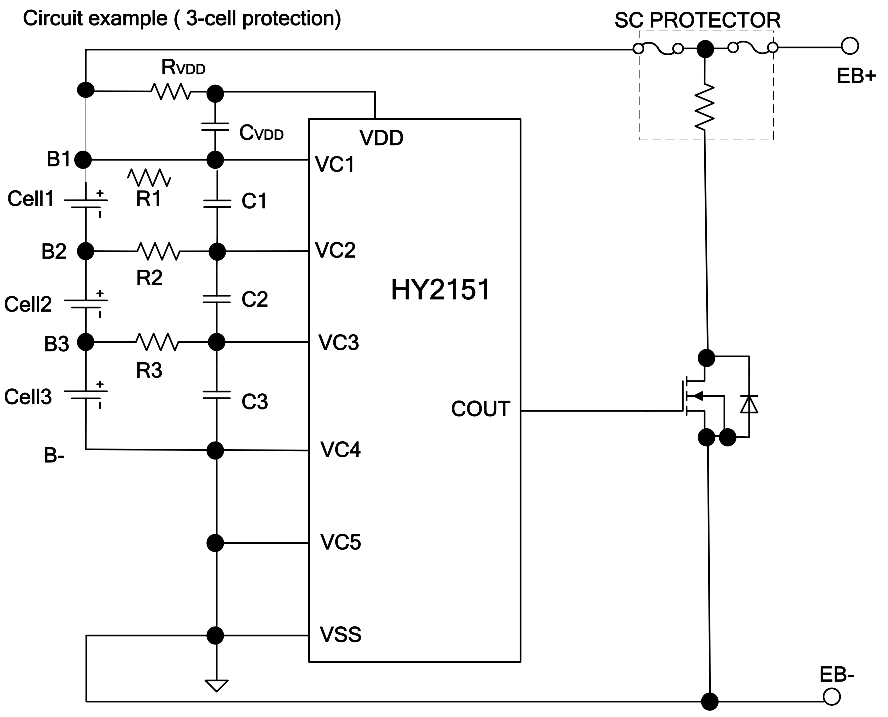
10.1 5-Cell in Series Connection



10.2 4-Cell in Series Connection



10.3 3-Cell in Series Connection



Symbol	Device Name	Purpose	Min.	Typ.	Max.	Remark
RVDD	Resistor	Limiting current, stabilizing VDD	100Ω	**100Ω**	1KΩ	*1
R1~R5	Resistor	Filtering, stabilizing VCn	330Ω	**1kΩ**	1kΩ	*2
CVDD	Capacitor	Filtering, stabilizing VDD	0.01μF	**0.1μF**	1.0μF	*1
C1~C5	Capacitor	Filtering, stabilizing VCn	0.01μF	**0.1μF**	1.0μF	*2

1. RVDD and CVDD are capable of VDD voltage stabilization. If RVDD is connected with an over small resistor, IC operation may be unstable because there is larger fluctuation on Cell voltage due to current. If RVDD is connected with an over large resistor, unpredicted result may be resulted from voltage difference between voltages on VDD pin and VC1 pin because of voltage difference across RVDD due to current consumption of the device itself. Therefore, RVDD is ranged from 100Ω to 1KΩ and CVDD is ranged from 0.01μF to 1.0μF, and never connect capacitor below 0.01μF.
2. R1 to R5 and C1 to C5 are capable of stabilizing voltages of cell1 to cell5. If R1 to R5 are connected to over large resistor, detection voltage precision would be impacted because of voltage difference due to current consumption. Therefore, R1 to R5 should be connected with resistor below 1KΩ, and C1 to C5 should be connected with capacitor equal to or above 0.01μF.
3. The typical application circuit diagram above is only for reference. The performance of the circuit depends on PCB layout and external components to a great extent. Sufficient evaluation and test are necessary in real application.

Caution：

1. The parameters above may be changed without announce in advance. Please download the latest ver. of Specification from our website. Our website is: http://www.hycontek.com.
2. If peripheral devices are to be adjusted, customers are recommended to conduct sufficient evaluation and test in advance.

11. Description of Operation

11.1 Overcharge Status

The device detects the voltage of battery cell 1 connected between V_{C1} and V_{C2} pins, the voltage of battery cell 2 connected between V_{C2} and V_{C3} pins, the voltage of battery cell 3 connected between V_{C3} and V_{C4} pins, the voltage of battery cell 4 connected between V_{C4} and Vc5 pins and the voltage of battery cell 5 connected between V_{C5} and VSS pins continuously in normal operation.

Overcharge Status: When the voltage of any battery cell is higher than or equal to *Overcharge Detection Voltage* (V_{CUn}) and the sustaining time of such status is larger than or equal to *Overcharge Detection Delay Time* (T_{OCn}), the output voltage at COUT pin of the device becomes high level (V_{COH}) from low level (V_{COL}), such that the MOSFET for charging control blows the fuse on power path, and charging is stopped. Such status is referred to as Overcharge Status. Otherwise, COUT pin of the device keeps at low level (V_{COL}).

Overcharge Status Release: When the voltage of battery cell 1, battery cell 2, battery cell 3 and battery cell 4 is all lower than or equal to *Overcharge Release Voltage* (V_{CRn}) and the sustaining time of such status is larger than or equal to *Overcharge Release Delay Time* (T_{CRn}), the output voltage at COUT pin of the device becomes low level (V_{COL}) from high level (V_{COH}), such that Overcharge Status is released and normal operating status is returned. Otherwise, COUT pin of the device keeps at high level (V_{COH}) until T_{COH} expired if applied.

Caution:

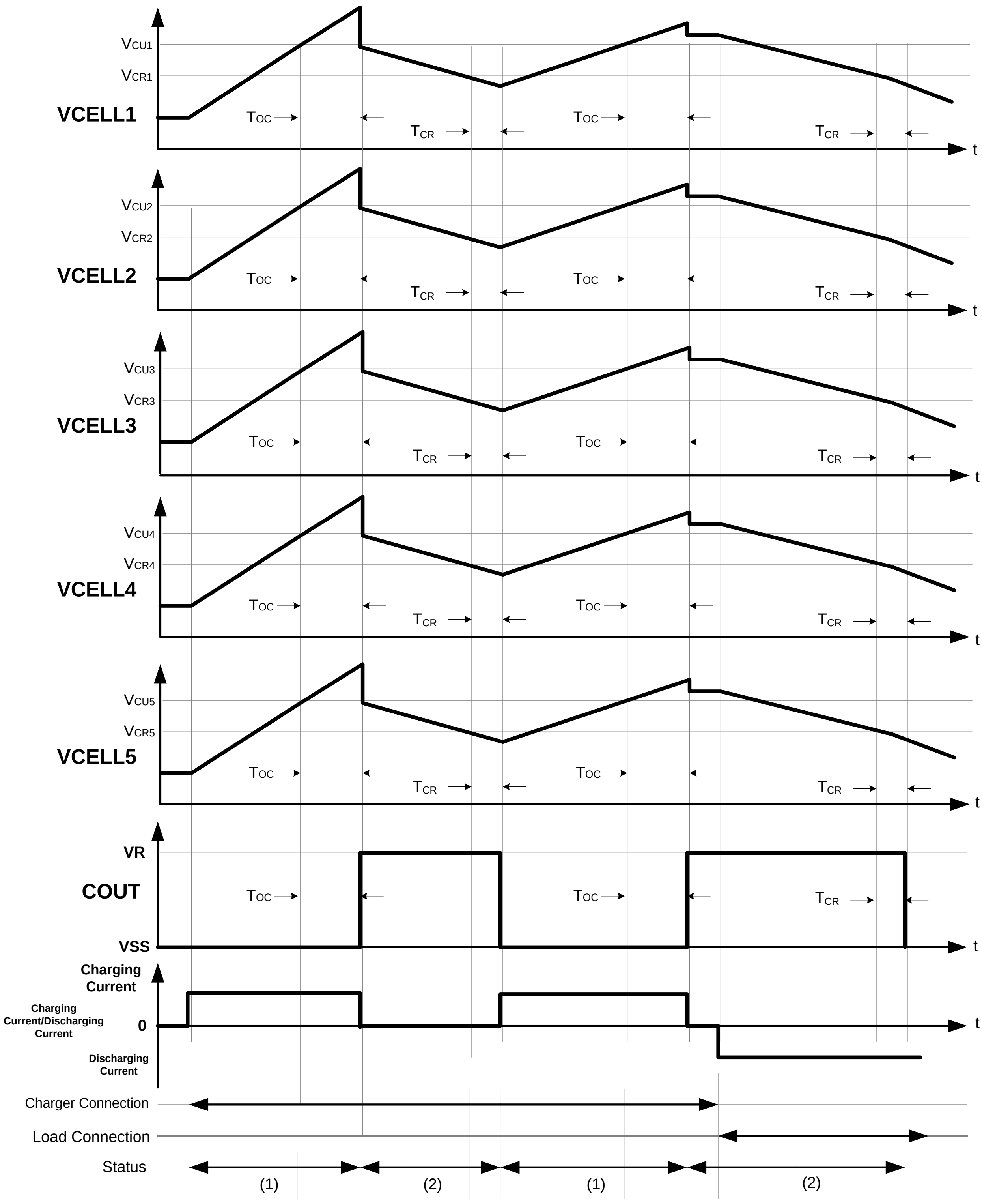
1. The overcharge delay time is a built-in fixed output. If the overcharge detection counter is reset, the overcharge protection status would be released and the normal status would be returned.
2. The device would still enter the overcharge protection status even though only the voltage of one battery keeps higher than the overcharge detection voltage and the sustaining time is beyond the overcharge detection delay time.
3. If the voltage of one battery is lower than the overcharge detection voltage due to noise or other causes while the voltage of all other batteries are all higher than the overcharge detection voltage in the overcharge detection delay time, the sustained period of time with voltage higher than the overcharge detection voltage would be retained and accumulated. As the accumulated time is larger than the overcharge detection delay time, the device would enter “overcharge status”.
4. After overcharge protection, the overcharge protection status would not be released if the voltage of any battery cell is higher than the overcharge release voltage in the overcharge release delay time even though the voltage of all other batteries are equal to or lower than the overcharge release voltage.
5. The output type of COUT pin is active high CMOS. The output voltage is between VSS and the output the voltage of internal regulator.

11.2 Test Time Shortening Capability

Applying a voltage of 4.5V ± 0.2V between VDD and VC1 can shorten the overcharge detection delay time into approximately 1/250

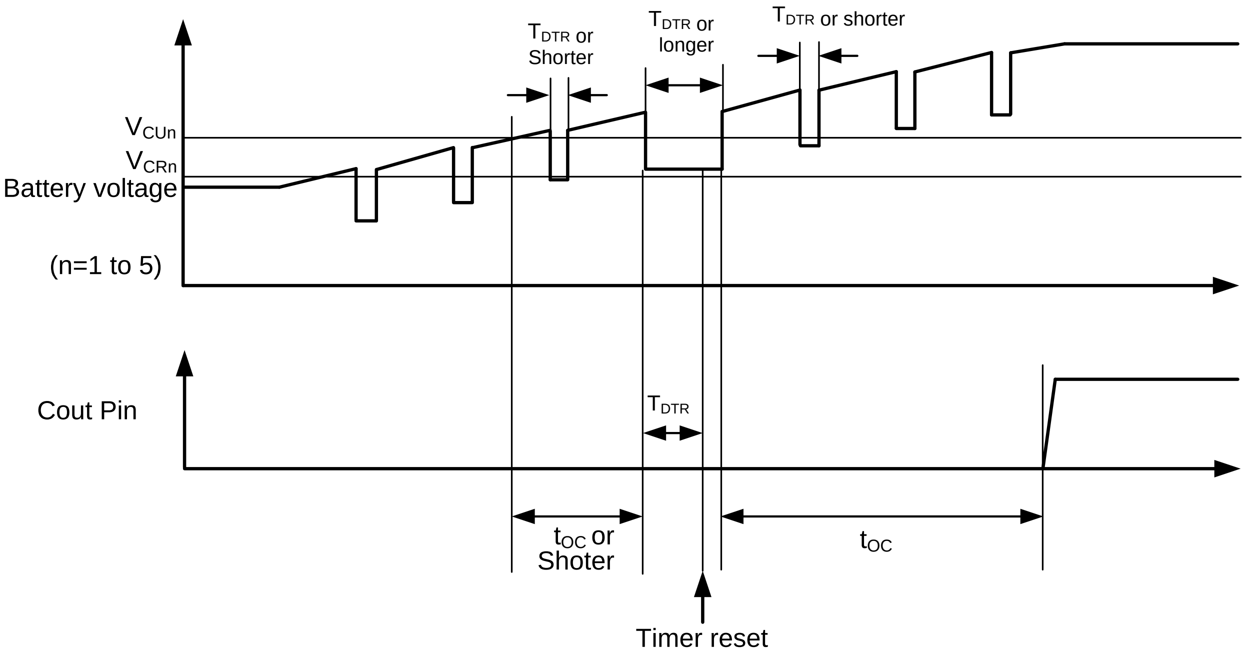
12. Timing Diagram

12.1 Overcharge Detection



Description: (1) Normal operating status, (2) Overcharge Status

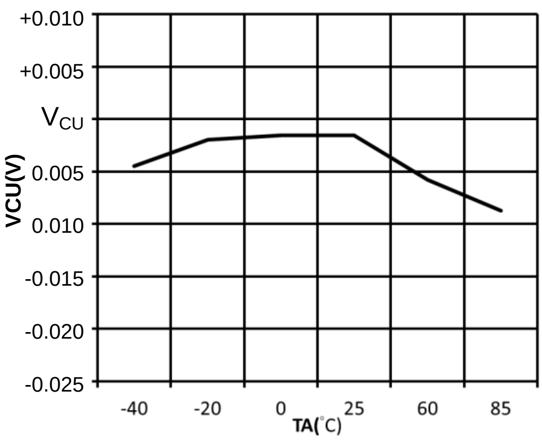
12.2 Reset Delay Time of Overcharge Detection Counter



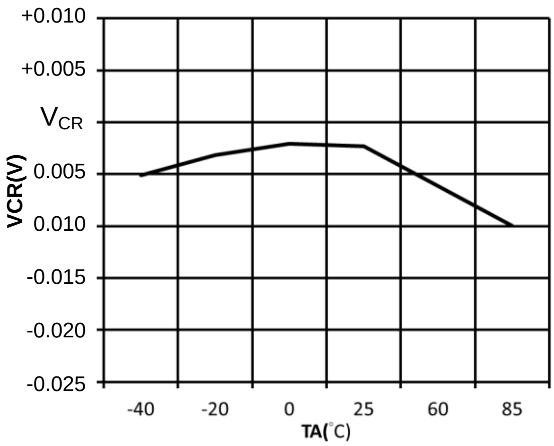
13. Characteristics (Typical Value)

13.1 Detection voltage.

(1) V_{CU} vs. Ta

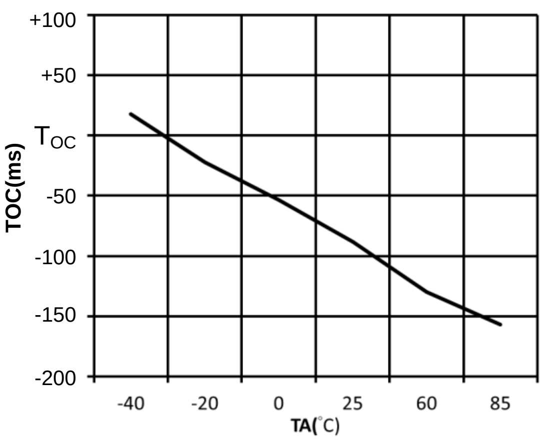


(2) V_{CR} vs. Ta

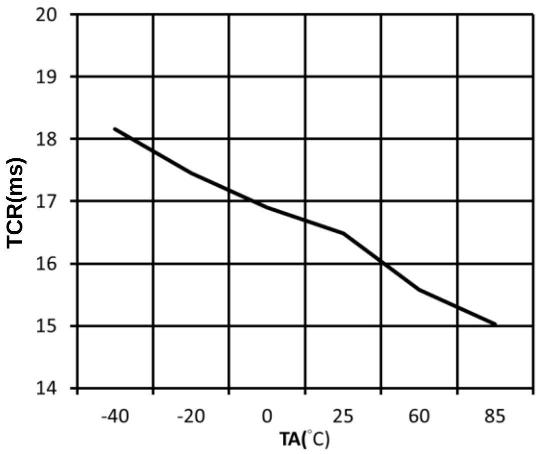


13.2 Delay time.

(3) T_{OC} vs. Ta

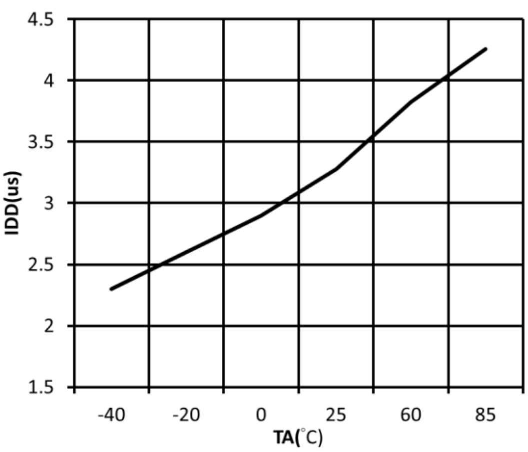


(4) T_{CR} vs. Ta

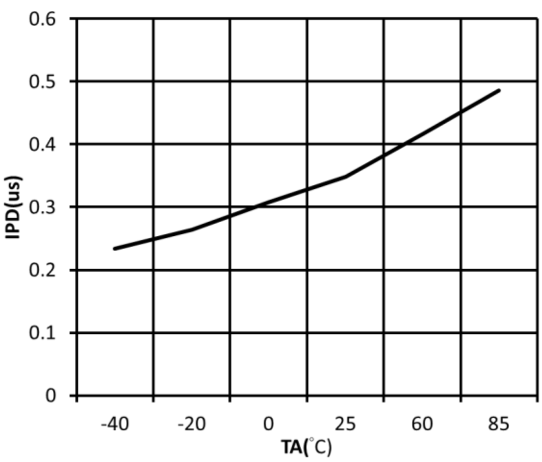


13.3 Current Consumption.

(5) I_{DD} vs. Ta



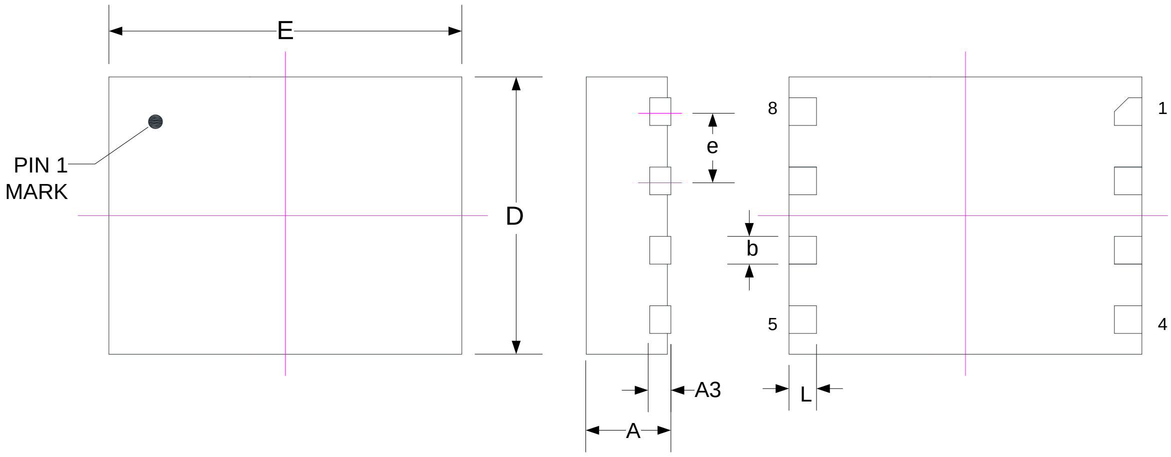
(6) I_{PD} vs. Ta



14. Package Information

14.1 DFN-1.97*2.46-8L Package

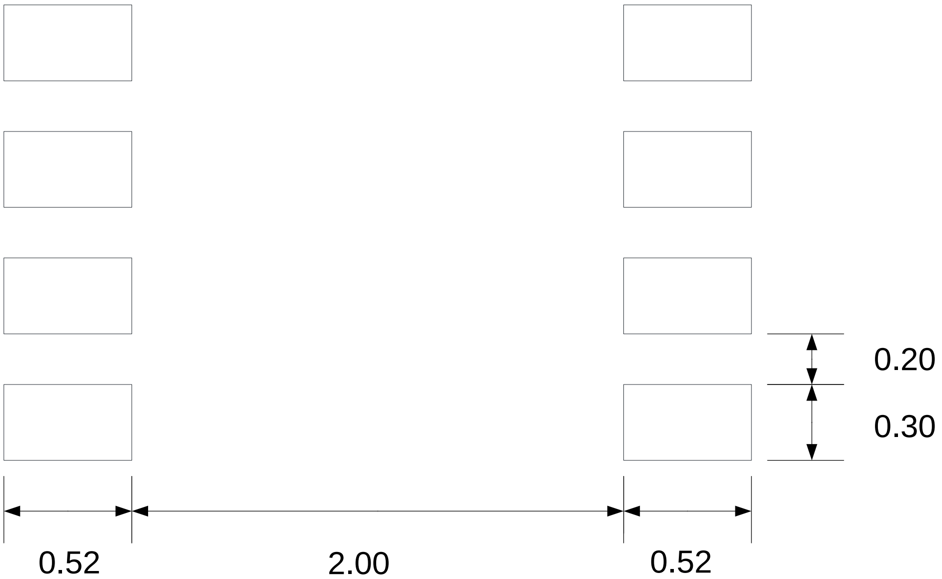
Note: All dimensions are in millimeters.



SYMBOLS	MIN	NOM	MAX
A	0.40	0.45	0.50
A3	0.127 REF.		
b	0.15	0.20	0.25
D	1.92	1.97	2.20
E	2.41	2.46	2.51
L	0.15	0.20	0.25
e	0.50 BSC		

15. Land Pattern Design Recommendations

15.1 DFN-1.97*2.46-8L Package

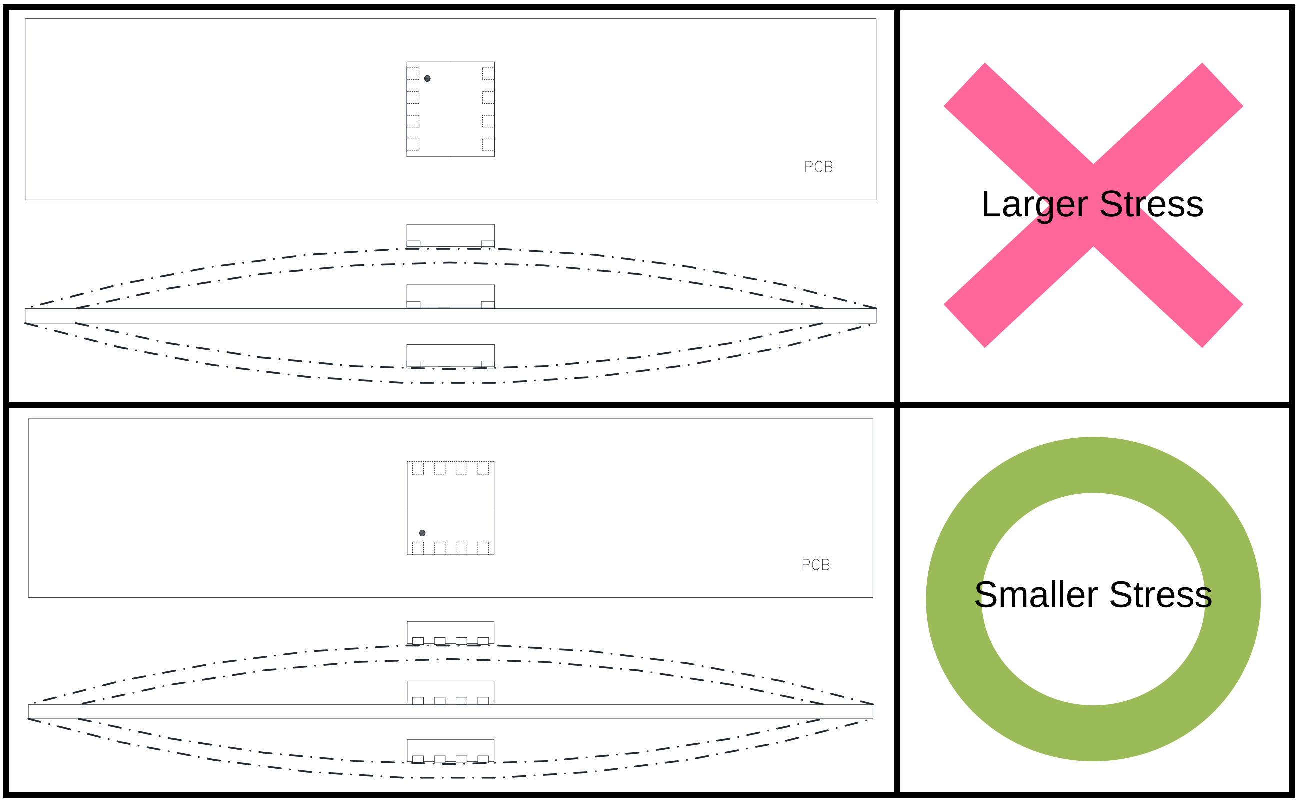


Note:

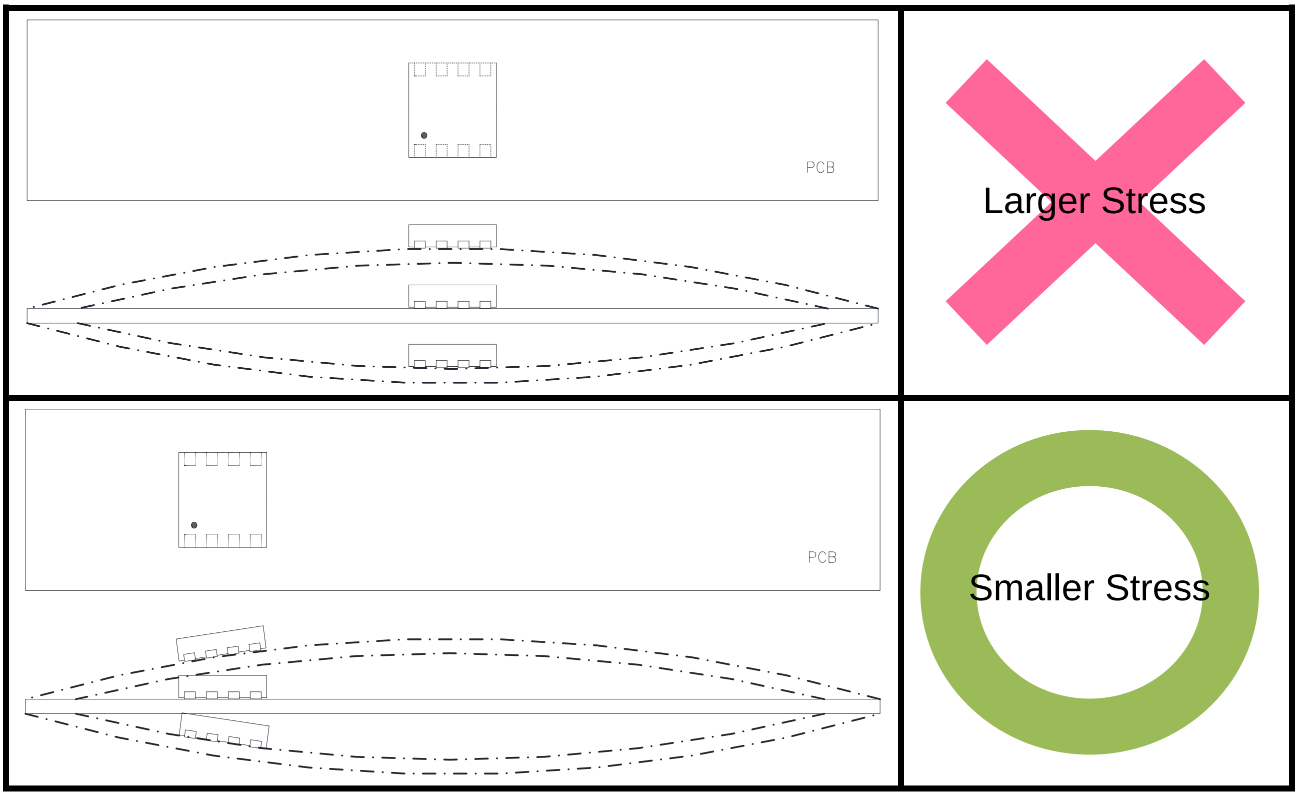
1. Publication IPC-7351 is recommended for alternate designs
2. Unit : mm
3. http://www.hycontek.com/attachments/MSP/OJTI-HM-2013-002.pdf

16. IC Placement Recommendations

16.1 IC Orientation For Surface Mount



16.2 IC Position For Surface Mount

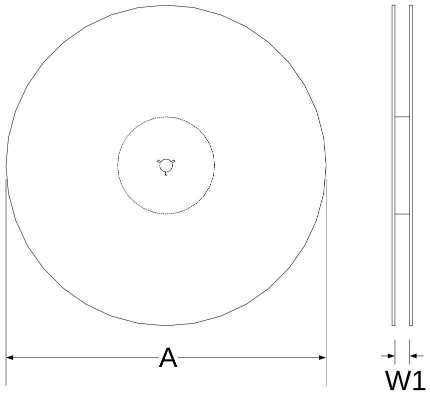


17. Tape & Reel Information

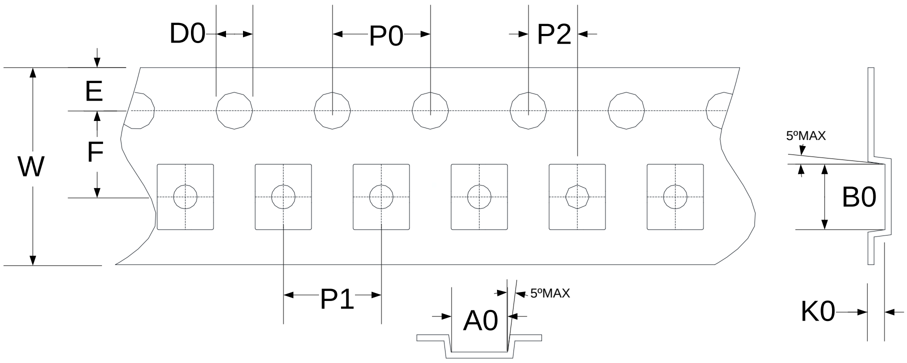
17.1 Tape & Reel Information---DFN-1.97*2.46-8L

Unit: mm

17.1.1 Reel Dimensions



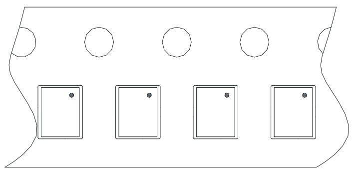
17.1.2 Carrier Tape Dimensions



SYMBOLS	Reel Dimensions		Carrier Tape Dimensions									
	A	W1	A0	B0	K0	P0	P1	P2	E	F	D0	W
Spec.	178	9.4	2.31	2.66	0.65	4.00	4.00	2.00	1.75	3.50	1.55	8.00
Tolerance	±2.00	±1.50	±0.10	±0.10	±0.10	±0.10	±0.10	±0.05	±0.10	±0.05	±0.05	±0.20

Note: 10 Sprocket hole pitch cumulative tolerance is ±0.20mm.

17.1.3 Pin1 direction



18. Revision Record

The larger modifications of this document are described below, but changes of punctuation marks and fonts are not within the scope of description.

Ver.	Page	Summary of Modification
V01	-	First release.
V02	P5,P7,P8,	Update DFN-1.97*2.46-8L Package information
	P23,P25	Delete TMSOP-8 Package information
	P5	Update Output logic active high maximum time