HY17P68

Datasheet

6000 Counts DMM Specialized IC
Embedded Digital RMS

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注意：

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4、 請注意輸入電壓、輸出電壓、負載電流的使用條件，使 IC 內的功耗不超過封裝的容許功耗。對於客戶在超出說明書中規定額定值使用產品，即使是瞬間的使用，由此所造成的損失，本公司不承擔任何責任。

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7、 本公司一直致力於提高產品的品質和可靠度，但所有的半導體產品都有一定的失效概率，這些失效概率可能會導致一些人身事故、火災事故等。當設計產品時，請充分留意冗餘設計並採用安全指標，這樣可以避免事故的發生。

8、 本規格書中內容，未經本公司許可，嚴禁用於其他目的之轉載或複製。

1. Features

- 8 位元加強型精簡指令集，共有 71 個指令包含硬體乘法指令及查表指令 H08D，支援 C Compiler 編譯環境
- 數位電源工作電壓範圍 2.2V to 5.5V，類比電源工作電壓 2.4V to 4.5V，-40~85℃ 工作溫度範圍
- 16kWord OTP (One Time Programmable) 程式記憶體，1024Byte 資料記憶體
- 高解析度 ΣΔADC
  - 最高取樣頻率達 1MHz
  - 超取樣頻率設置 32~61440
  - 二/三階梳狀濾波器，轉換頻率 30.72ksps
  - 信號放大 x1/2, x1,x2,x4,x8
  - 零輸入電壓，零輸出電壓
  - 高輸入阻抗 (內置輸入緩衝器)
  - 內置絕對溫度感測器
- 內建數位訊號處理(DSP)實現數位 AC 有效值、Peak Hold 等數位計算功能
- 可程式化多功能網路
  - 電壓/電阻/電容換檔量測
  - 定電壓/定電流輸出
  - 元件可自我校正
  - 元件正負極性判別
- 窗型比較器
  - 具有遲滯與 latch 功能，可降低 glitch
  - 可程式化設定比較電壓
  - 可做為短路測試量測、頻率量測或電容充放電頻率量測
- 多功能比較器
  - 可實現 LVD 低電壓檢測功能具多段檢測電壓設置與外部輸入電壓檢測功能
  - 具有遲滯與 latch 功能，可降低 glitch
- 運算放大器
  - 搭配外部元件可將小訊號放大
  - 可程式化成緩衝器
- 類比電壓源 VDDA 具 10mA 穩壓電壓源輸出，快速啟動功能
- 1.2V 的內部類比電路共地電壓源
- 4x36 LCD 液晶驅動器
  - 1/4 Duty、1/3 Bias
  - 內建 Charge Pump 穩壓線路，可提供多種 LCD 偏壓
  - LCD 埠可設定數位輸入輸出埠
- 3 組 24 bits 可程式化計數器可同時量測頻率, 週期與占空比
- 8-bit Timer A1
- 16-bit Timer B 模組具 PWM 功能
- UART、SPI、I^2C(Master/Slave)模組
- Built-In EPROM (BIE)，內建 2.75V 低壓燒錄控制電路
- 內建 Brownout 與 Watch dog timer，可防止 CPU 進入死機模式
- 支援外部石英震盪器 1MHz~16MHz /32768Hz 及內部高精度 RC 震盪器 4.9152MHz/9.8304MHz Mode 多種 CPU 工作時脈切換選擇，可讓使用者達到最佳省電規劃
  - 運行模式
  - 待機模式: LPO 14.5kHz
  - 休眠模式
- Support 8 stack level.
- 封裝
  - LQFP64、LQFP100

2. 引腳定義

2.1. LQFP100 引腳圖

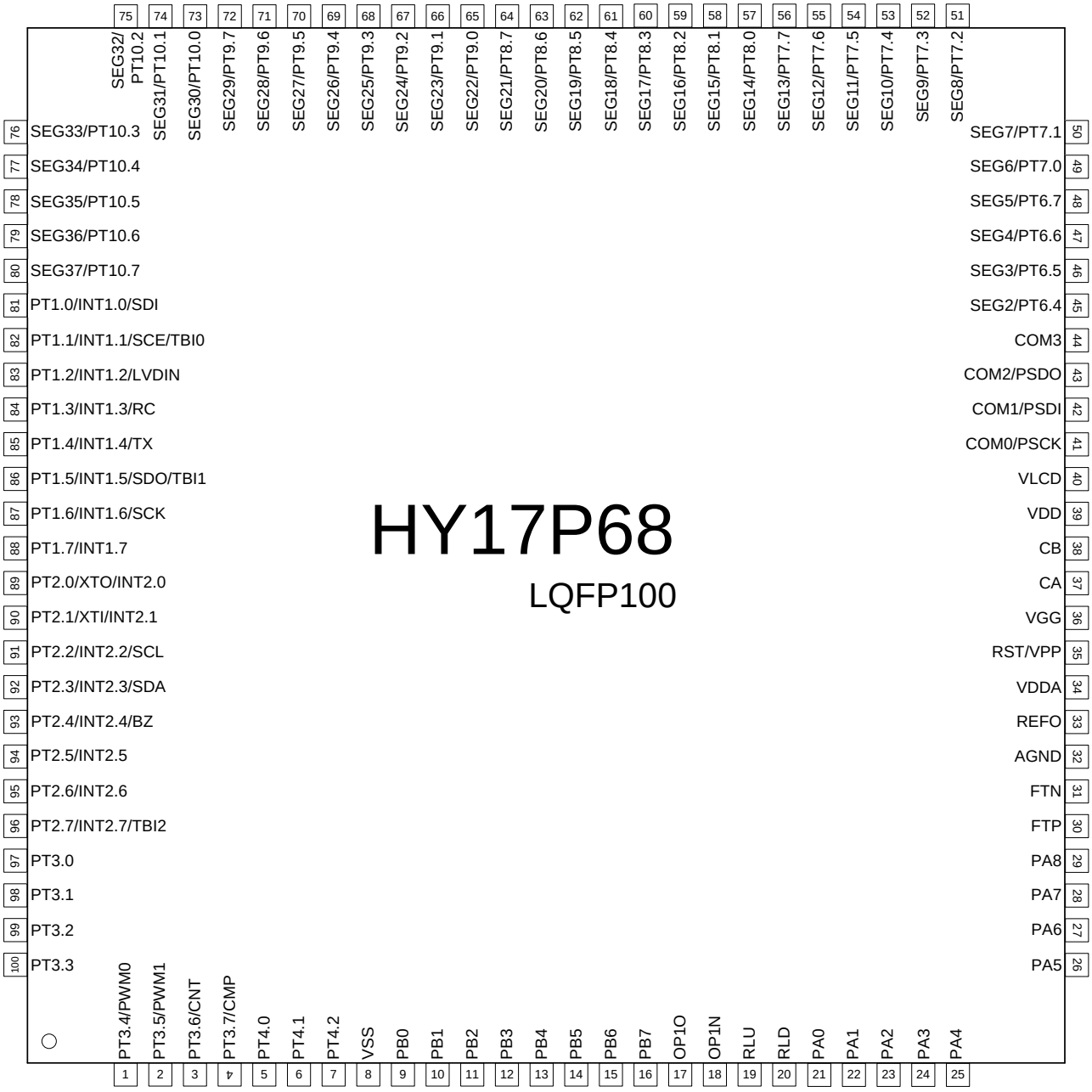


圖 2-1 HY17P68 LQFP100 引腳圖

註 1：VPP 與 RST 復用同一接口，非燒錄 EPROM 時禁止輸入電壓超過 8.5V

2.2. LQFP64 引腳圖

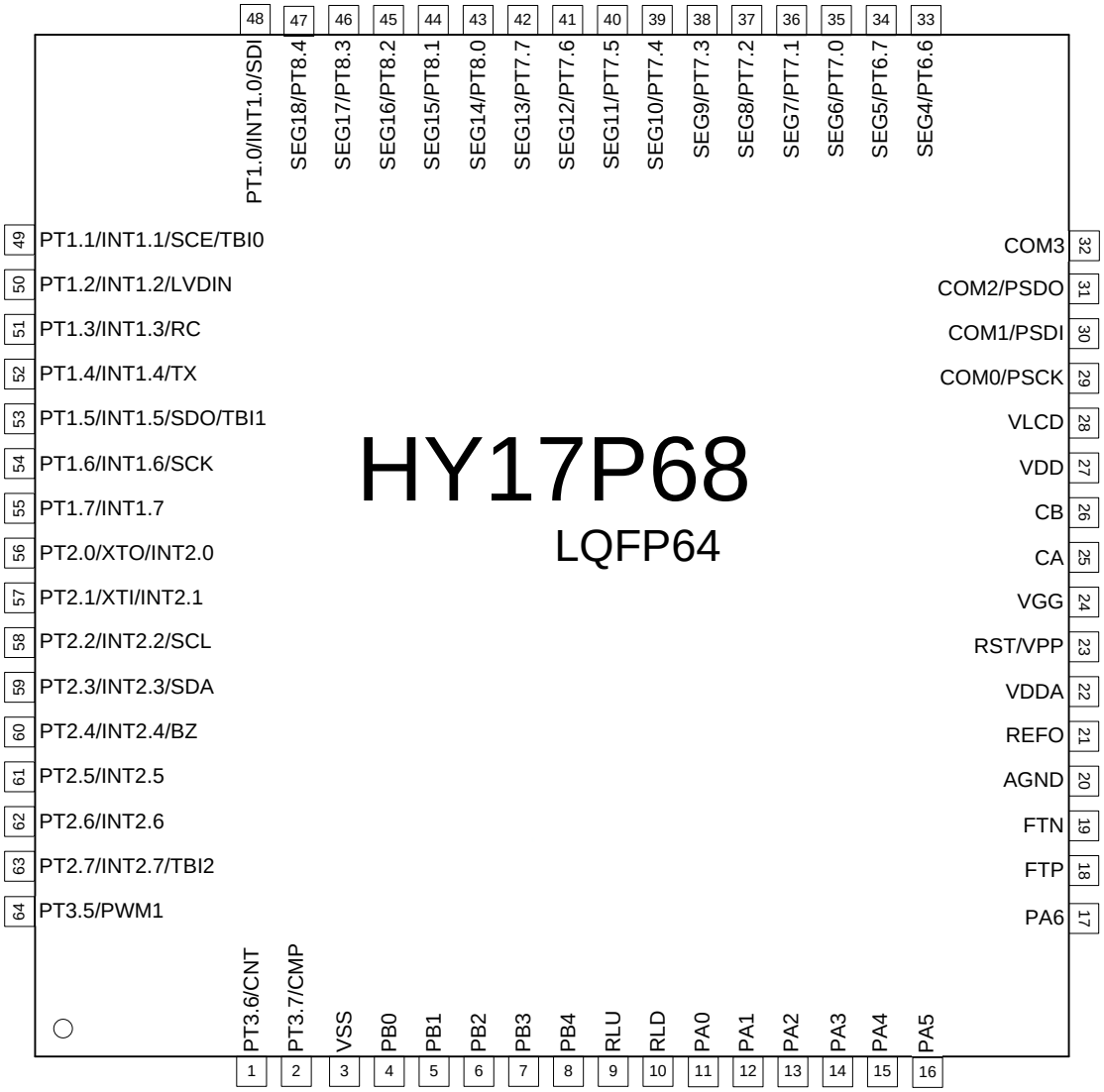


圖 2-2 HY17P68 LQFP64 引腳圖

註 1：VPP 與 RST 復用同一接口，非燒錄 EPROM 時禁止輸入電壓超過 8.5V

2.3. 引腳定義與說明

"I/O"輸入/輸出,"I"輸入,"O"輸出,"S"史密斯觸發,"C"CMOS 特性兼容輸出與輸入,"P"電壓源,"A"類比通道

引腳編號		引腳名稱	引腳特性		功能說明
LQFP100	LQFP64		格式	緩衝	
1	-	PT3.4/PWM0 PT3.4 PWM0	I/O O	S/C C	數位輸入/輸出 PWM0 輸出接口
2	64	PT3.5/PWM1 PT3.5 PWM1	I/O O	S/C C	數位輸入/輸出 PWM1 輸出接口
3	1	PT3.6/CNT PT3.6 CNT	I/O I	S/C S	數位輸入/輸出 頻率計數輸入接口
4	2	PT3.7/CMP PT3.7 CMP	I/O O	S/C S	數位輸入/輸出 比較器輸出接口
5	-	PT4.0	I	S/C	數位輸入/輸出
6	-	PT4.1	I	S/C	數位輸入/輸出
7	-	PT4.2	I	S/C	數位輸入/輸出
8	3	VSS	P	P	晶片工作電壓源接地端
9	4	PB0	I	A	類比輸入通道
10	5	PB1	I	A	類比輸入通道
11	6	PB2	I	A	類比輸入通道
12	7	PB3	I	A	類比輸入通道
13	8	PB4	I	A	類比輸入通道
14	-	PB5	I	A	類比輸入通道
15	-	PB6	I	A	類比輸入通道
16	-	PB7	I	A	類比輸入通道
17	-	OP1O	O	A	OPAMP(OP1) output terminal
18	-	OP1N	I	A	OPAMP(OP1) negative input terminal
19	9	RLU	I/O	A	類比網路開關接口
20	10	RLD	I/O	A	類比網路開關接口
21	11	PA0	I/O	A	類比網路開關接口
22	12	PA1	I/O	A	類比網路開關接口
23	13	PA2	I/O	A	類比網路開關接口
24	14	PA3	I/O	A	類比網路開關接口

引腳編號		引腳名稱	引腳特性		功能說明
LQFP100	LQFP64		格式	緩衝	
25	15	PA4	I/O	A	類比網路開關接口
26	16	PA5	I/O	A	類比網路開關接口
27	17	PA6	I/O	A	類比網路開關接口
28	-	PA7	I/O	A	類比網路開關接口
29	-	PA8	I/O	A	類比網路開關接口
30	18	FTP	I/O	A	前置濾波電容連接口
31	19	FTN	I/O	A	前置濾波電容連接口
32	20	AGND	P	P	類比電源接地端(source: VDDA)
33	21	REFO	P	P	類比電路基準電壓源(source: VDDA)
34	22	VDDA	P	P	穩壓器輸出，類比電路電壓源 (source: VDD)
35	23	RST/VPP RST VPP	 I P	 S P	 重置晶片 OTP 讀/寫時的電壓源
36	24	VGG	P	P	倍壓穩壓電源輸出，10uF need. (Source: VDD)
37	25	CA	A	A	倍壓電容接口，1~10uF to CB Pin.
38	26	CB	A	A	倍壓電容接口
39	27	VDD	P	P	晶片工作電壓源，1~10uF need.
40	28	VLCD	P	P	LCD 的電壓源，1~10uF need. (Source: VDD)
41	29	COM0/PSCK COM0 PSCK	 O I	 A S	 LCD Segment 輸出 OTP 讀/寫介面接口
42	30	COM1/PSDI COM1 PSDI	 O I	 A S	 LCD Segment 輸出 OTP 讀/寫介面接口
43	31	COM2/PSDO COM2 PSDO	 O O	 A S	 LCD Segment 輸出 OTP 讀/寫介面接口
44	32	COM3 COM3	 O	 A	 LCD Segment 輸出
45	-	SEG2/PT6.4 SEG2 PT6.4	 O I/O	 A S/C	 LCD Segment 輸出 數位輸入/輸出

引腳編號		引腳名稱	引腳特性		功能說明
LQFP100	LQFP64		格式	緩衝	
46	-	SEG3/PT6.5 SEG3 PT6.5	 O I/O	 A S/C	 LCD Segment 輸出 數位輸入/輸出
47	33	SEG4/PT6.6 SEG4 PT6.6	 O I/O	 A S/C	 LCD Segment 輸出 數位輸入/輸出
48	34	SEG5/PT6.7 SEG5 PT6.7	 O I/O	 A S/C	 LCD Segment 輸出 數位輸入/輸出
49	35	SEG6/PT7.0 SEG6 PT7.0	 O I/O	 A S/C	 LCD Segment 輸出 數位輸入/輸出
50	36	SEG7/PT7.1 SEG7 PT7.1	 O I/O	 A S/C	 LCD Segment 輸出 數位輸入/輸出
51	37	SEG8/PT7.2 SEG8 PT7.2	 O I/O	 A S/C	 LCD Segment 輸出 數位輸入/輸出
52	38	SEG9/PT7.3 SEG9 PT7.3	 O I/O	 A S/C	 LCD Segment 輸出 數位輸入/輸出
53	39	SEG10/PT7.4 SEG10 PT7.4	 O I/O	 A S/C	 LCD Segment 輸出 數位輸入/輸出
54	40	SEG11/PT7.5 SEG11 PT7.5	 O I/O	 A S/C	 LCD Segment 輸出 數位輸入/輸出
55	41	SEG12/PT7.6 SEG12 PT7.6	 O I/O	 A S/C	 LCD Segment 輸出 數位輸入/輸出
56	42	SEG13/PT7.7 SEG13 PT7.7	 O I/O	 A S/C	 LCD Segment 輸出 數位輸入/輸出
57	43	SEG14/PT8.0 SEG14 PT8.0	 O I/O	 A S/C	 LCD Segment 輸出 數位輸入/輸出

引腳編號		引腳名稱	引腳特性		功能說明
LQFP100	LQFP64		格式	緩衝	
58	44	SEG15/PT8.1 SEG15 PT8.1	O I/O	A S/C	LCD Segment 輸出 數位輸入/輸出
59	45	SEG16/PT8.2 SEG16 PT8.2	O I/O	A S/C	LCD Segment 輸出 數位輸入/輸出
60	46	SEG17/PT8.3 SEG17 PT8.3	O I/O	A S/C	LCD Segment 輸出 數位輸入/輸出
61	47	SEG18/PT8.4 SEG18 PT8.4	O I/O	A S/C	LCD Segment 輸出 數位輸入/輸出
62	-	SEG19/PT8.5 SEG19 PT8.5	O I/O	A S/C	LCD Segment 輸出 數位輸入/輸出
63	-	SEG20/PT8.6 SEG20 PT8.6	O I/O	A S/C	LCD Segment 輸出 數位輸入/輸出
64	-	SEG21/PT8.7 SEG21 PT8.7	O I/O	A S/C	LCD Segment 輸出 數位輸入/輸出
65	-	SEG22/PT9.0 SEG22 PT9.0	O I/O	A S/C	LCD Segment 輸出 數位輸入/輸出
66	-	SEG23/PT9.1 SEG23 PT9.1	O I/O	A S/C	LCD Segment 輸出 數位輸入/輸出
67	-	SEG24/PT9.2 SEG24 PT9.2	O I/O	A S/C	LCD Segment 輸出 數位輸入/輸出
68	-	SEG25/PT9.3 SEG25 PT9.3	O I/O	A S/C	LCD Segment 輸出 數位輸入/輸出
69	-	SEG26/PT9.4 SEG26 PT9.4	O I/O	A S/C	LCD Segment 輸出 數位輸入/輸出

引腳編號		引腳名稱	引腳特性		功能說明
LQFP100	LQFP64		格式	緩衝	
70	-	SEG27/PT9.5 SEG27 PT9.5	 O I/O	 A S/C	 LCD Segment 輸出 數位輸入/輸出
71	-	SEG28/PT9.6 SEG28 PT9.6	 O I/O	 A S/C	 LCD Segment 輸出 數位輸入/輸出
72	-	SEG29/PT9.7 SEG29 PT9.7	 O I/O	 A S/C	 LCD Segment 輸出 數位輸入/輸出
73	-	SEG30/PT10.0 SEG30 PT10.0	 O I/O	 A S/C	 LCD Segment 輸出 數位輸入/輸出
74	-	SEG31/PT10.1 SEG31 PT10.1	 O I/O	 A S/C	 LCD Segment 輸出 數位輸入/輸出
75	-	SEG32/PT10.2 SEG32 PT10.2	 O I/O	 A S/C	 LCD Segment 輸出 數位輸入/輸出
76	-	SEG33/PT10.3 SEG33 PT10.3	 O I/O	 A S/C	 LCD Segment 輸出 數位輸入/輸出
77	-	SEG34/PT10.4 SEG34 PT10.4	 O I/O	 A S/C	 LCD Segment 輸出 數位輸入/輸出
78	-	SEG35/PT10.5 SEG35 PT10.5	 O I/O	 A S/C	 LCD Segment 輸出 數位輸入/輸出
79	-	SEG36/PT10.6 SEG36 PT10.6	 O I/O	 A S/C	 LCD Segment 輸出 數位輸入/輸出
80	-	SEG37/PT10.7 SEG37 PT10.7	 O I/O	 A S/C	 LCD Segment 輸出 數位輸入/輸出

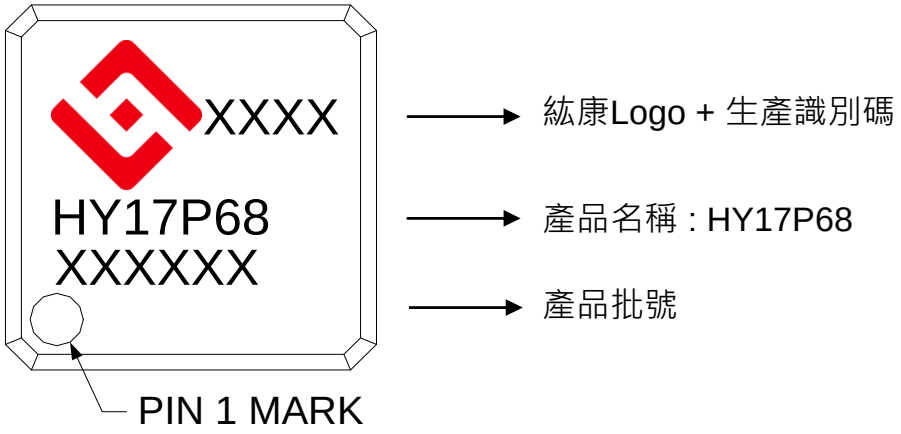
引腳編號		引腳名稱	引腳特性		功能說明
LQFP100	LQFP64		格式	緩衝	
81	48	PT1.0/INT1.0/SDI			
		PT1.0	I/O	S/C	數位輸入/輸出
		INT1.0	I	S	中斷源 E0IF
		SDI	I/O	S	SPI 通訊介面接口
82	49	PT1.1/INT1.1/SCE/TBI0			
		PT1.1	I/O	S/C	數位輸入/輸出
		INT1.1	I	S	中斷源 E1IF
		SCE	I	S	SPI 通訊介面接口
		TBI0	I	S	TimerB 啟動輸入接口
83	50	PT1.2/INT1.2/LVDIN			
		PT1.2	I/O	S/C	數位輸入/輸出
		INT1.2	I	S	中斷源 E2IF
		LVDIN	A	A	LVD 外部信號輸入接口
84	51	PT1.3/INT1.3/RC			
		PT1.3	I/O	S/C	數位輸入/輸出
		INT1.3	I	S	中斷源 E3IF
		RC	I	S	EUART 通訊介面接口
85	52	PT1.4/INT1.4/TX			
		PT1.4	I/O	S/C	數位輸入/輸出
		INT1.4	I	S	中斷源 INTF1.4
		TX	O	C	EUART 通訊介面接口
86	53	PT1.5/INT1.5/SDO/TBI1			
		PT1.5	I/O	S/C	數位輸入/輸出
		INT1.5	I	S	中斷源 INTF1.5
		SDO	I/O	S	SPI 通訊介面接口
		TBI1	I	S	TimerB 啟動輸入接口
87	54	PT1.6/INT1.6/SCK			
		PT1.6	I/O	S/C	數位輸入/輸出
		INT1.6	I	S	中斷源 INTF1.6
		SCK	I/O	S	SPI 通訊介面接口
88	55	PT1.7/INT1.7			
		PT1.7	I/O	S/C	數位輸入/輸出
		INT1.7	I	S	中斷源 INTF1.7

引腳編號		引腳名稱	引腳特性		功能說明
LQFP100	LQFP64		格式	緩衝	
89	56	PT2.0/XTO/INT2.0			
		PT2.0	I/O	S/C	數位輸入/輸出
		XTO	A	A	外接振盪器輸出端
		INT2.0	I	S	中斷源 INTF2.0
90	57	PT2.1/XTI/INT2.1			
		PT2.1	I/O	S/C	數位輸入/輸出
		XTI	A	A	外接振盪器輸入端
		INT2.1	I	S	中斷源 INTF2.1
91	58	PT2.2/INT2.2/SCL			
		PT2.2	I/O	S/C	數位輸入/輸出
		INT2.2	I	S	中斷源 INTF2.2
		SCL	I/O	S	I2C 通訊介面引腳
92	59	PT2.3/INT2.3/SDA			
		PT2.3	I/O	S/C	數位輸入/輸出
		INT2.3	I	S	中斷源 INTF2.3
		SDA	I/O	S	I2C 通訊介面引腳
93	60	PT2.4/INT2.4/BZ			
		PT2.4	I/O	S/C	數位輸入/輸出
		INT2.4	I	S	中斷源 INTF2.4
		BZ	O	C	蜂鳴器輸出端
94	61	PT2.5/INT2.5			
		PT2.5	I/O	S/C	數位輸入/輸出
		INT2.5	I	S	中斷源 INTF2.5
95	62	PT2.6/INT2.6			
		PT2.6	I/O	S/C	數位輸入/輸出
		INT2.6	I	S	中斷源 INTF2.6
96	63	PT2.7/INT2.7/TBI2			
		PT2.7	I/O	S/C	數位輸入/輸出
		INT2.7	I	S	中斷源 INTF2.7
		TBI2	I	S	TimerB 啟動輸入接口
97	-	PT3.0	I/O	S/C	數位輸入/輸出
98	-	PT3.1	I/O	S/C	數位輸入/輸出
99	-	PT3.2	I/O	S/C	數位輸入/輸出
100	-	PT3.3	I/O	S/C	數位輸入/輸出

表 2-1 引腳編號與說明

2.4. 封裝片標記信息

2.4.1. LQFP 封裝片標記信息



3. 應用電路

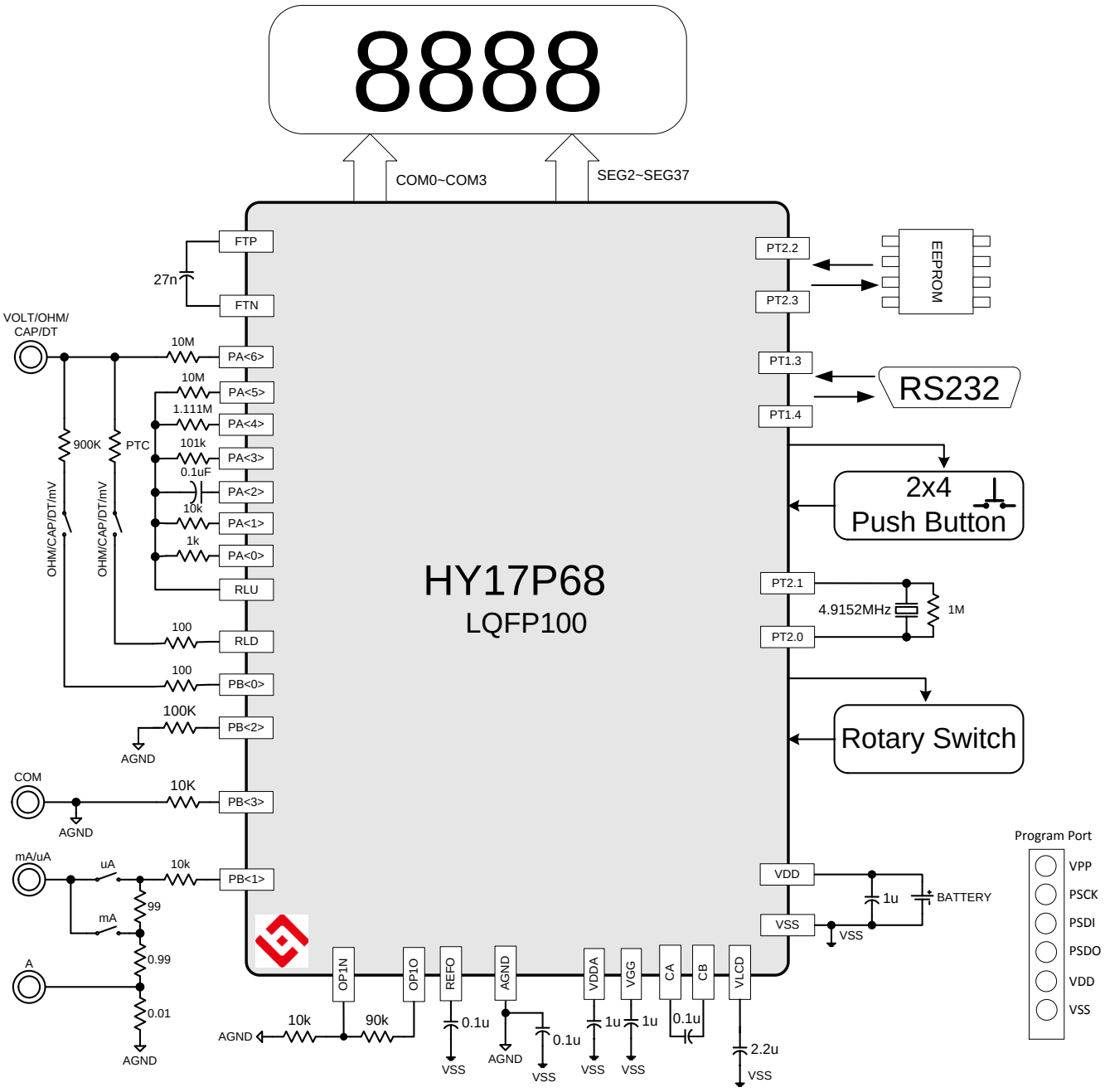


圖 3-1 DMM 應用電路

4. Function Outline

4.1. Internal Block Diagram

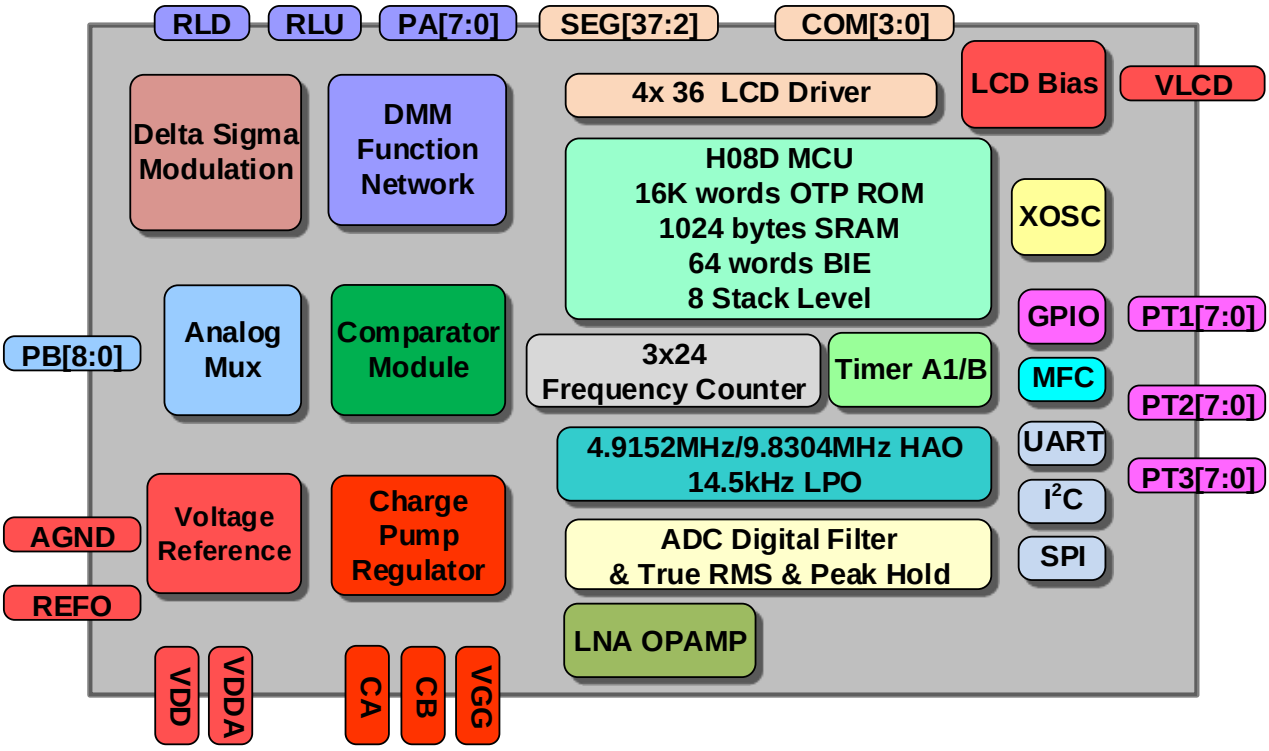


圖 4-1 HY17P68 內部方塊圖

4.2. 相關說明與支援文件

晶片功能相關使用說明書

DS-HY17P68	HY17P68 說明書
UG-HY17S68	HY17S68 使用說明書
APD-CORE005	H08D 指令集說明書

開發工具相關使用說明書

APD-HY17PIDE001	HY17P 系列開發工具軟體使用說明書
APD-HY17PIDE005	HY17P6x 系列開發工具硬體使用說明書
APD-HYIDE013	整合型燒錄器使用說明書
APD-HYIDE014	HY10000-WK08C 整合型燒錄器線上更新說明書
APD-OTP005	OTP 燒錄引腳資訊

產品生產相關使用說明書

APD-HY17PIDE004	HY17P 系列 HexLoader 說明書

4.3. ADC Network

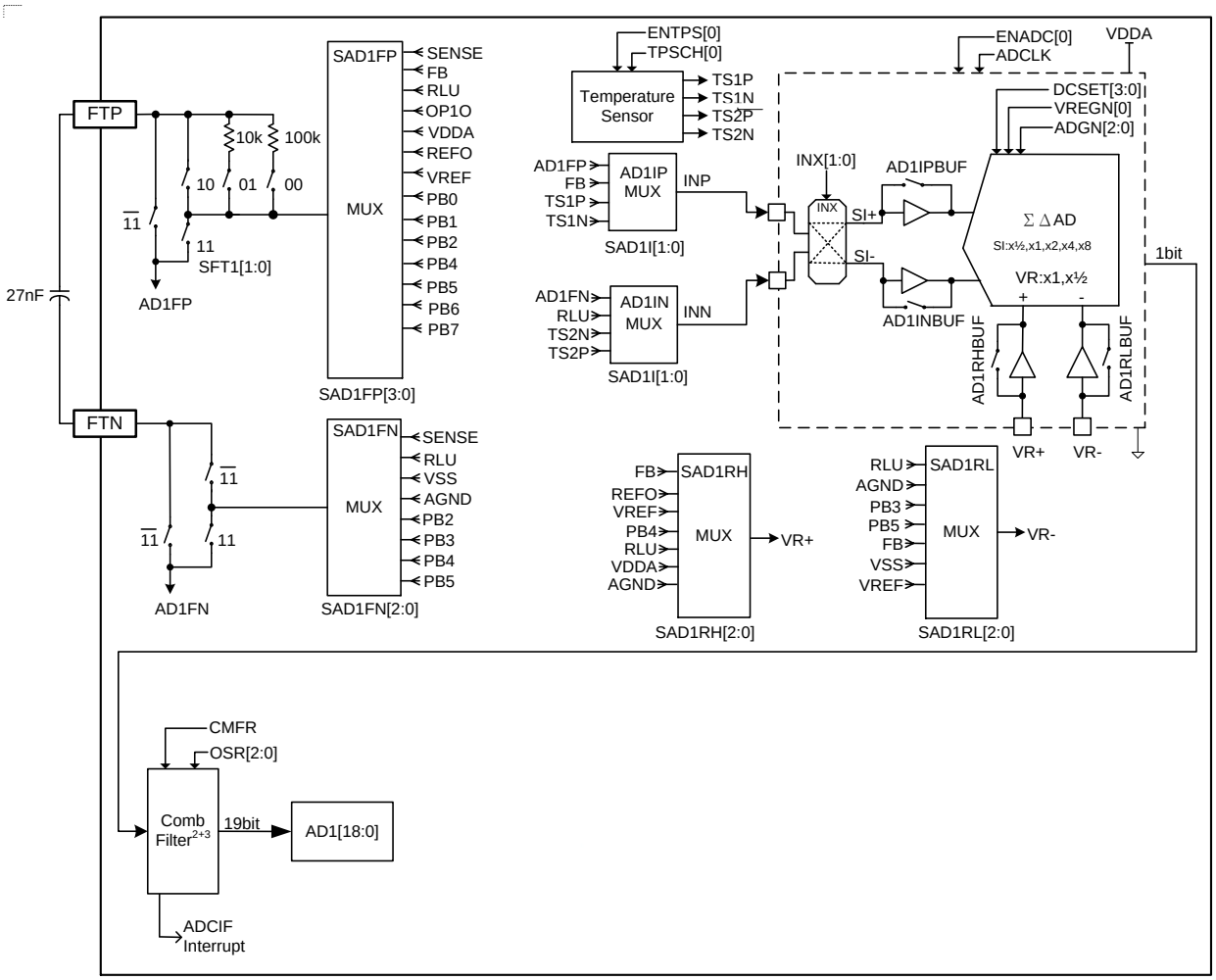


圖 4-2 ΣΔADC Network 方塊圖

4.4. Digital Signal Processing(DSP)

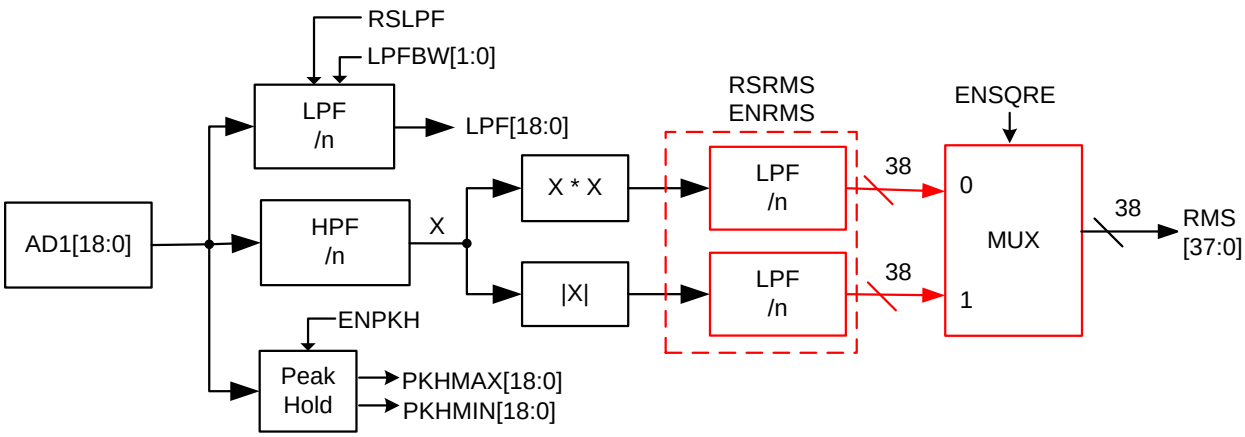


圖 4-3 Digital Signal Processing(DSP) 方塊圖

4.5. Analog Input Network

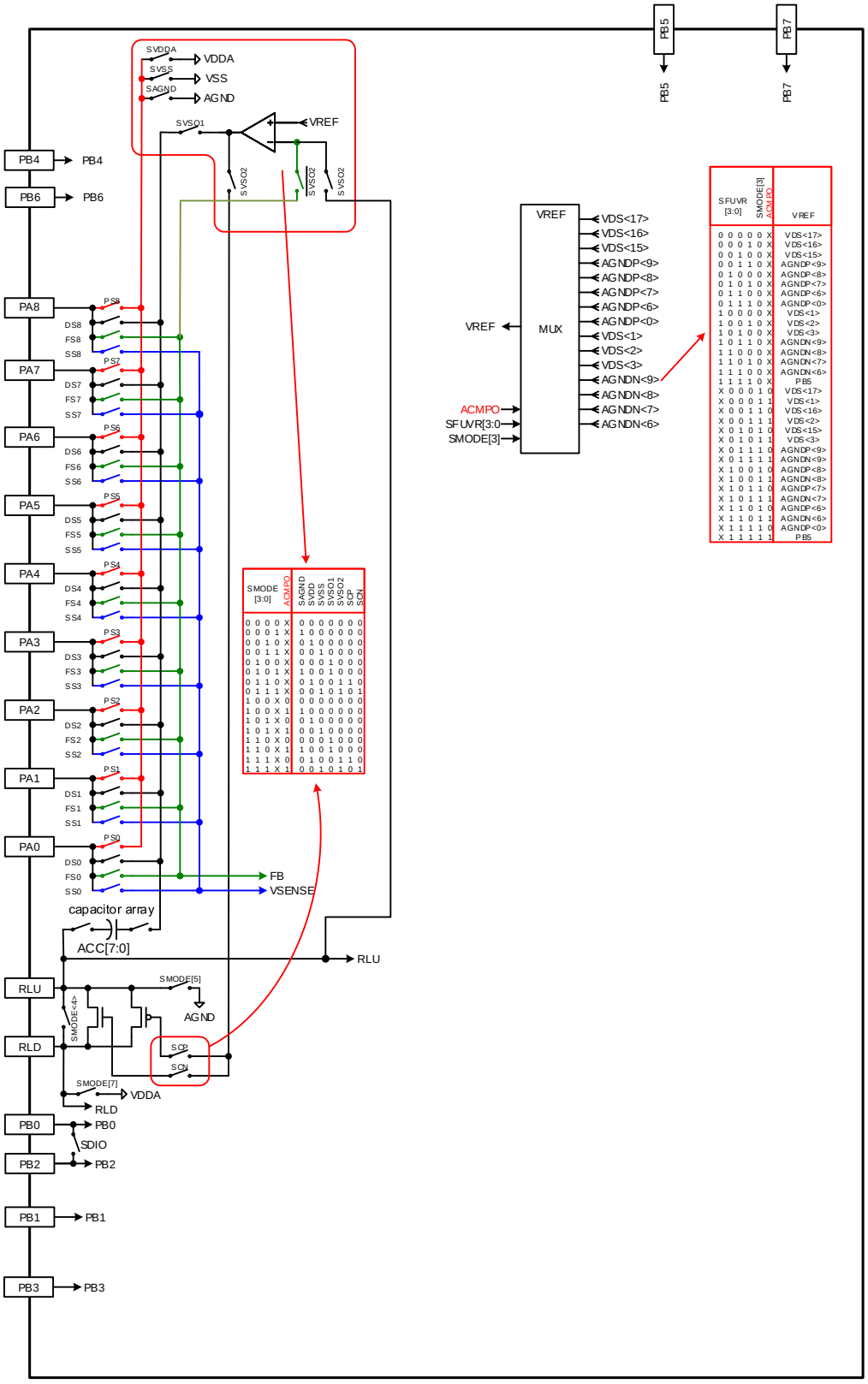


圖 4-4 Analog Input Network 方塊圖

4.6. Clock System

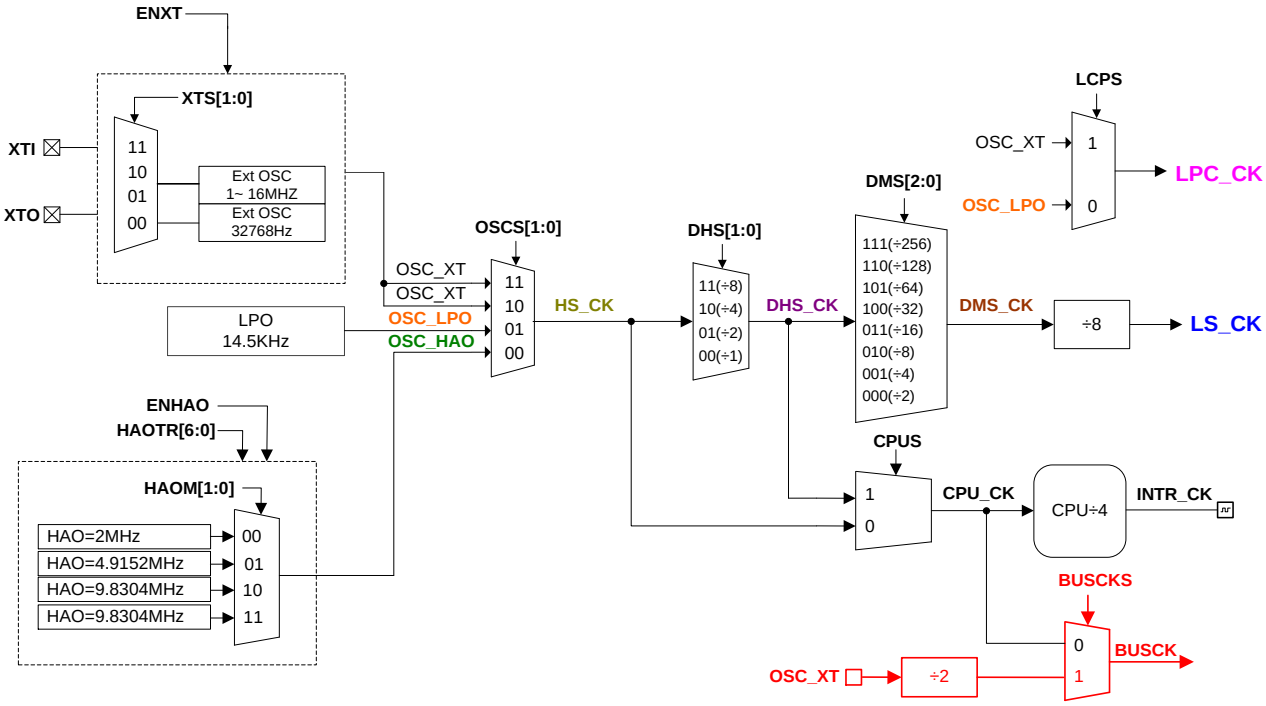


圖 4-5 Clock System 方塊圖(一)

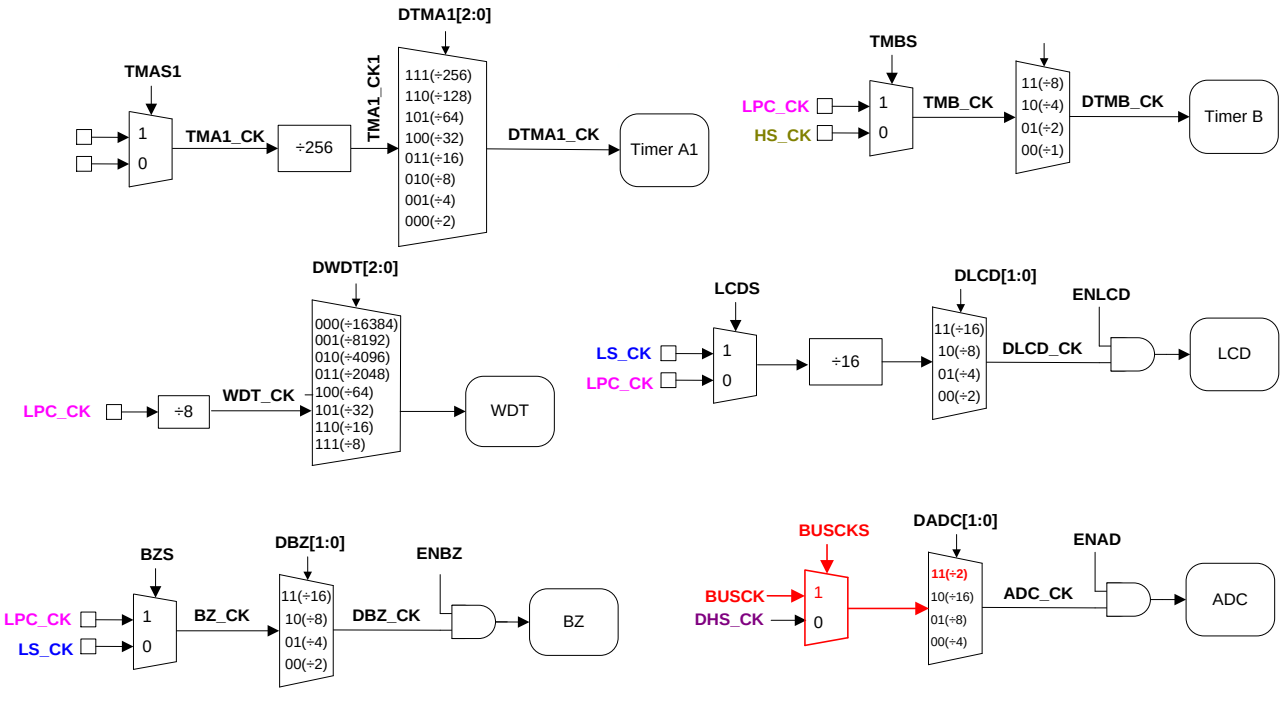
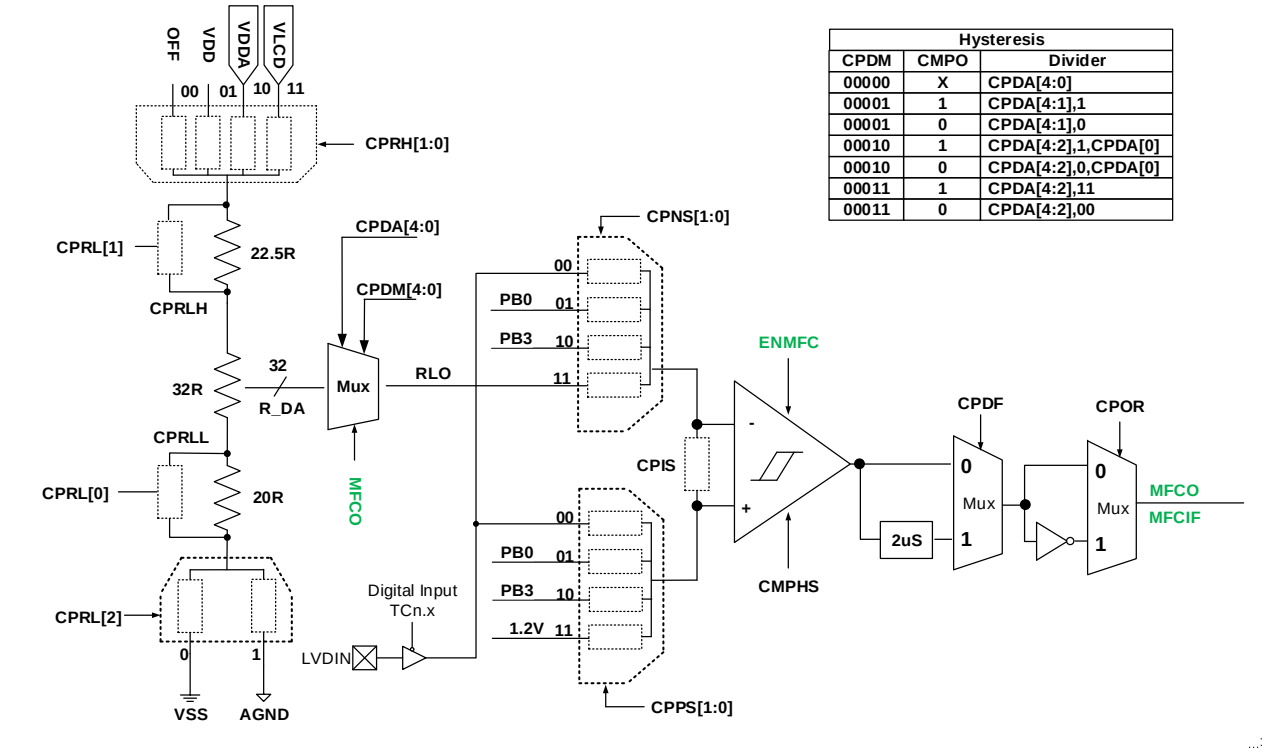


圖 4-6 Clock System 方塊圖(二)

4.7. Multi-function Comparator



Hysteresis		
CPDM	CMPO	Divider
00000	X	CPDA[4:0]
00001	1	CPDA[4:1],1
00001	0	CPDA[4:1],0
00010	1	CPDA[4:2],1,CPDA[0]
00010	0	CPDA[4:2],0,CPDA[0]
00011	1	CPDA[4:2],11
00011	0	CPDA[4:2],00

圖 4-7 Multi-function Comparator 方塊圖

4.8. Reset

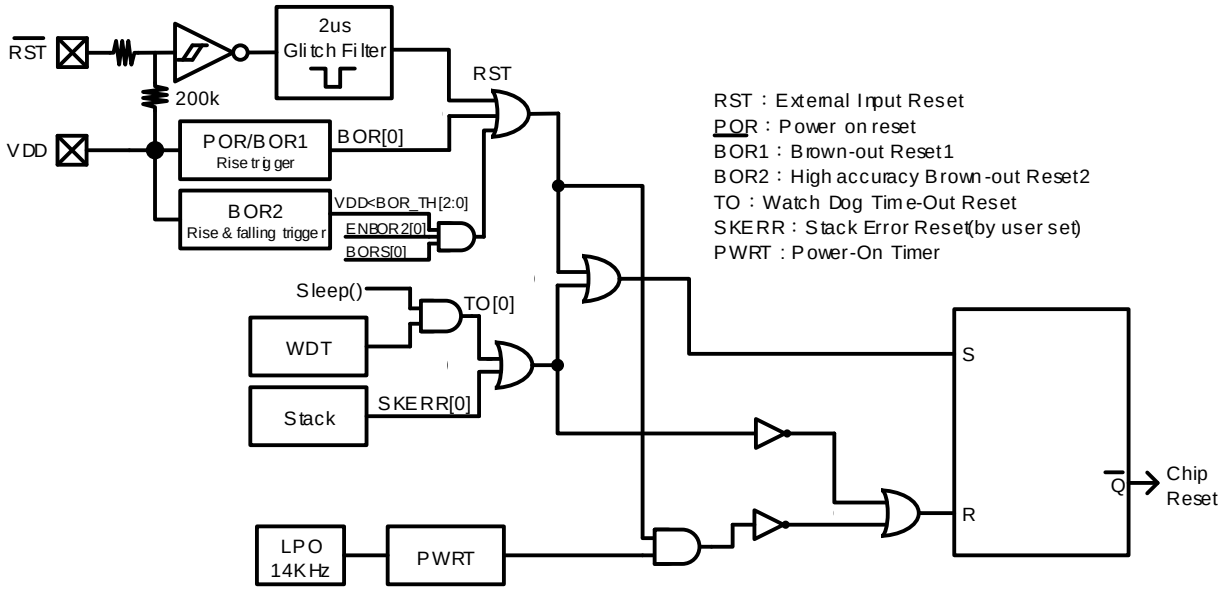
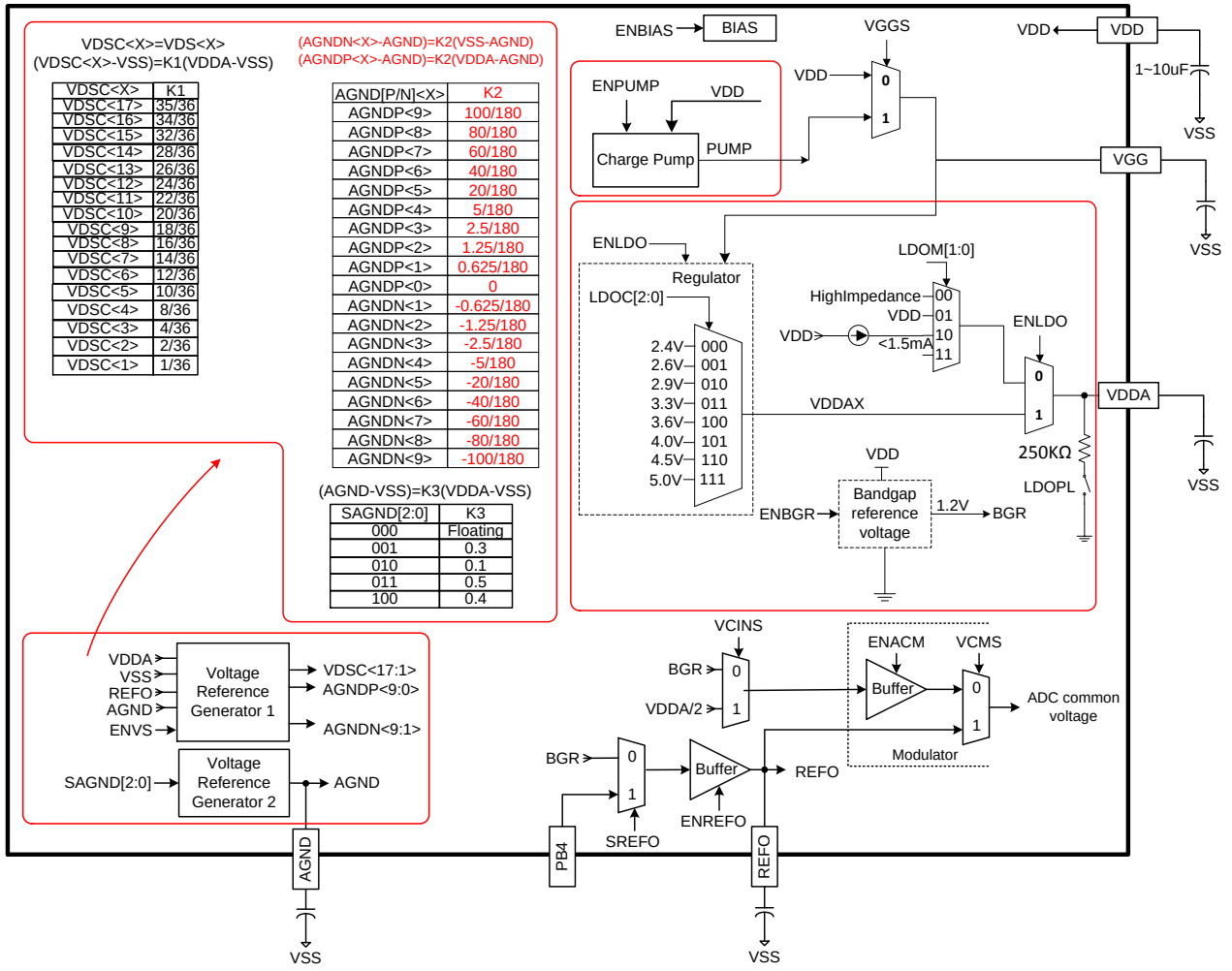


圖 4-8 Reset 方塊圖

4.9. Power Diagram



VDSC<X>	K1
VDSC<17>	35/36
VDSC<16>	34/36
VDSC<15>	32/36
VDSC<14>	28/36
VDSC<13>	26/36
VDSC<12>	24/36
VDSC<11>	22/36
VDSC<10>	20/36
VDSC<9>	18/36
VDSC<8>	16/36
VDSC<7>	14/36
VDSC<6>	12/36
VDSC<5>	10/36
VDSC<4>	8/36
VDSC<3>	4/36
VDSC<2>	2/36
VDSC<1>	1/36

AGND[P/N]<X>	K2
AGNDP<9>	100/180
AGNDP<8>	80/180
AGNDP<7>	60/180
AGNDP<6>	40/180
AGNDP<5>	20/180
AGNDP<4>	5/180
AGNDP<3>	2.5/180
AGNDP<2>	1.25/180
AGNDP<1>	0.625/180
AGNDP<0>	0
AGNDN<1>	-0.625/180
AGNDN<2>	-1.25/180
AGNDN<3>	-2.5/180
AGNDN<4>	-5/180
AGNDN<5>	-20/180
AGNDN<6>	-40/180
AGNDN<7>	-60/180
AGNDN<8>	-80/180
AGNDN<9>	-100/180

SAGND[2:0]	K3
000	Floating
001	0.3
010	0.1
011	0.5
100	0.4

圖 4-9 Power System 方塊圖

4.10. Window Comparator Network And CMP Pin

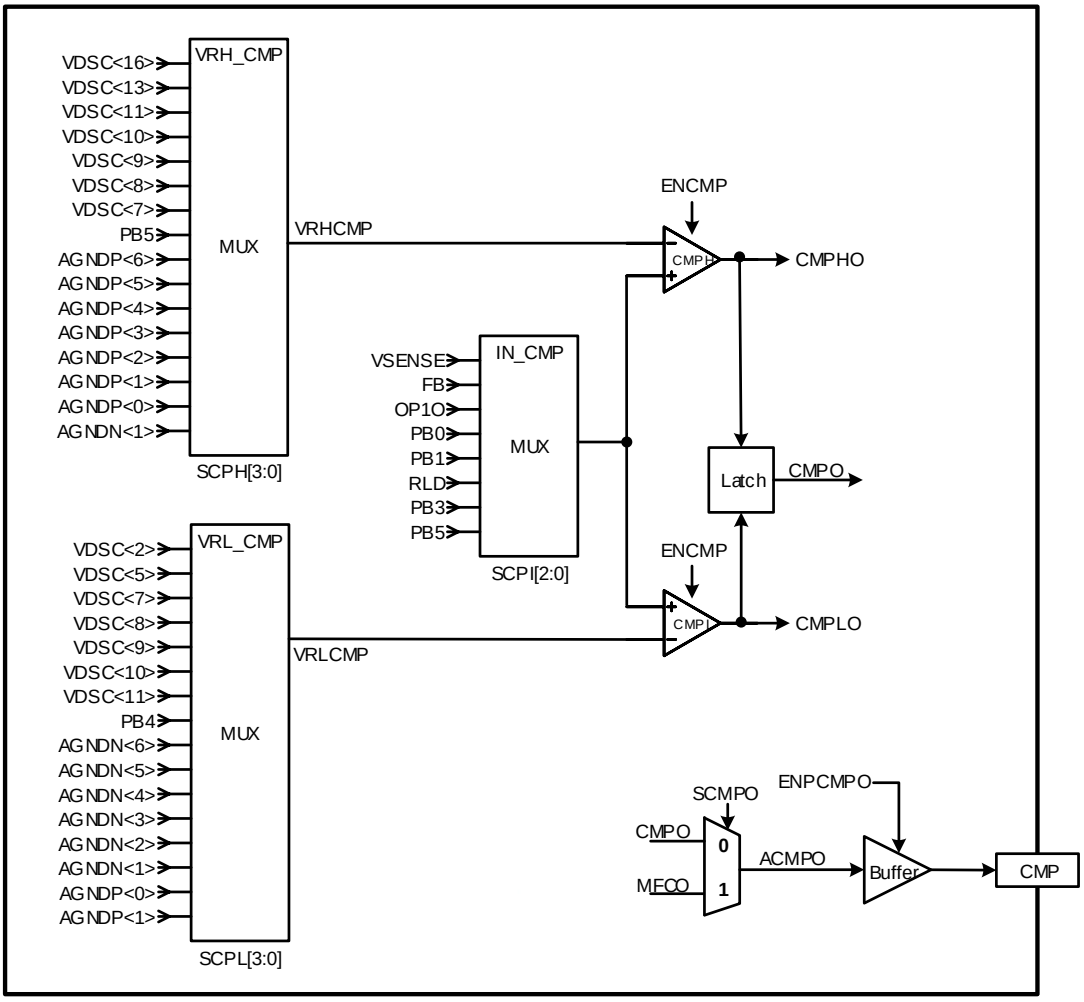


圖 4-10 Window Comparator Network 方塊圖

4.11. OPAMP

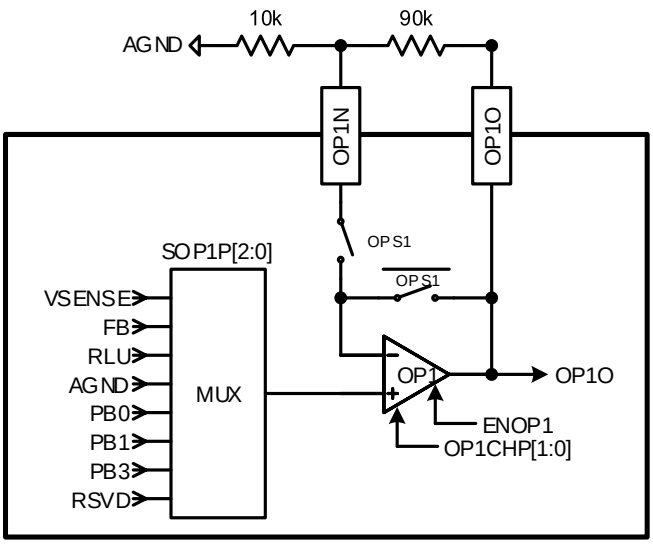


圖 4-11 OPAMP 方塊圖

4.12. Frequency Counter、CNT Pin

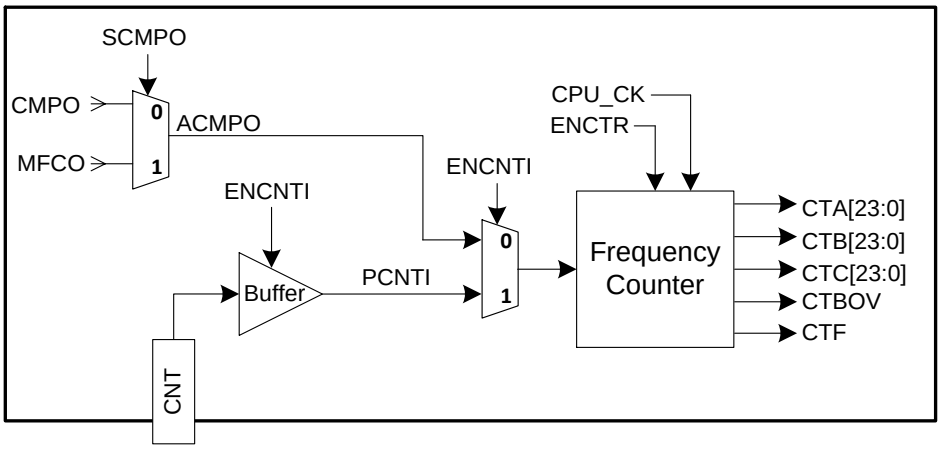


圖 4-12 Frequency Counter 方塊圖

4.13. GPIO PORT1~4,6~10

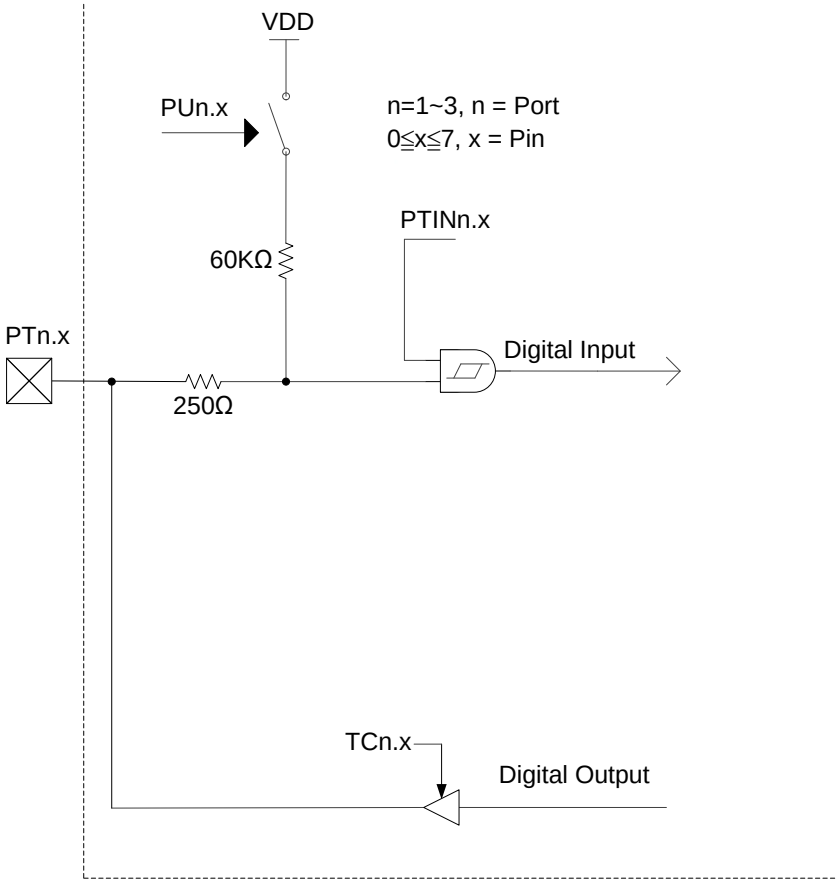


圖 4-13a GPIO PORT1~4 方塊圖

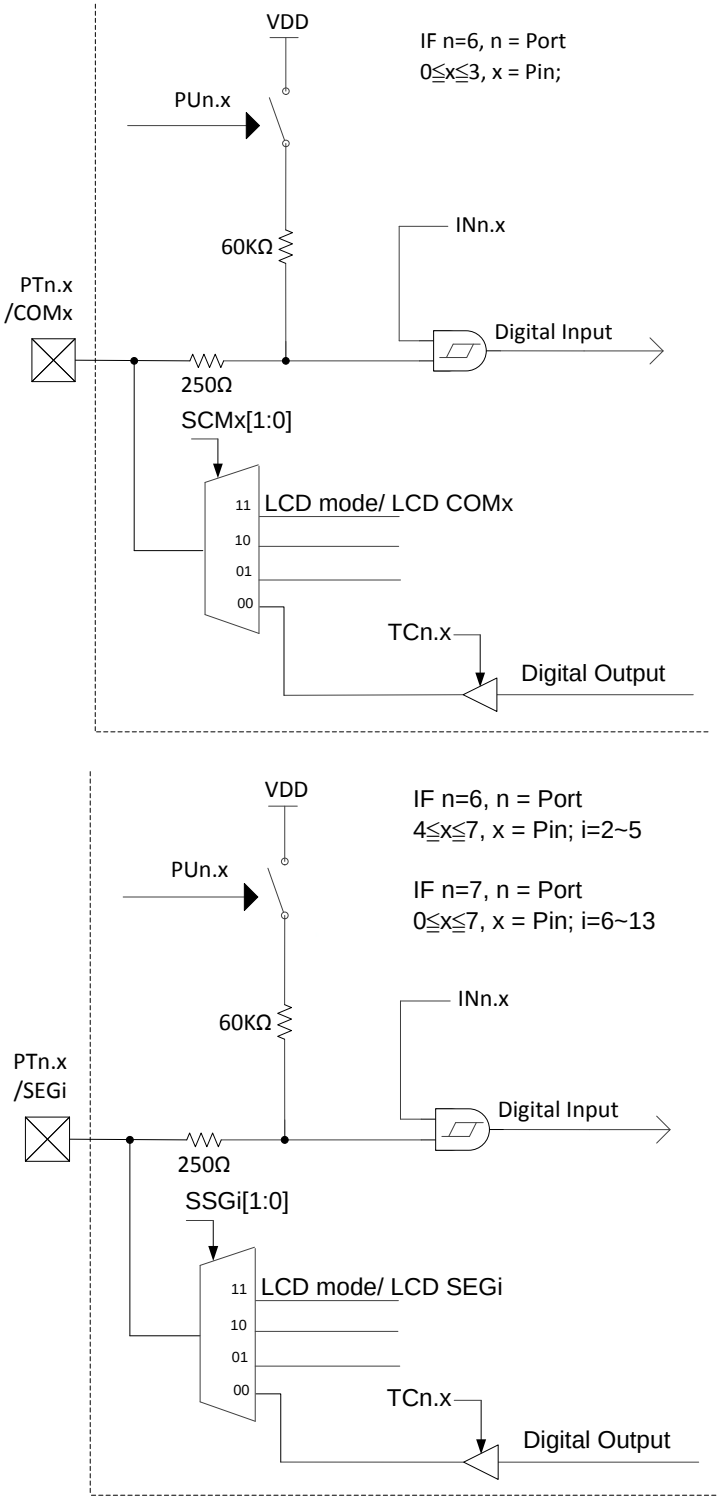


圖 4-14b I/O PORT6~7 架構方塊圖

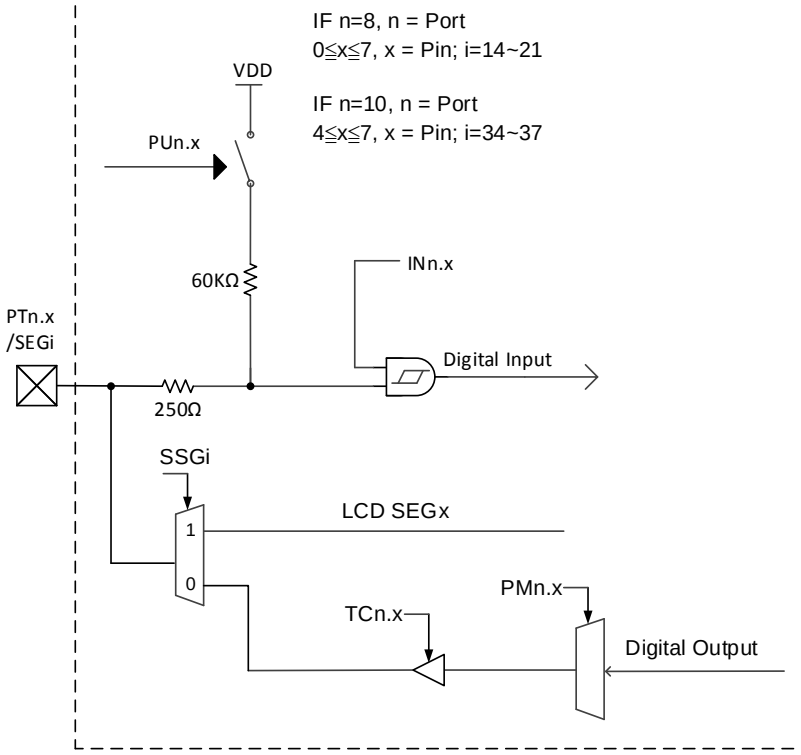


圖 4-15c I/O PORT8,10 架構方塊圖

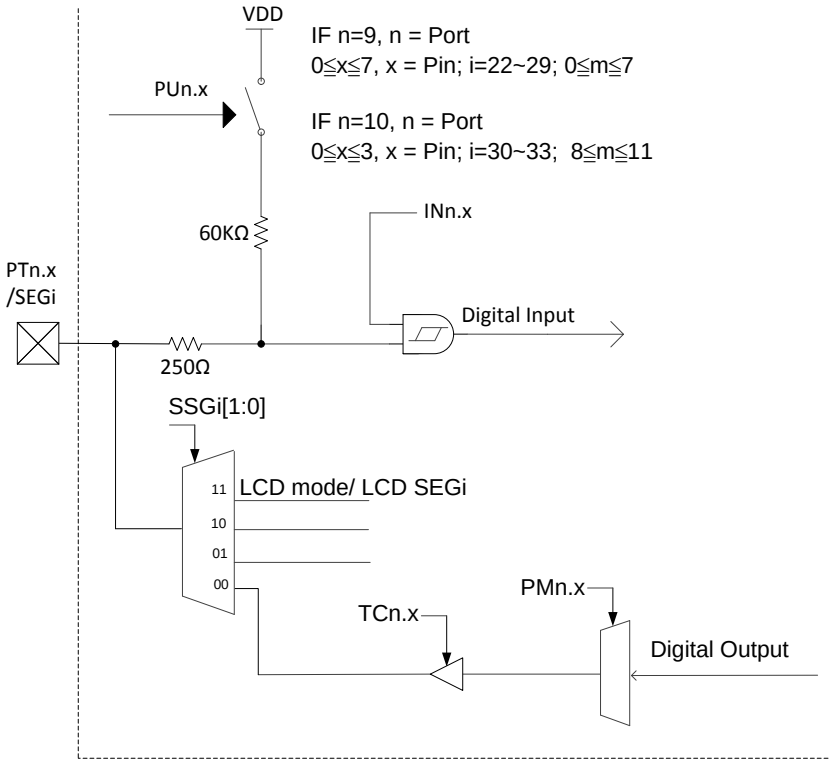


圖 4-16d I/O PORT9~10 架構方塊圖

4.14. Watch Dog

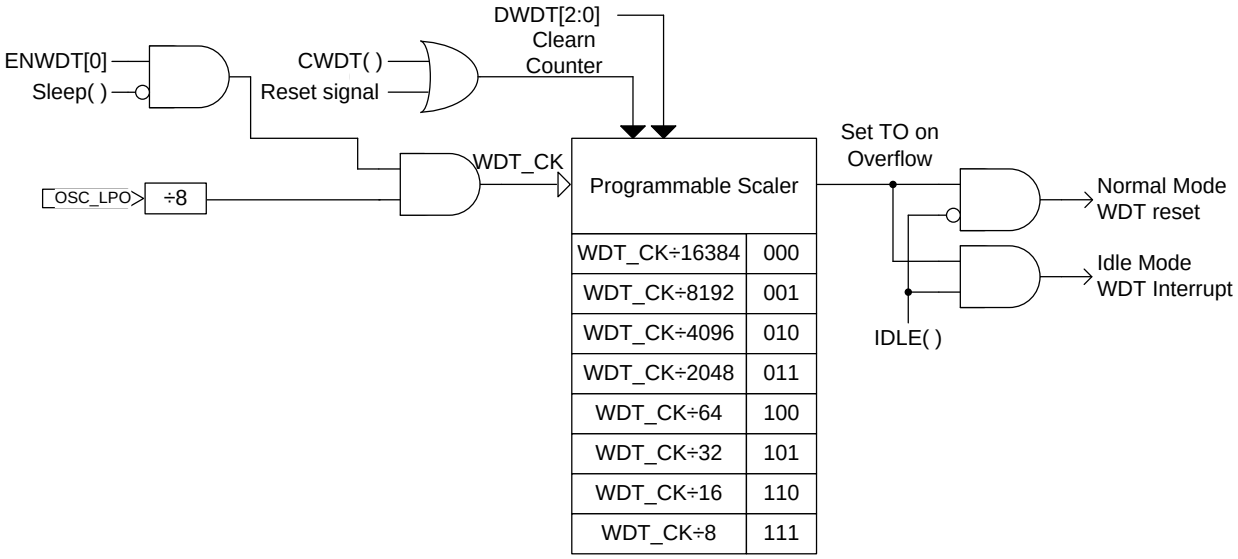


圖 4-17 Watch Dog 方塊圖

4.15. 8-bit Timer A1

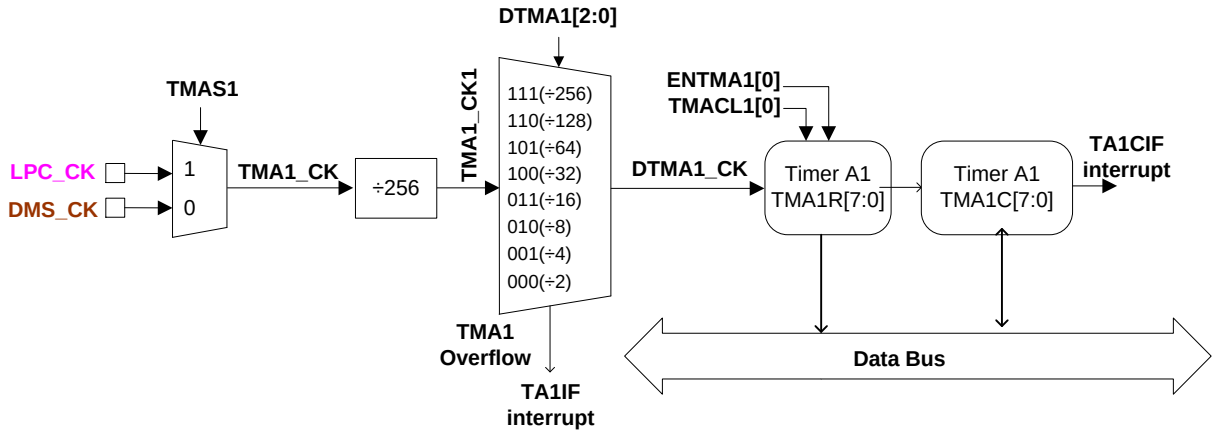


圖 4-18 8-bit Timer A1 方塊圖

4.16. 16-bit Timer B

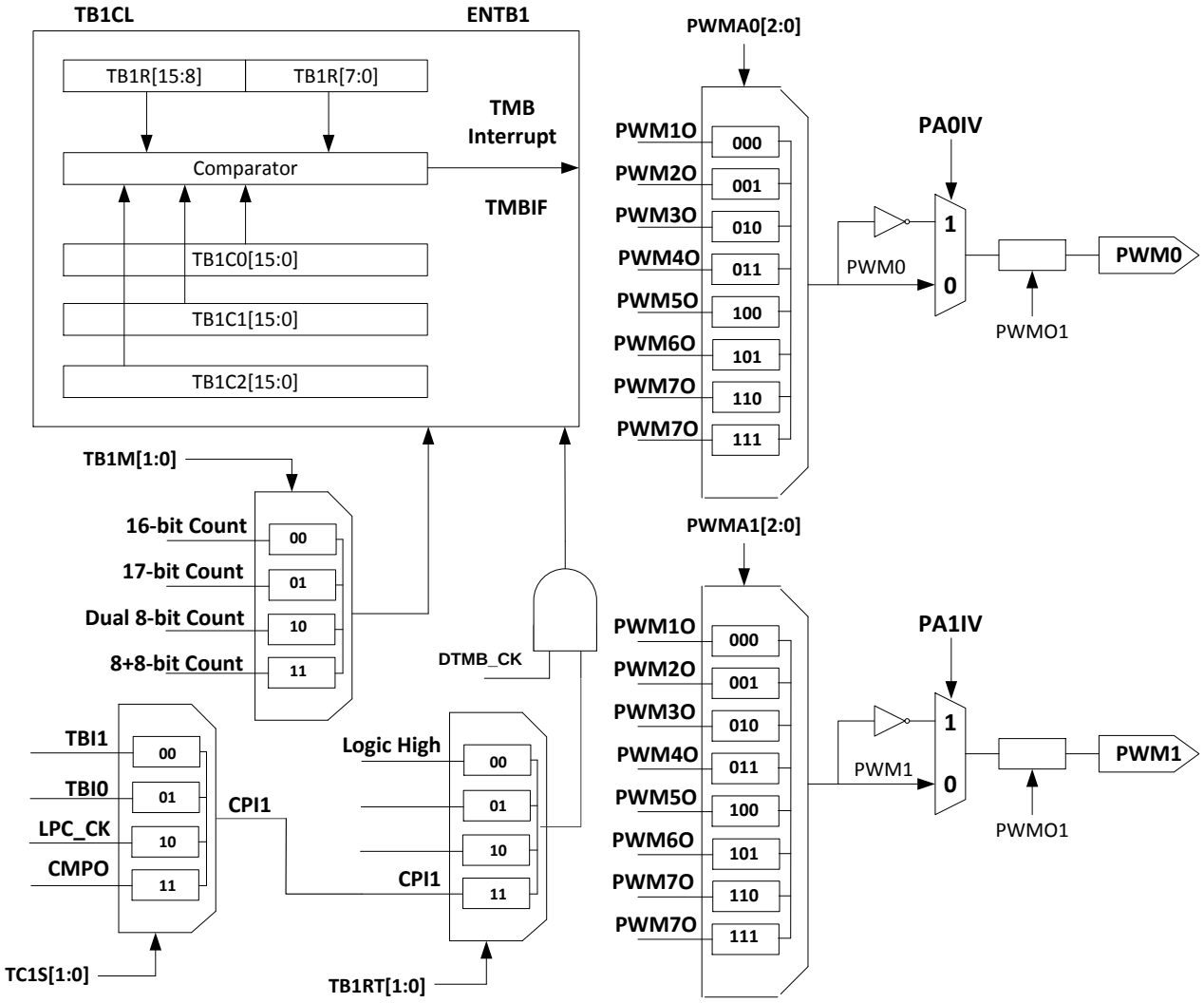


圖 4-19 16-bit Timer B 方塊圖

4.17. LCD

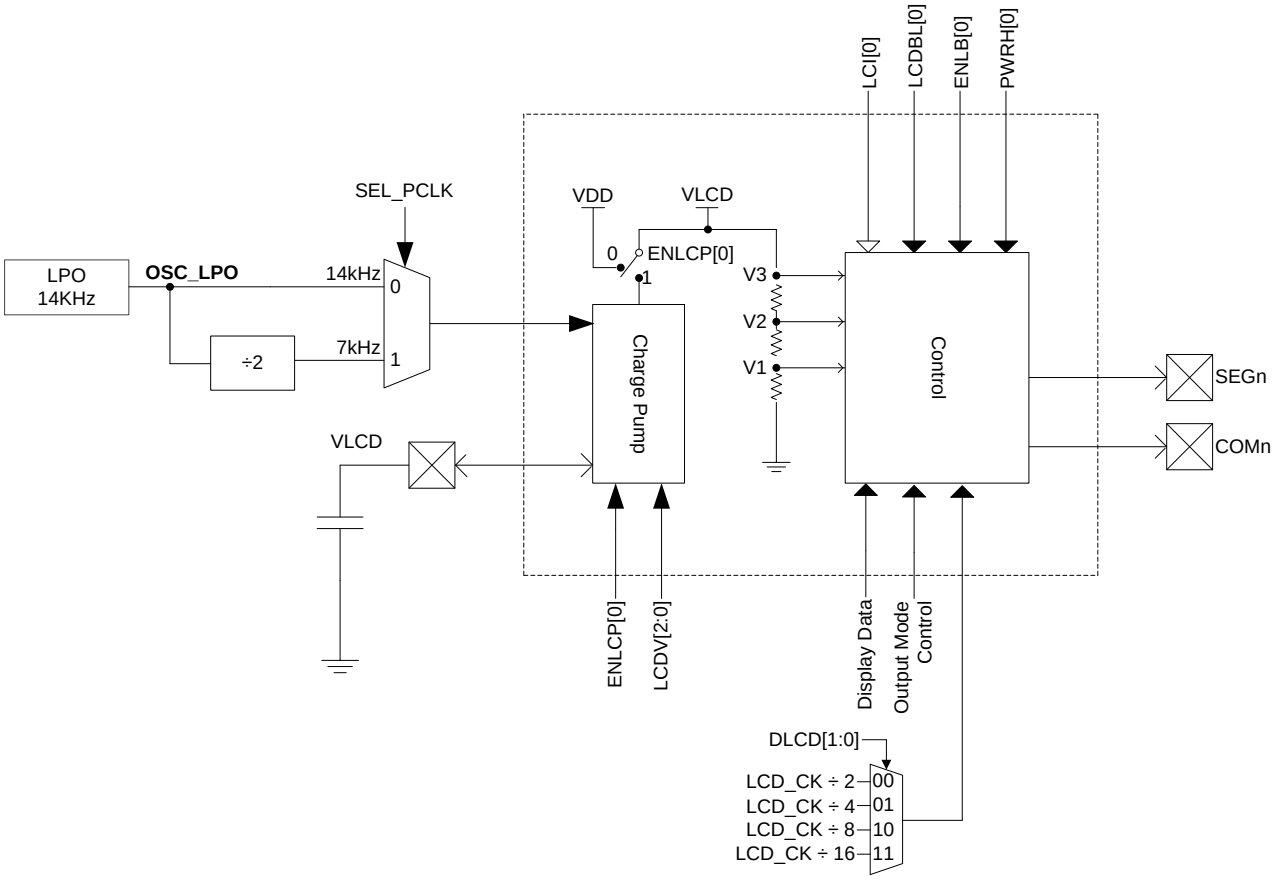


圖 4-20 LCD 方塊圖

4.18. EUART

EUART TRANSMIT BLOCK DIAGRAM

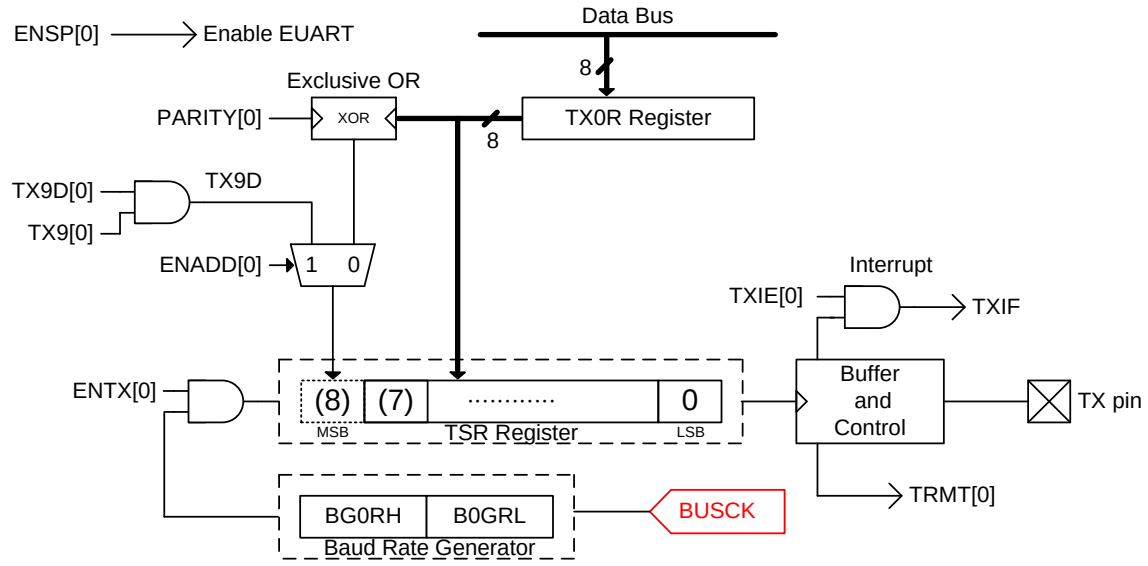
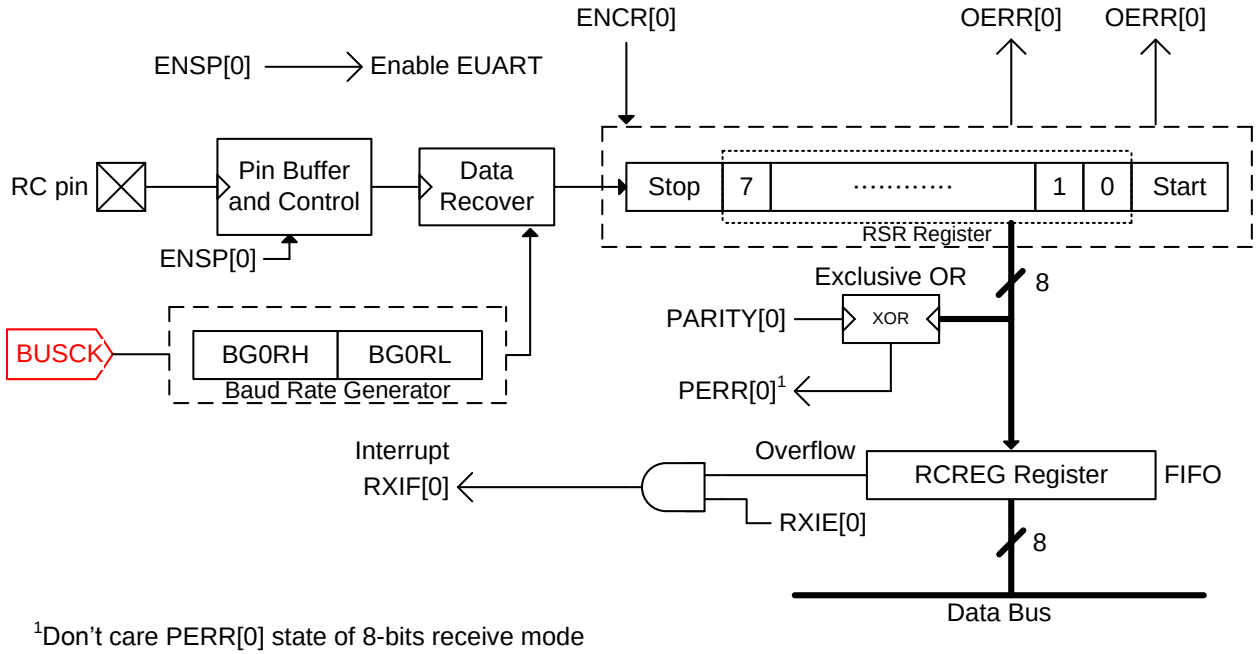


圖 4-21 EUART 傳送方塊圖

EUART 8-BITs RECEIVE BLOCK DIAGRAM



[1]Don't care PERR[0] state of 8-bits receive mode

圖 4-22 EUART 8-bits 接收方塊圖

4.19. I2C

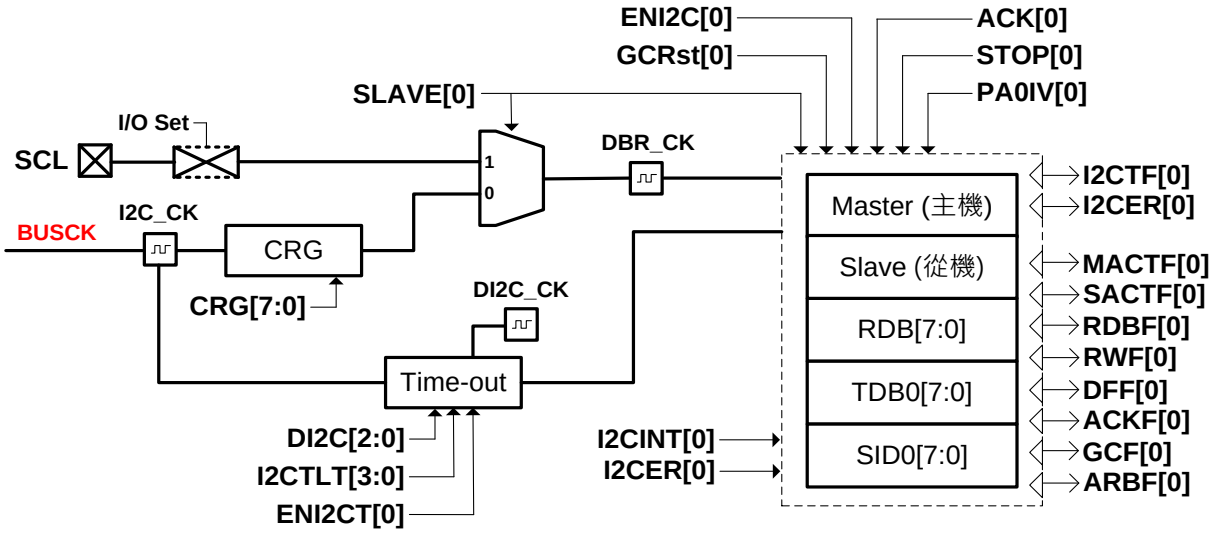


圖 4-23 I²C 方塊圖

4.20. SPI

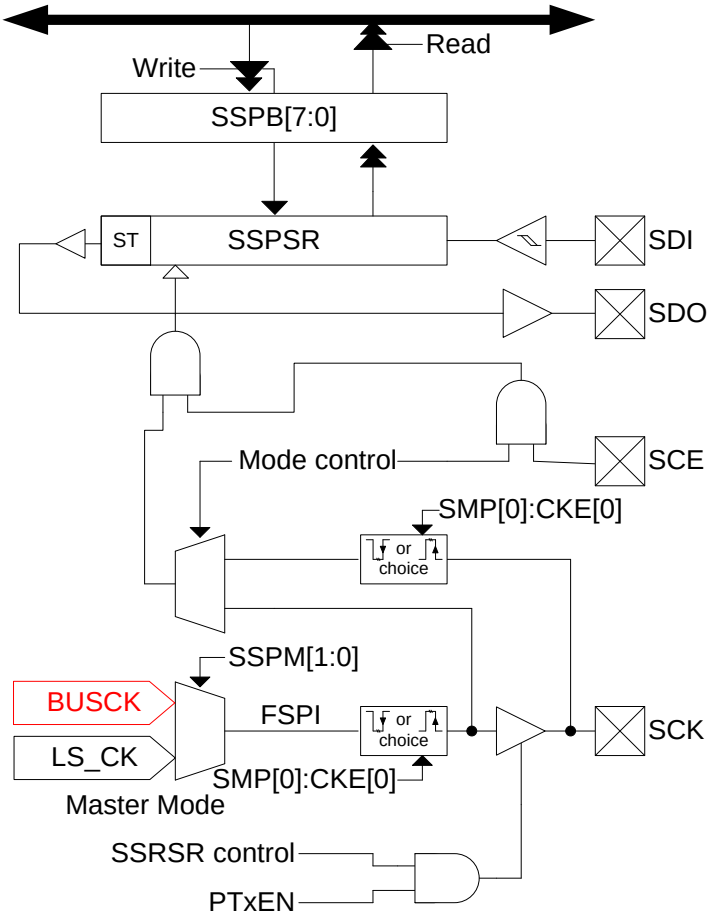


圖 4-24 SPI 方塊圖

5. 暫存器列表

"-"no use,"*"read/write,"w"write,"r"read,"r0"only read 0,"r1"only read 1,"w0"only write 0,"w1"only write 1

"$"for event status,"."unimplemented bit,"x"unknown,"u"unchanged,"d"depends on condition

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	ARST	IRST	R/W
000H	INDF0	Contents of FSR0 to address data memoryvalue of FSR0 not changed								xxxx xxxx	uuuu uuuu	*,*,*,*,*,*,*,*
001H	POINC0	Contents of FSR0 to address data memoryvalue of FSR0 post-incremented								xxxx xxxx	uuuu uuuu	*,*,*,*,*,*,*,*
002H	PODEC0	Contents of FSR0 to address data memoryvalue of FSR0 post-decremented								xxxx xxxx	uuuu uuuu	*,*,*,*,*,*,*,*
003H	PRINC0	Contents of FSR0 to address data memoryvalue of FSR0 pre-incremented								xxxx xxxx	uuuu uuuu	*,*,*,*,*,*,*,*
004H	PLUSW0	Contents of FSR0 to address data memoryvalue of FSR0 offset by W								xxxx xxxx	uuuu uuuu	*,*,*,*,*,*,*,*
005H	INDF1	Contents of FSR1 to address data memoryvalue of FSR1 not changed								xxxx xxxx	uuuu uuuu	*,*,*,*,*,*,*,*
006H	POINC1	Contents of FSR1 to address data memoryvalue of FSR1 post-incremented								xxxx xxxx	uuuu uuuu	*,*,*,*,*,*,*,*
007H	PODEC1	Contents of FSR1 to address data memoryvalue of FSR1 post-decremented								xxxx xxxx	uuuu uuuu	*,*,*,*,*,*,*,*
008H	PRINC1	Contents of FSR1 to address data memoryvalue of FSR1 pre-incremented								xxxx xxxx	uuuu uuuu	*,*,*,*,*,*,*,*
009H	PLUSW1	Contents of FSR1 to address data memoryvalue of FSR1 offset by W								xxxx xxxx	uuuu uuuu	*,*,*,*,*,*,*,*
00AH	INDF2	Contents of FSR2 to address data memoryvalue of FSR2 not changed								xxxx xxxx	uuuu uuuu	*,*,*,*,*,*,*,*
00BH	POINC2	Contents of FSR2 to address data memoryvalue of FSR2 post-incremented								xxxx xxxx	uuuu uuuu	*,*,*,*,*,*,*,*
00CH	PODEC2	Contents of FSR2 to address data memoryvalue of FSR2 post-decremented								xxxx xxxx	uuuu uuuu	*,*,*,*,*,*,*,*
00DH	PRINC2	Contents of FSR2 to address data memoryvalue of FSR2 pre-incremented								xxxx xxxx	uuuu uuuu	*,*,*,*,*,*,*,*
00EH	PLUSW2	Contents of FSR2 to address data memoryvalue of FSR2 offset by W								xxxx xxxx	uuuu uuuu	*,*,*,*,*,*,*,*
00FH	FSR0H	-	-	-	-	-	FSR0[10:8]			 xxxx	.... .uuu	-,-,-,-,*,*,*,*
010H	FSR0L	Indirect Data Memory Address Pointer 0 Low Byte,FSR0[7:0]								xxxx xxxx	uuuu uuuu	*,*,*,*,*,*,*,*
011H	FSR1H	-	-	-	-	-	FSR1[10:8]			xxx	.... .uuu	-,-,-,-,*,*,*,*
012H	FSR1L	Indirect Data Memory Address Pointer 0 Low Byte,FSR1[7:0]								xxxx xxxx	uuuu uuuu	*,*,*,*,*,*,*,*
013H	FSR2H	-	-	-	-	-	FSR2[10:8]			xxx	.... .uuu	-,-,-,-,*,*,*,*
014H	FSR2L	Indirect Data Memory Address Pointer 0 Low Byte,FSR2[7:0]								xxxx xxxx	uuuu uuuu	*,*,*,*,*,*,*,*
015H	TOSU	-	-	-	-	-	-	-	-	xxxx xxxx	uuuu uuuu	*,*,*,*,*,*,*,*
016H	TOSH			Top-of-Stack High Byte (TOS[13:8])						.xxx xxxx	..uu uuuu	-,*,*,*,*,*,*,*
017H	TOSL	Top-of-Stack Low Byte (TOS[7:0])								xxxx xxxx	uuuu uuuu	*,*,*,*,*,*,*,*
018H	SKCN	SKFL	SKUN	SKOV	SKPRT[4:0]					0000 0000	u$$$ $$$$	rw0,rw0,rw0,* *,*,*,*
019H	PCLATU	-	-	-	-	-	-	-	-	xxxx xxxx	uuuu uuuu	*,*,*,*,*,*,*,*
01AH	PCLATH			PC High Byte for PC[13:8]						..00 0000	..00 0000	*,*,*,*,*,*,*,*
01BH	PCLATL	PC Low Byte for PC[7:0]								0000 0000	0000 0000	*,*,*,*,*,*,*,*
01CH	TBLPTRU	-	-	-	-	-	-	-	-	xxxx xxxx	uuuu uuuu	*,*,*,*,*,*,*,*
01DH	TBLPTRH	-	-	Program Memory Table Pointer High Byte (TBLPTR[13:8])						..xx xxxx	..uu uuuu	-,-,*,*,*,*,*,*
01EH	TBLPTRL	Program Memory Table Pointer Low Byte (TBLPTR[7:0])								xxxx xxxx	uuuu uuuu	*,*,*,*,*,*,*,*
01FH	TBLDH	Program Memory Table Latch High Byte								xxxx xxxx	uuuu uuuu	*,*,*,*,*,*,*,*
020H	TBLDL	Program Memory Table Latch Low Byte								xxxx xxxx	uuuu uuuu	*,*,*,*,*,*,*,*
021H	PRODH	Product Register of Multiply High Byte								xxxx xxxx	uuuu uuuu	*,*,*,*,*,*,*,*
022H	PRODL	Product Register of Multiply Low Byte								xxxx xxxx	uuuu uuuu	*,*,*,*,*,*,*,*
023H	INTE0	GIE	TA1CIE	ADIE	WDTIE	TB1IE	CTIE	E1IE	E0IE	0000 0000	0uuu uuuu	*,*,*,*,*,*,*,*
024H	INTE1	TA1IE	SPIIE	TXIE	RCIE	I2CERIE	I2CIE	E3IE	E2IE	0000 0000	uuuu uuuu	*,*,*,*,*,*,*,*
025H	INTE2	MFCIE	CMPOIE	CMPHOIE	CMPLOIE	CTBOVE	RMSIE	LPFIE	BOR2IE	.000 0000	.uuu uuuu	*,*,*,*,*,*,*,*
026H	INTF0	-	TA1CIF	ADIF	WDTIF	TB1IF	CTF	E1IF	E0IF	.000 0000	.uuu uuuu	*,*,*,*,*,*,*,*
027H	INTF1	TA1IF	SPIIF	TXIF	RCIF	I2CERIF	I2CIF	E3IF	E2IF	0000 0000	uuuu uuuu	*,*,*,* r,r,*,*
028H	INTF2	MFCIF	CMPIF	CMPHIF	CMPLIF	CTBOV	RMSF	LPFF	BOR2IF	0000 0000	uuuu uuuu	*,*,*,*,*,*,*,*
029H	WREG	Working Register								xxxx xxxx	uuuu uuuu	*,*,*,*,*,*,*,*
02AH	BSRCN	-	-	-	-	-	BSR[2:0]			 xxxx	.... uuuu	-,-,-,-,*,*,*,*
02BH	MSTAT	-	-	-	C	DC	N	OV	Z	...x xxxx	...u uuuu	-,-,-,-,*,*,*,*
02CH	PSTAT	BOR	PD	TO	IDL	RST	SKERR	BOR2LV	GCRstIF	$000 $000	uu$u u$uu	rw0,rw0,rw0,rw0 rw0,rw0,r,rw0
02DH	BIECN	1	BLKSEL	-	ENBVD	VPPHV	ENBCP	BIEWR	BIERD	1.00 $000	1.00 $uuu	r1,-,*,* r,*,*,*
02EH	BIEARH	-	-	BIE High Byte Address Register as BIEA[13:8]						0.xx xxxx	u.uu uuuu	*,-,*,*,*,*,*,*
02FH	BIEARL	BIE Low Byte Address Register as BIEA[7:0]								xxxx xxxx	uuuu uuuu	*,*,*,*,*,*,*,*
030H	BIEDRH	BIE High Byte Data Register								xxxx xxxx	uuuu uuuu	*,*,*,*,*,*,*,*
031H	BIEDRL	BIE Low Byte Data Register								xxxx xxxx	uuuu uuuu	*,*,*,*,*,*,*,*
032H	PWRCN	ENBGR	LDOC[2:0]			LDOM[1:0]		ENLDO	CSFON	1000 0000	1uuu u00u	*,*,*,* *,wr0,wr0,*
033H	PWRCN1	ENREFO	ENCMP	ENCNTI	ENCTR	ENVS	SAGND[2:0]			0000 0000	uuuu uuuu	*,*,*,*,*,*,*,*
034H	PWRCN2	ENPUMP	VGGS	CHP_CKS[1]	CHP_CKS[0]	ENFIR	LDOPL	ENTPS	-	0000 0000	uuuu uuuu	*,*,*,*,*,*,*,*
035H	OSCCN0	OSCS[1:0]		DHS[1:0]		DMS[2:0]			CUPS	0000 0000	uuuu uuuu	*,*,*,*,*,*,*,*
036H	OSCCN1	CCOPT	LCPS	DADC[1:0]		DTMB[1:0]		TMBS	LCDS	0000 0000	uuuu uuu.	*,*,*,*,*,*,*,-
037H	OSCCN2	DLCD[1:0]		ENXT	XTS[1:0]		HAOM[1:0]		ENHAO	0000 0001	uuuu uuu1	*,*,*,*,*,*,*,*

表 5-1 資料記憶體列表

"-"no use,"*"read/write,"w"write,"r"read,"r0"only read 0,"r1"only read 1,"w0"only write 0,"w1"only write 1
"$"for event status,"."unimplemented bit,"x"unknown,"u"unchanged,"d"depends on condition

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	ARST	IRST	R/W
038H	CSFCN0	SKRST	HAOTR[6:0]							.1..	....	*,*,*,*,*,*,*,*
039H	CSFCN1	BUSCKS	-	-	BOR_TH[2:0]			BORS	ENBOR2	0000 0011	uuuu uuuu	*,*,*,*,*,*,*,*
03AH	WDTCN	ENBZ	BZS	DBZ[1:0]		ENWDT	DWDT[2:0]			0000 0000	uuuu $000	-,*,*,* rw1,*,*,*
03BH	AD1CN0	ENAD1	ENCH	ENINXCH	VREGN	OSR[2:0]			CMFR	000. 0000	uuu. uuuu	*,*,*,*,*,*,*,*
03CH	AD1CN1	ENACM	VCMS	VCINS	TPSCH	TPSCP	ADGN[2:0]			xxxx xxxx	uuuu uuuu	*,*,*,*,*,*,*,*
03DH	AD1CN2	FilterN[1:0]		-	DAFM	DCSET[3:0]				xxxx xxxx	uuuu uuuu	*,*,*,*,*,*,*,*
03EH	AD1CN3	SAD1FP[3:0]				-	SAD1FN[2:0]			xxxx xxxx	uuuu uuuu	*,*,*,*,*,*,*,*
03FH	AD1CN4	AD1RHBUF	AD1RLBUF	AD1IPBUF	AD1INBUF	INX[1:0]		VRIS	INIS	0000 0000	uuuu uuuu	*,*,*,*,*,*,*,*
040H	AD1CN5	SAD1RH[2:0]			SAD1RL[2:0]			SAD1I[1:0]		0000 0000	uuuu uuuu	*,*,*,*,*,*,*,*
041H	RMSCN	ENRMS	ENLPF	ENSQRE	LPFBW[1:0]		ENPKH	RSLPF	RSRMS	0000 0000	uuuu uuuu	*,*,*,*,*,*,*,*
042H	NET0	SDIO	SREFO	SFT1[1:0]		SFUVR[3:0]				0000 0000	uuuu uuuu	*,*,*,*,*,*,*,*
043H	NET1	SMODE[7:4]				SMODE[3:0]				0000 0000	uuuu uuuu	*,*,*,*,*,*,*,*
044H	NET2	SCMPRH[3:0]				SCMPRL[3:0]				0000 0000	uuuu uuuu	*,*,*,*,*,*,*,*
045H	NET3	SCMPI[2:0]			SCMPO	CMPO	CMPHO	CMPLO	CNTI_IF	0000 0000	uuuu uuuu	*,*,*,*,*,*,*,*
046H	PA1110	PS11	DS11	FS11	SS11	PS10	DS10	FS10	SS10	0000 0000	uuuu uuuu	*,*,*,*,*,*,*,*
047H	PA98	PS9	DS9	FS9	SS9	PS8	DS8	FS8	SS8	0000 0000	uuuu uuuu	*,*,*,*,*,*,*,*
048H	PA76	PS7	DS7	FS7	SS7	PS6	DS6	FS6	SS6	0000 0000	uuuu uuuu	*,*,*,*,*,*,*,*
049H	PA54	PS5	DS5	FS5	SS5	PS4	DS4	FS4	SS4	0000 0000	uuuu uuuu	*,*,*,*,*,*,*,*
04AH	PA32	PS3	DS3	FS3	SS3	PS2	DS2	FS2	SS2	0000 0000	uuuu uuuu	*,*,*,*,*,*,*,*
04BH	PA10	PS1	DS1	FS1	SS1	PS0	DS0	FS0	SS0	0000 0000	uuuu uuuu	*,*,*,*,*,*,*,*
04CH	CTAU	CTA[23:16]								xxxx xxxx	uuuu uuuu	r,r,r,r r,r,r,r
04DH	CTAH	CTA[15:8]								xxxx xxxx	uuuu uuuu	r,r,r,r r,r,r,r
04EH	CTAL	CTA[7:0]								xxxx xxxx	uuuu uuuu	r,r,r,r r,r,r,r
04FH	CTBU	CTB[23:16]								xxxx xxxx	uuuu uuuu	r,r,r,r r,r,r,r
050H	CTBH	CTB[15:8]								xxxx xxxx	uuuu uuuu	r,r,r,r r,r,r,r
051H	CTBL	CTB[7:0]								xxxx xxxx	uuuu uuuu	r,r,r,r r,r,r,r
052H	CTCU	CTC[23:16]								xxxx xxxx	uuuu uuuu	r,r,r,r r,r,r,r
053H	CTCH	CTC[15:8]								xxxx xxxx	uuuu uuuu	r,r,r,r r,r,r,r
054H	CTCL	CTC[7:0]								xxxx xxxx	uuuu uuuu	r,r,r,r r,r,r,r
055H	PKHMAXU	PKHMAX[18:11]								xxxx xxxx	uuuu uuuu	r,r,r,r r,r,r,r
056H	PKHMAXH	PKHMAX[10:3]								xxxx xxxx	uuuu uuuu	r,r,r,r r,r,r,r
057H	PKHMAXL	PKHMAX[2:0]			-	-	-	-	-	xxxx xxxx	uuuu uuuu	r,r,r,r r,r,r,r
058H	PKHMINU	PKHMIN[18:11]								xxxx xxxx	uuuu uuuu	r,r,r,r r,r,r,r
059H	PKHMINH	PKHMIN[10:3]								xxxx xxxx	uuuu uuuu	r,r,r,r r,r,r,r
05AH	PKHMINL	PKHMIN[2:0]			-	-	-	-	-	xxxx xxxx	uuuu uuuu	r,r,r,r r,r,r,r
05BH	RMSDATA4	RMS[37:30]								xxxx xxxx	uuuu uuuu	r,r,r,r r,r,r,r
05CH	RMSDATA3	RMS[29:22]								xxxx xxxx	uuuu uuuu	r,r,r,r r,r,r,r
05DH	RMSDATA2	RMS[21:14]								xxxx xxxx	uuuu uuuu	r,r,r,r r,r,r,r
05EH	RMSDATA1	RMS[13:6]								xxxx xxxx	uuuu uuuu	r,r,r,r r,r,r,r
05FH	RMSDATA0	RMS[5:0]						-	-	xxxx xxxx	uuuu uuuu	r,r,r,r r,r,r,r
060H	LPFDATAU	LPF[18:11]								xxxx xxxx	uuuu uuuu	r,r,r,r r,r,r,r
061H	LPFDATAH	LPF[10:3]								xxxx xxxx	uuuu uuuu	r,r,r,r r,r,r,r
062H	LPFDATAL	LPF[2:0]			-	-	-	-	-	xxxx xxxx	uuuu uuuu	r,r,r,r r,r,r,r
063H	AD1DATAU	AD1[18:11]								xxxx xxxx	uuuu uuuu	r,r,r,r r,r,r,r
064H	AD1DATAH	AD1[10:3]								xxxx xxxx	uuuu uuuu	r,r,r,r r,r,r,r
065H	AD1DATAL	AD1[2:0]			-	-	-	-	-	xxxx xxxx	uuuu uuuu	r,r,r,r r,r,r,r
066H	OP1CN0	ENOP1	SOP1P[2:0]			OP1CHOP[1:0]		HS	OPS1	0000 0000	uuuu uuuu	*,*,*,*,*,*,*,*
067H	ACC	Capacitor array								0000 0000	uuuu uuuu	*,*,*,*,*,*,*,*
068H	TMA1CN	ENTMA1	TMACL1	TMAS1	DTMA1[2:0]			-	-	0000 00.0	u0uu uu.u	*,rw1,*,*,*,-,*
069H	TMA1R	TMA1 counter Register								0000 0000	uuuu uuuu	rw0,rw0,rw0,rw0 rw0,rw0,rw0,rw0
06AH	TMA1C	TMA1C counter Register								0000 0000	uuuu uuuu	rw0,rw0,rw0,rw0 rw0,rw0,rw0,rw0
06BH	PT1	PT1.7	PT1.6	PT1.5	PT1.4	PT1.3	PT1.2	PT1.1	PT1.0	xxxx xxxx	uuuu uuuu	*,*,*,*,*,*,*,*
06CH	PT1IN	IN1.7	IN1.6	IN1.5	IN1.4	IN1.3	IN1.2	IN1.1	IN1.0	0000 0000	uuuu uuuu	*,*,*,*,*,*,*,*
06DH	TRISC1	TC1.7	TC1.6	TC1.5	TC1.4	TC1.3	TC1.2	TC1.1	TC1.0	0000 0000	uuuu uuuu	*,*,*,*,*,*,*,*
06EH	PT1PU	PU1.7	PU1.6	PU1.5	PU1.4	PU1.3	PU1.2	PU1.1	PU1.0	0000 0000	uuuu uuuu	*,*,*,*,*,*,*,*
06FH	PT1M1					INTEG1[1:0]		INTEG0[1:0]		0000 0000	uuuu uuuu	*,*,*,*,*,*,*,*
070H	PT1INT	INTEG7	INTEG6	INTEG5	INTEG4	INTEG3	INTEG2	-	-	0000 0000	uuuu uuuu	*,*,*,*,*,*,*,*
071H	PT1INTE	INTE1.7	INTE1.6	INTE1.5	INTE1.4	-	-	-	-	0000 0000	uuuu uuuu	*,*,*,*,*,*,*,*
072H	PT1INTF	INTF1.7	INTF1.6	INTF1.5	INTF1.4	-	-	-	-	0000 0000	uuuu uuuu	*,*,*,*,*,*,*,*

表 5-2 資料記憶體列表(續)

"-"no use,"*"read/write,"w"write,"r"read,"r0"only read 0,"r1"only read 1,"w0"only write 0,"w1"only write 1
"$"for event status,"."unimplemented bit,"x"unknown,"u"unchanged,"d"depends on condition

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	ARST	IRST	R/W
073H	PT2	PT2.7	PT2.6	PT2.5	PT2.4	PT2.3	PT2.2	PT2.1	PT2.0	xxxx xxxx	uuuu uuuu	*,*,*,*,*,*,*,*
074H	PT2IN	IN2.7	IN2.6	IN2.5	IN2.4	IN2.3	IN2.2	IN2.1	IN2.0	0000 0000	uuuu uuuu	*,*,*,*,*,*,*,*
075H	TRISC2	TC2.7	TC2.6	TC2.5	TC2.4	TC2.3	TC2.2	TC2.1	TC2.0	0000 0000	uuuu uuuu	*,*,*,*,*,*,*,*
076H	PT2PU	PU2.7	PU2.6	PU2.5	PU2.4	PU2.3	PU2.2	PU2.1	PU2.0	0000 0000	uuuu uuuu	*,*,*,*,*,*,*,*
077H	PT2INT	INTG2.7	INTG2.6	INTG2.5	INTG2.4	INTG2.3	INTG2.2	INTG2.1	INTG2.0	0000 0000	uuuu uuuu	*,*,*,*,*,*,*,*
078H	PT2INTE	INTE2.7	INTE2.6	INTE2.5	INTE2.4	INTE2.3	INTE2.2	INTE2.1	INTE2.0	0000 0000	uuuu uuuu	
079H	PT2INTF	INTF2.7	INTF2.6	INTF2.5	INTF2.4	INTF2.3	INTF2.2	INTF2.1	INTF2.0	0000 0000	uuuu uuuu	*,*,*,*,*,*,*,*
07AH	MFCCN0	CPRH[1:0]		MFCO	CPIS	CPOR	CPDF	CMPHS	ENMFC	0000 0000	uuuu uuuu	*,*,r,*,*,*,*,*
07BH	MFCCN1	CPRL[2:0]			-	CPPS[1:0]		CPNS[1:0]		0000 0000	uuuu uuuu	*,*,*,*,*,*,*,*
07CH	MFCCN2	-	-	-	CPDA[4:0]					0000 0000	uuuu uuuu	*,*,*,*,*,*,*,*
07DH	MFCCN3	-	-	-	CPDM[4:0]					0000 0000	uuuu uuuu	*,*,*,*,*,*,*,*
180H	LCDCN1	ENLCP	LCDV[2:0]			ENLB	SELPCLK	LCDBL	ENLCD	0000 0000	uuuu uuuu	*,*,*,*,*,*,*,*
181H	LCDCN2									0000 0000	uuuu uuuu	*,*,*,*,*,*,*,*
182H	LCDCN3	SCM3[1:0]		SCM2[1:0]		SCM1[1:0]		SCM0[1:0]		0000 0000	uuuu uuuu	*,*,*,*,*,*,*,*
183H	LCDCN4	SSG21	SSG20	SSG19	SSG18	SSG17	SSG16	SSG15	SSG14	0000 0000	uuuu uuuu	*,*,*,*,*,*,*,*
184H	LCDCN5					SSG37	SSG36	SSG35	SSG34	0000 0000	uuuu uuuu	*,*,*,*,*,*,*,*
185H	LCDCN6	SSG5[1:0]		SSG4[1:0]		SSG3[1:0]		SSG02[1:0]		0000 0000	uuuu uuuu	*,*,*,*,*,*,*,*
186H	LCDCN7	SSG9[1:0]		SSG8[1:0]		SSG7[1:0]		SSG6[1:0]		0000 0000	uuuu uuuu	*,*,*,*,*,*,*,*
187H	LCDCN8	SSG13[1:0]		SSG12[1:0]		SSG11[1:0]		SSG10[1:0]		0000 0000	uuuu uuuu	*,*,*,*,*,*,*,*
188H	LCDCN9	SSG25[1:0]		SSG24[1:0]		SSG23[1:0]		SSG22[1:0]		0000 0000	uuuu uuuu	*,*,*,*,*,*,*,*
189H	LCDCN10	SSG29[1:1]		SSG28[1:1]		SSG27[1:1]		SSG26[1:1]		0000 0000	uuuu uuuu	*,*,*,*,*,*,*,*
18AH	LCDCN11	SSG33[1:1]		SSG32[1:1]		SSG31[1:1]		SSG30[1:1]		0000 0000	uuuu uuuu	*,*,*,*,*,*,*,*
18BH	LCD0	LCD SEG3[4:7] data				LCD SEG2[3:0] data				xxxx xxxx	uuuu uuuu	*,*,*,*,*,*,*,*
18CH	LCD1	LCD SEG5[4:7] data				LCD SEG4[3:0] data				xxxx xxxx	uuuu uuuu	*,*,*,*,*,*,*,*
18DH	LCD2	LCD SEG7[4:7] data				LCD SEG6[3:0] data				xxxx xxxx	uuuu uuuu	*,*,*,*,*,*,*,*
18EH	LCD3	LCD SEG9[4:7] data				LCD SEG8[3:0] data				xxxx xxxx	uuuu uuuu	*,*,*,*,*,*,*,*
18FH	LCD4	LCD SEG11[4:7] data				LCD SEG10[3:0] data				xxxx xxxx	uuuu uuuu	*,*,*,*,*,*,*,*
190H	LCD5	LCD SEG13[4:7] data				LCD SEG12[3:0] data				xxxx xxxx	uuuu uuuu	*,*,*,*,*,*,*,*
191H	LCD6	LCD SEG15[4:7] data				LCD SEG14[3:0] data				xxxx xxxx	uuuu uuuu	*,*,*,*,*,*,*,*
192H	LCD7	LCD SEG17[4:7] data				LCD SEG16[3:0] data				xxxx xxxx	uuuu uuuu	*,*,*,*,*,*,*,*
193H	LCD8	LCD SEG19[4:7] data				LCD SEG18[3:0] data				xxxx xxxx	uuuu uuuu	*,*,*,*,*,*,*,*
194H	LCD9	LCD SEG21[4:7] data				LCD SEG20[3:0] data				xxxx xxxx	uuuu uuuu	*,*,*,*,*,*,*,*
195H	LCD10	LCD SEG23[4:7] data				LCD SEG22[3:0] data				xxxx xxxx	uuuu uuuu	*,*,*,*,*,*,*,*
196H	LCD11	LCD SEG25[4:7] data				LCD SEG24[3:0] data				xxxx xxxx	uuuu uuuu	*,*,*,*,*,*,*,*
197H	LCD12	LCD SEG27[4:7] data				LCD SEG26[3:0] data				xxxx xxxx	uuuu uuuu	*,*,*,*,*,*,*,*
198H	LCD13	LCD SEG29[4:7] data				LCD SEG28[3:0] data				xxxx xxxx	uuuu uuuu	*,*,*,*,*,*,*,*
199H	LCD14	LCD SEG31[4:7] data				LCD SEG30[3:0] data				xxxx xxxx	uuuu uuuu	*,*,*,*,*,*,*,*
19AH	LCD15	LCD SEG33[4:7] data				LCD SEG32[3:0] data				xxxx xxxx	uuuu uuuu	*,*,*,*,*,*,*,*
19BH	LCD16	LCD SEG35[4:7] data				LCD SEG34[3:0] data				xxxx xxxx	uuuu uuuu	*,*,*,*,*,*,*,*
19CH	LCD17	LCD SEG37[4:7] data				LCD SEG36[3:0] data				xxxx xxxx	uuuu uuuu	*,*,*,*,*,*,*,*
19DH	LCD18	LCD SEG39[4:7] data				LCD SEG38[3:0] data				xxxx xxxx	uuuu uuuu	*,*,*,*,*,*,*,*
19EH	LCD19	LCD SEG41[4:7] data				LCD SEG40[3:0] data				xxxx xxxx	uuuu uuuu	*,*,*,*,*,*,*,*
19FH	PT3	PT3.7	PT3.6	PT3.5	PT3.4	PT3.3	PT3.2	PT3.1	PT3.0	xxxx xxxx	uuuu uuuu	*,*,*,*,*,*,*,*
1A0H	PT3IN	IN3.7	IN3.6	IN3.5	IN3.4	IN3.3	IN3.2	IN3.1	IN3.0	0000 0000	uuuu uuuu	*,*,*,*,*,*,*,*
1A1H	TRISC3	TC3.7	TC3.6	TC3.5	TC3.4	TC3.3	TC3.2	TC3.1	TC3.0	0000 0000	uuuu uuuu	*,*,*,*,*,*,*,*
1A2H	PT3PU	PU3.7	PU3.6	PU3.5	PU3.4	PU3.3	PU3.2	PU3.1	PU3.0	0000 0000	uuuu uuuu	*,*,*,*,*,*,*,*
1A3H	PT3M1	PM3.7 ENPCMPO				-	-	-	-	0000 0000	uuuu uuuu	*,*,*,*,*,*,*,*
1A4H	PT4	-	-	-			PT4.2	PT4.1	PT4.0	xxxx xxxx	uuuu uuuu	*,*,*,*,*,*,*,*
1A5H	PT4IN	-	-	-			IN3.2	IN3.1	IN3.0	xxx0 0000	uuuu uuuu	*,*,*,*,*,*,*,*
1A6H	TRISC4	-	-	-			TC4.2	TC4.1	TC4.0	xxx0 0000	uuuu uuuu	*,*,*,*,*,*,*,*
1A7H	PT4PU	-	-	-			PU4.2	PU4.1	PU4.0	xxx0 0000	uuuu uuuu	*,*,*,*,*,*,*,*
1A8H	PT6	PT6.7	PT6.6	PT6.5	PT6.4	PT6.3	PT6.2	PT6.1	PT6.0	xxxx xxxx	uuuu uuuu	*,*,*,*,*,*,*,*
1A9H	PT6IN	IN6.7	IN6.6	IN6.5	IN6.4	IN6.3	IN6.2	IN6.1	IN6.0	0000 xxxx	uuuu uuuu	*,*,*,*,*,*,*,*
1AAH	TRISC6	TC6.7	TC6.6	TC6.5	TC6.4	TC6.3	TC6.2	TC6.1	TC6.0	0000 xxxx	uuuu uuuu	*,*,*,*,*,*,*,*
1ABH	PT6PU	PU6.7	PU6.6	PU6.5	PU6.4	PU6.3	PU6.2	PU6.1	PU6.0	0000 xxxx	uuuu uuuu	*,*,*,*,*,*,*,*
1ACH	PT7	PT7.7	PT7.6	PT7.5	PT7.4	PT7.3	PT7.2	PT7.1	PT7.0	xxxx xxxx	uuuu uuuu	*,*,*,*,*,*,*,*
1ADH	PT7IN	IN7.7	IN7.6	IN7.5	IN7.4	IN7.3	IN7.2	IN7.1	IN7.0	0000 0000	uuuu uuuu	*,*,*,*,*,*,*,*
1AEH	TRISC7	TC7.7	TC7.6	TC7.5	TC7.4	TC7.3	TC7.2	TC7.1	TC7.0	0000 0000	uuuu uuuu	*,*,*,*,*,*,*,*
1AFH	PT7PU	PU7.7	PU7.6	PU7.5	PU7.4	PU7.3	PU7.2	PU7.1	PU7.0	0000 0000	uuuu uuuu	*,*,*,*,*,*,*,*

表 5-3 資料記憶體列表(續)

"-"no use,"*"read/write,"w"write,"r"read,"r0"only read 0,"r1"only read 1,"w0"only write 0,"w1"only write 1

"$"for event status,"."unimplemented bit,"x"unknown,"u"unchanged,"d"depends on condition

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	ARST	IRST	R/W
1B0H	PT8	PT8.7	PT8.6	PT8.5	PT8.4	PT8.3	PT8.2	PT8.1	PT8.0	xxxx xxxx	uuuu uuuu	*,*,*,*,*,*,*,*
1B1H	PT8IN	IN8.7	IN8.6	IN8.5	IN8.4	IN8.3	IN8.2	IN8.1	IN8.0	0000 0000	uuuu uuuu	*,*,*,*,*,*,*,*
1B2H	TRISC8	TC8.7	TC8.6	TC8.5	TC8.4	TC8.3	TC8.2	TC8.1	TC8.0	0000 0000	uuuu uuuu	*,*,*,*,*,*,*,*
1B3H	PT8PU	PU8.7	PU8.6	PU8.5	PU8.4	PU8.3	PU8.2	PU8.1	PU8.0	0000 0000	uuuu uuuu	*,*,*,*,*,*,*,*
1B4H	PT9	PT9.7	PT9.6	PT9.5	PT9.4	PT9.3	PT9.2	PT9.1	PT9.0	xxxx xxxx	uuuu uuuu	*,*,*,*,*,*,*,*
1B5H	PT9IN	IN9.7	IN9.6	IN9.5	IN9.4	IN9.3	IN9.2	IN9.1	IN9.0	0000 0000	uuuu uuuu	*,*,*,*,*,*,*,*
1B6H	TRISC9	TC9.7	TC9.6	TC9.5	TC9.4	TC9.3	TC9.2	TC9.1	TC9.0	0000 0000	uuuu uuuu	*,*,*,*,*,*,*,*
1B7H	PT9PU	PU9.7	PU9.6	PU9.5	PU9.4	PU9.3	PU9.2	PU9.1	PU9.0	0000 0000	uuuu uuuu	*,*,*,*,*,*,*,*
1B8H	PT10	PT10.7	PT10.6	PT10.5	PT10.4	PT10.3	PT10.2	PT10.1	PT10.0	xxxx xxxx	uuuu uuuu	*,*,*,*,*,*,*,*
1B9H	PT10IN	IN10.7	IN10.6	IN10.5	IN10.4	IN10.3	IN10.2	IN10.1	IN10.0	0000 0000	uuuu uuuu	*,*,*,*,*,*,*,*
1BAH	TRISC10	TC10.7	TC10.6	TC10.5	TC10.4	TC10.3	TC10.2	TC10.1	TC10.0	0000 0000	uuuu uuuu	*,*,*,*,*,*,*,*
1BBH	PT10PU	PU10.7	PU10.6	PU10.5	PU10.4	PU10.3	PU10.2	PU10.1	PU10.0	0000 0000	uuuu uuuu	*,*,*,*,*,*,*,*
1C0H	SSPCN0	ENSSP	CKP	CKE	SMP	-	-	SSPM[1:0]		0000 ..00	uuuu ..uu	*,*,*,*-,-,*,*
1C1H	SSPSTA0	SSPBY	SSPOV	-	-	-	-	-	BF	00.. ...0	uu.. ...u	*,*,-,- -,-,-,*
1C2H	SSPBUF0	SSP Receive/Transmit Buffer Register								xxxx xxxx	uuuu uuuu	*,*,*,*,*,*,*,*
1C3H	CFG0	-	-	-	-	-	GCRst	ENI2CT	ENI2C	0000 0000	.... .uuu	-,-,-,- -,*,*,*
1C4H	ACT0	SLAVE	-	-	I2CER	START	STOP	I2CINT	ACK	0000 0000	uuuu uuuu	*,*,*,*,*,*,*,*
1C5H	STA0	MACTF	SACTF	RDBF	RWF	DFF	ACKF	GCF	ARBF	0001 0000	uuuu uuuu	*,*,*,*,*,*,*,*
1C6H	CRG0	CRG[7:0]								0000 0000	uuuu uuuu	*,*,*,*,*,*,*,*
1C7H	TOC0	I2CTF	DI2C[2:0]			I2CTLT[3:0]				0000 0000	uuuu uuuu	*,*,*,*,*,*,*,*
1C8H	RDB0	RDB[7:1]							RDB[0]	xxxx xxxx	uuuu uuuu	*,*,*,*,*,*,*,*
1C9H	TDB0	TDB0[7:1]							TDB0[0]	xxxx xxxx	uuuu uuuu	*,*,*,*,*,*,*,*
1CAH	SID0	SID0[7:1],The corresponding address of the 7-bit mode							SID0V[0]	0000 0000	uuuu uuuu	*,*,*,*,*,*,*,*
1CBH	UR0CN	ENSP	ENTX	TX9	TX9D	PARITY	-	-	WUE	0000 0..0	uuuu u..u	*,*,*,*,-,-,*
1CCH	UR0STA	-	RC9D	PERR	FERR	OERR	RCIDL	TRMT	ABDOVF	.000 0010	.uuu uuuu	-,r,r,r r,r,r,rw0
1CDH	BA0CN	-	-	-	-	ENCR	RC9	ENADD	ENABD	 0000	.... uuuu	-,-,-,- *,*,*,*
1CEH	BG0RH	-	-	-	Baud Rate Generator Register High Byte					...x xxxx	...u uuuu	-,-,-,*,*,*,*,*
1CFH	BG0RL	Baud Rate Generator Register Low Byte								xxxx xxxx	uuuu uuuu	*,*,*,*,*,*,*,*
1D0H	TX0R	UART Transmit Register								xxxx xxxx	uuuu uuuu	*,*,*,*,*,*,*,*
1D1H	RC0REG	UART Receive Register								xxxx xxxx	uuuu uuuu	r,r,r,r r,r,r,r
1D2H	TB1Flag		PWM7A	PWM6A	PWM5A	PWM4A	PWM3A	PWM2A	PWM1A	.000 0000	.uuu uuuu	-,r,r,r r,r,r,r
1D3H	TB1CN0	ENTB1	TB1M[1:0]		TB1RT[1:0]		TB1CL	PWMO1	PWMO0	0000 0000	uuuu u0uu	*,*,*,* *,rw1,*,*
1D4H	TB1CN1	PA1IV	PWMA1[2:0]			PA0IV	PWMA0[2:0]			0000 0000	uuuu uuuu	*,*,*,*,*,*,*,*
1D5H	TB1RH	TimerB1 counter Register [15:8]								xxxx xxxx	uuuu uuuu	r,r,r,r r,r,r,r
1D6H	TB1RL	TimerB1 counter Register [7:0]								xxxx xxxx	uuuu uuuu	r,r,r,r r,r,r,r
1D7H	TB1C0H	TimerB1 counter Condition Register [15:8]								xxxx xxxx	uuuu uuuu	*,*,*,*,*,*,*,*
1D8H	TB1C0L	TimerB1 counter Condition Register [7:0]								xxxx xxxx	uuuu uuuu	*,*,*,*,*,*,*,*
1D9H	TB1C1H	TimerB1 counter Condition Register [15:8]								xxxx xxxx	uuuu uuuu	*,*,*,*,*,*,*,*
1DAH	TB1C1L	TimerB1 counter Condition Register [7:0]								xxxx xxxx	uuuu uuuu	*,*,*,*,*,*,*,*
1DBH	TB1C2H	TimerB1 counter Condition Register [15:8]								xxxx xxxx	uuuu uuuu	*,*,*,*,*,*,*,*
1DCH	TB1C2L	TimerB1 counter Condition Register [7:0]								xxxx xxxx	uuuu uuuu	*,*,*,*,*,*,*,*
1DDH	TB1CN2	-	TC1S[1:0]		-	-	-	-	-	0000 0000	uuuu uuuu	uuuu uuuu
1DEH	DGCON1	-	-	-	DGRST	DGDiv[2:0]			DGEN	0000 0000	uuuu uuuu	*,*,*,*,*,*,*,*
1DFH	DGCON2	-	-	DGRP[5:0]						0000 0000	uuuu uuuu	*,*,*,*,*,*,*,*
1E0H	DACCN0	DANS[1:0]		DAPS[1:0]		-	-	DALH	ENDA	0000 0000	uuuu uuuu	*,*,*,*,*,*,*,*
1E1H	DACCN1	DABIT[7:0]								0000 0000	uuuu uuuu	*,*,*,*,*,*,*,*
1E2H	FILTER	FreSpect		Frebit	ENSpect	-	-	-	-	0000 0000	uuuu uuuu	*,*,*,*,*,*,*,*
080h ~ 0FFh		SRAM as 128Byte								uuuu uuuu	uuuu uuuu	*,*,*,*,*,*,*,*
100h ~ 17Fh		SRAM as 128Byte								uuuu uuuu	uuuu uuuu	*,*,*,*,*,*,*,*
200h ~ 2FFh		SRAM as 256Byte								uuuu uuuu	uuuu uuuu	*,*,*,*,*,*,*,*
300h ~ 3FFh		SRAM as 256Byte, 300h~33Fh set for hardware sinewave first.								uuuu uuuu	uuuu uuuu	*,*,*,*,*,*,*,*
400h ~ 4FFh		SRAM as 256Byte								uuuu uuuu	uuuu uuuu	*,*,*,*,*,*,*,*

表 5-4 資料記憶體列表(續)

6. 電氣特性

Absolute Maximum Ratings:

Absolute maximum ratings over operating free-air temperature (unless otherwise noted)

Voltage applied at V_{DD} to V_{SS} . . . . −0.2 V to 6.0 V

Voltage applied to any pin . . . . −0.2 V to V_{DD} + 0.3 V

Voltage applied to RST/VPP pin . . . . −0.2 V to 8.75 V

Diode current at any device terminal . . . . . ±2 mA

Storage temperature, Tstg: (unprogrammed device) . . . . −55℃ to 125℃

(programmed device) . . . . −40℃ to 85℃

Total power dissipation. 0.5W

Maximum output current sink by any I/O pin. 20mA

6.1. Recommended operating conditions

T_A = -40℃ ~ 85℃,unless otherwise noted

Sym.	Parameter		Test Conditions		Min.	Typ.	Max.	unit
V_{DD}	Supply Voltage		All digital peripherals and CPU V_{DD} = 2.2V~5.5V, Frequency<=9.6MHz, V_{DD} = 3.6V~5.5V, Frequency<=16MHz,		2.2		5.5	V
V_{DDA}	Supply Voltage		Analog peripherals		2.4		4.5	
V_{SS}	Supply Voltage				0		0	
XT	External Oscillator Frequency	Watch crystal	V_{DD} = 2.2V~5.5V, ENXT[0]=1	XTS[1:0]=0x	32768			Hz
		Ceramic resonator, Crystal		XTS[1:0]=10	450K		4M	
				XTS[1:0]=11	1M		8M	
		Ceramic resonator, Crystal	V_{DD} = 3.6V~5.5V, ENXT[0]=1	XTS[1:0]=11	450K		16M	

6.2. Internal RC Oscillator

T_A = 25℃,VDD = 3.0V,unless otherwise noted

Sym.	Parameter	Test Conditions	Min.	Typ.	Max.	unit
HAO	High Speed Oscillator frequency	ENHAO[0]=1, HAOM[1:0]=01	-20%	4.9152	+20%	MHz
		ENHAO[0]=1, HAOM[1:0]=11	-20%	9.8304	+20%	
LPO	Low Power Oscillator frequency	VDD supply voltage be enable LPO	-20%	14.5	+20%	kHz

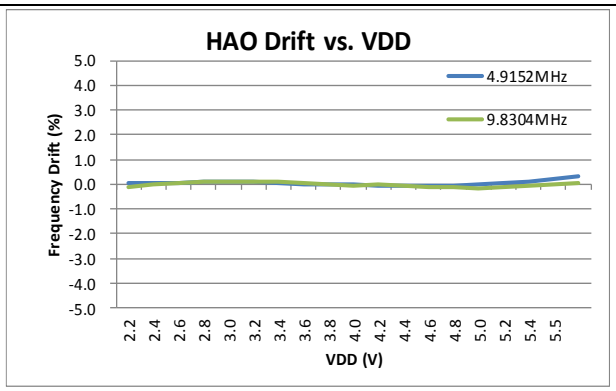


Figure 6.2-1 HAO vs. VDD

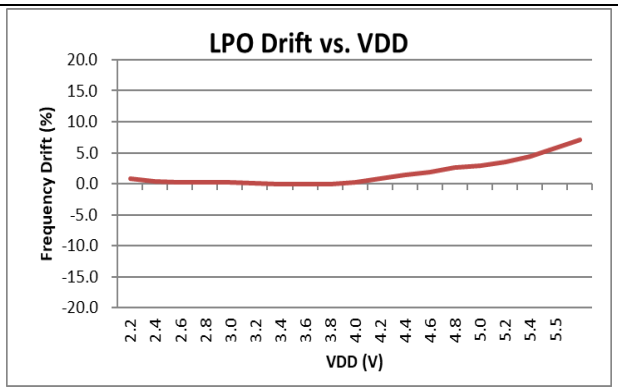


Figure 6.2-2 LPO vs. VDD

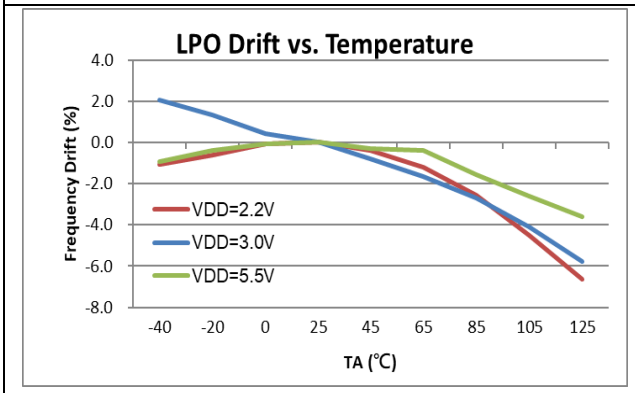


Figure 6.2-3 LPO vs. Temperature

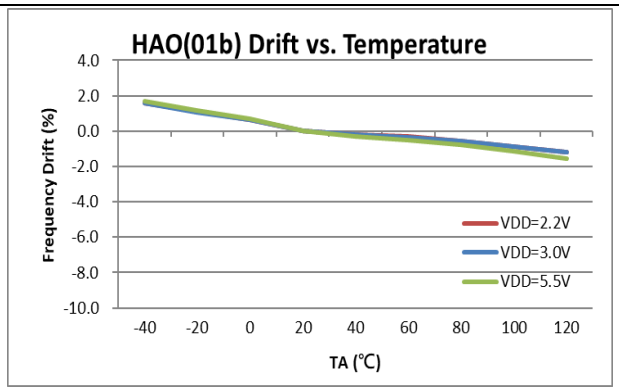


Figure 6.2-4 HAO(4.9152MHz) vs. Temperature

6.3. Supply current into VDD excluding peripherals current

T_A = 25℃,V_{DD} = 3.0V,OSC_LPO = 14.5KHz,unless otherwise noted

Sym.	Parameter	Test Conditions	Min.	Typ.	Max.	unit
I_{AM1}	Active mode 1	OSC_CY = off, OSC_HAO =4.9152MHz, CPU_CK =4.9152MHz		550	800	uA
I_{AM2}	Active mode 2	OSC_CY = off, OSC_HAO =4.9152MHz, CPU_CK = 4.9152MHz/2		500	700	uA
I_{LP1}	Low Power 1	OSC_CY = off, OSC_HAO = off, CPU_CK = LPO,		2	5	uA
I_{LP2}	Low Power 2	OSC_CY = off, OSC_HAO = off, CPU_CK = LPO, Idle state		1.0	2.5	uA
I_{LP3}	Low Power 3	OSC_CY = off, OSC_HAO = off, CPU_CK = off, Sleep state		0.25	1.0	uA

OSC_CY：External Oscillator frequency.

OSC_HAO：Internal High Accuracy Oscillator frequency.

CPU_CK：CPU core work frequency.

T_A = 25℃,V_{DD} = 5.5V,OSC_LPO = 14.5KHz,unless otherwise noted

Sym.	Parameter	Test Conditions	Min.	Typ.	Max.	unit
I_{AM1}	Active mode 1	OSC_CY = off, OSC_HAO =4.9152MHz, CPU_CK =4.9152MHz		1000	1500	uA
I_{AM2}	Active mode 2	OSC_CY = off, OSC_HAO =4.9152MHz, CPU_CK = 4.9152MHz/2		900	1300	uA
I_{LP1}	Low Power 1	OSC_CY = off, OSC_HAO = off, CPU_CK = LPO,		4	10	uA
I_{LP2}	Low Power 2	OSC_CY = off, OSC_HAO = off, CPU_CK = LPO, Idle state		2.5	5	uA
I_{LP3}	Low Power 3	OSC_CY = off, OSC_HAO = off, CPU_CK = off, Sleep state		0.4	2	uA

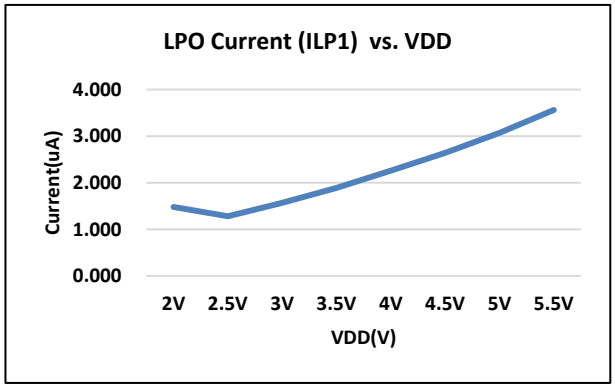


Figure 6.3-1 I_{AM1} vs. VDD

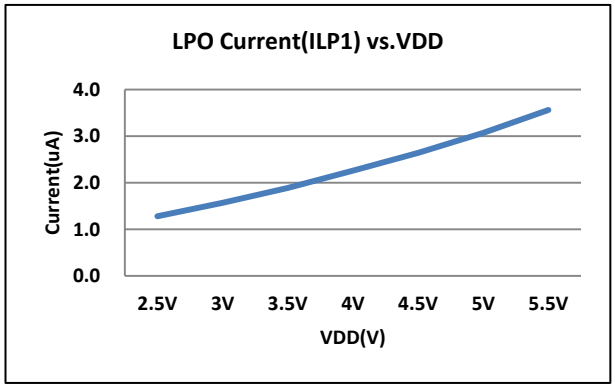


Figure 6.3-2 I_{LP1} vs. VDD

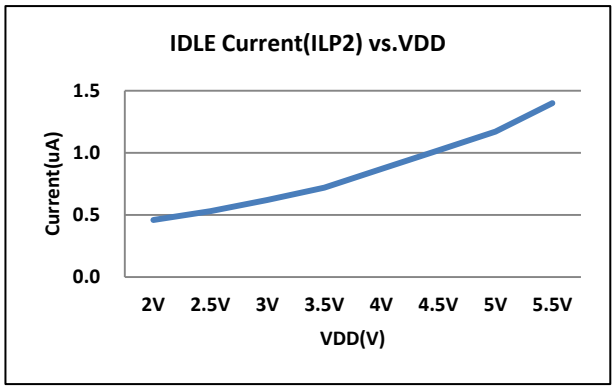


Figure 6.3-3 I_{LP2} vs. VDD

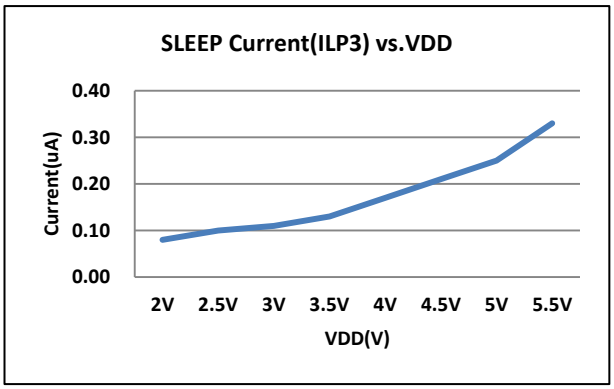


Figure 6.3-4 I_{LP3} vs. VDD

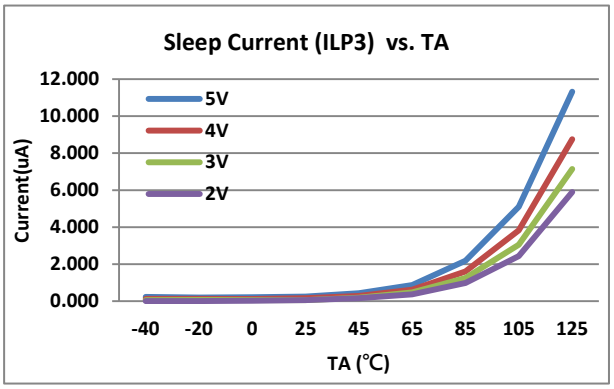


Figure 6.3-2 I_{LP3} vs. Temperature

6.4. Port 1~4,6~10

T_A = 25℃,VDD = 3.0V,unless otherwise noted

Sym.	Parameter	Test Conditions	Min.	Typ.	Max.	unit
Input voltage and Schmitt trigger and leakage current and timing						
V_{IH}	High-Level input voltage				0.7*VDD	V
V_{IL}	Low-Level input voltage		0.3*VDD			
V_{hys}	Input Voltage hysteresis(V_{IH} - V_{IL})			0.3*VDD		V
I_{LKG}	Leakage Current				0.1	uA
R_{PU}	Port pull high resistance			60		kΩ
Output voltage and current and frequency						
V_{OH}	High-level output voltage	VDD<4V, I_{OH}=10mA,	VDD -0.4			V
		VDD>=4V, I_{OH}=15mA,	VDD -0.4			
V_{OL}	Low-level output voltage	VDD<4V, I_{OL}=-10mA			VSS +0.4	
		VDD>=4V, I_{OL}=-15mA			VSS +0.4	

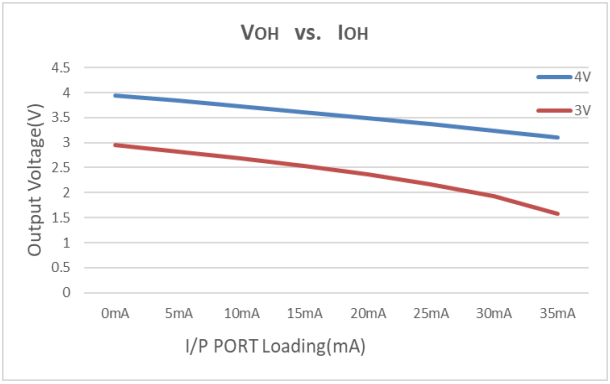


Figure 6.4-1 V_{OH} vs. I_{OH}

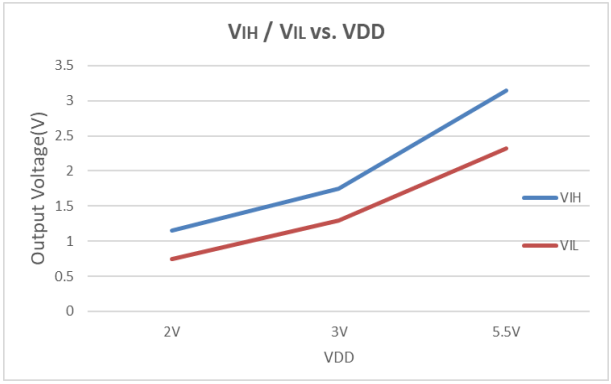


Figure 6.4-2 V_{IH}/V_{IL} vs. VDD

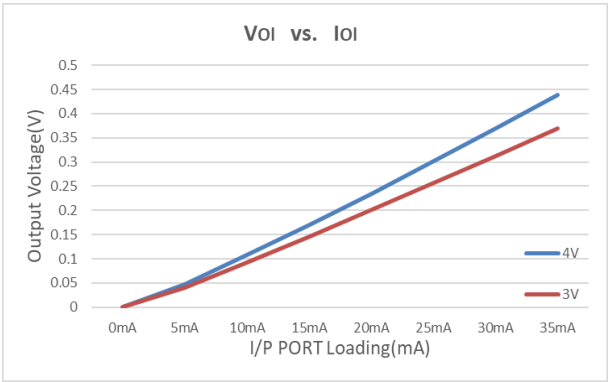


Figure 6.4-3 V_{OL} vs. I_{OL}

6.5. Reset(Brownout)

T_A = 25℃,VDD = 3.0V,unless otherwise noted

Sym.	Parameter	Test Conditions		Min.	Typ.	Max.	unit
BOR1	Pulse length needed to accepted reset internally, t_{d-LVR1}			2			us
	V_{DD} Start Voltage to accepted reset internally (L➔H),V_{HYS1}			1.0	1.35	1.65	V
	BOR1 current, I_{BOR1}				0.2	0.5	uA
	Temperature Drift				5		%
BOR2	Pulse length needed to accepted reset internally, t_{d-LVR2}			2			us
	V_{DD} Start Voltage to accepted reset internally (L➔H),V_{HYS2}, and BOR_TH[2:0]:		000b	-8%	1.73	+8%	V
			001b	-8%	2.0	+8%	
			010b	-8%	2.22	+8%	
			011b	-8%	2.5	+8%	
			100b	-8%	2.72	+8%	
			101b	-8%	3.0	+8%	
			110b	-10%	3.63	+10%	
			111b	-10%	4.0	+10%	
	V_{DD} Start Voltage to accepted reset internally (H➔L),V_{LVR2}, and BOR_TH[2:0]:		000b	-8%	1.67	+8%	V
			001b	-8%	1.96	+8%	
			010b	-8%	2.17	+8%	
			011b	-8%	2.44	+8%	
			100b	-8%	2.69	+8%	
			101b	-8%	2.96	+8%	
			110b	-10%	3.58	+10%	
			111b	-10%	3.94	+10%	
	Hysteresis, $V_{HYS2-LVR2}$			25	60	90	mV
	BOR2 current, I_{BOR2}				25	35	uA
	Temperature Drift				3	5	%
RST	Pulse length needed as RST/VPP pin to accepted reset internally, t_{d-RST}			2			us
	Input Voltage to accepted reset voltage				1.1		V
	Reset release voltage				2		V

BOR1/BOR2：Brownout Reset 1/2
LVR：Low Voltage Reset of BOR
RST：External Reset pin

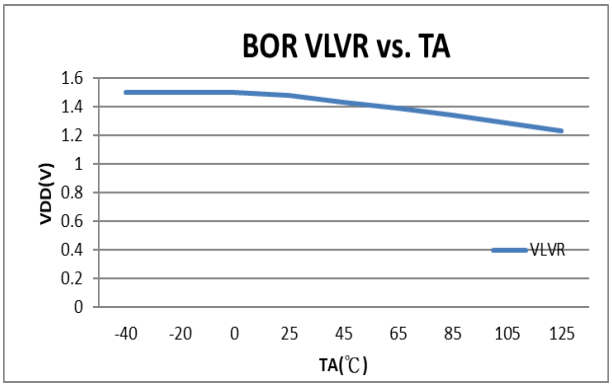


Figure 6.5-1 BOR vs. Temperature

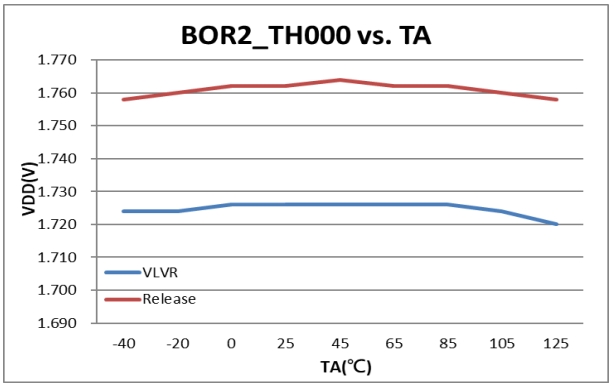


Figure 6.5-2 BOR2 vs. Temperature

6.6. Multi-function Comparator

T_A = 25℃,V_{DD} = 3.0V, unless otherwise noted.

Sym.	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
I_{MC}	Operation supply current	ENCMP[0]=1, CMPHS[0]=1b		5		uA
	Low Power Mode	ENCMP[0]=1, CMPHS [0]=0b		1		
V_{IC}	Common-mode input voltage		0		V_{DD}-1	V
V_{OS}	Offset voltage		-5		5	mV
V_{hys}	Input hysteresis		0	0.7	1.5	mV
V_{accy}	Reference Voltage	ENLDO[0]=1b, CPPS[1:0]=11b, VRSEL[0]=1b	1.15	1.2	1.25	V
	Temperature Drift			50		ppm/℃
	VDD Voltage drift			±0.2		%/V
I_R	Multi-node resistor current	CPRL[0]=0b		10		uA
		CPRL[0]=1b		30		
	ENLDO[0]=1b,CPPS[1:0]=11b,CPRH[1:0]=01b,CPRL[0]=0b.	CPDA[4:0]=00011b	-5%	3.89	5%	V
		CPDA[4:0]=00100b		3.73		
		CPDA[4:0]=00101b		3.58		
		CPDA[4:0]=00110b		3.44		
		CPDA[4:0]=00111b		3.31		
		CPDA[4:0]=01000b		3.19		
		CPDA[4:0]=01001b		3.08		
		CPDA[4:0]=01010b		2.98		
		CPDA[4:0]=01011b		2.88		
		CPDA[4:0]=01100b		2.79		
		CPDA[4:0]=01101b		2.71		
		CPDA[4:0]=01110b		2.63		
		CPDA[4:0]=01111b		2.55		
		CPDA[4:0]=10000b		2.48		
		CPDA[4:0]=10001b		2.42		
		CPDA[4:0]=10010b		2.35		
		CPDA[4:0]=10011b		2.29		
		CPDA[4:0]=10100b		2.24		
	CPDA[4:0]=00011b~10100b					

6.7. Power System

T_A = 25℃,VDD = 3.0V,unless otherwise noted

Sym.	Parameter	Test Conditions		Min.	Typ.	Max.	unit
VDDA	VDDA operation current, I_{VDDA}	I_L = 0mA	LDOC[2:0]=000b		30		uA
	Select VDDA output voltage	I_L = 0.1mA, VDD≧VDDA+0.25V ENPUMP=1b	LDOC [2:0]=000b	-5%	2.4	+5%	V
			LDOC [2:0]=001b		2.6		V
			LDOC [2:0]=010b		2.9		V
			LDOC [2:0]=011b		3.3		V
			LDOC [2:0]=100b		3.6		V
			LDOC [2:0]=101b		4.0		V
			LDOC [2:0]=110b		4.5		V
	Dropout voltage	VDD=2.9V I_L = 10mA	LDOC [2:0]=010b		200		mV
	Temperature drift	LDOC [2:0]=000b I_L = 0.1mA	T_A=-40℃~85℃		50		PPM/℃
	V_{DD} Voltage drift	LDOC [2:0]=000b	V_{DD}=2.2V~5.5V		±0.2		%/V
AGND	AGND operation current, I_{Agnd}	SAGND≠000b ENPUMP=1b VGGS=1b	I_L = 0mA		450		uA
	Output voltage ,V_{Agnd}	SAGND=001b	I_L = 10uA	-5%	VDDA*0.3	-5%	
		SAGND=010b	I_L = 10uA	-5%	VDDA*0.1	-5%	
		SAGND=011b	I_L = 10uA	-5%	VDDA*0.5	-5%	
		SAGND=100b	I_L = 10uA	-5%	VDDA*0.4	-5%	
REFO	V(REFO,VSS)		I_L = 10uA	-3%	1,2	-3%	V
	Temperature drift		T_A=-40℃~85℃		100		PPM/℃
	RMS Noise				60		uVrms

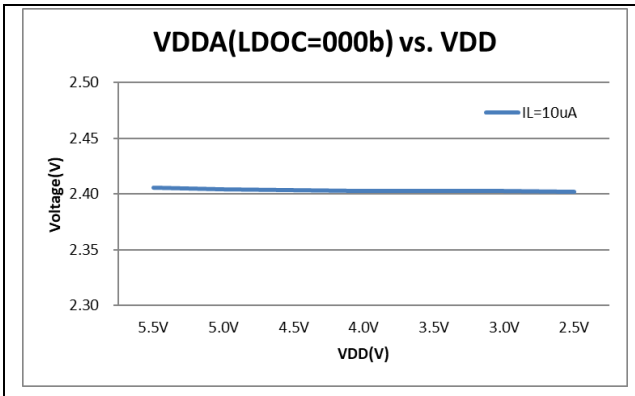


Figure 6.6-1 VDDA(000b) vs. VDD

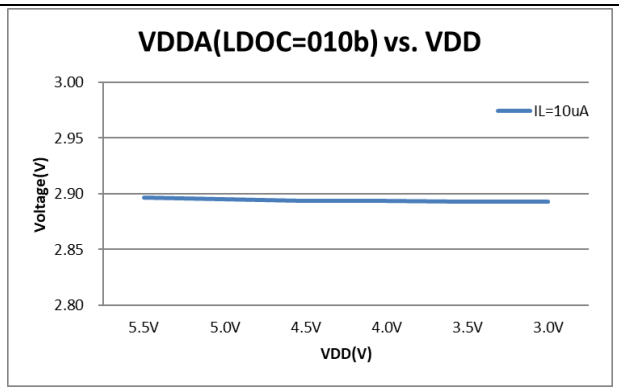


Figure 6.6-2 VDDA(010b) vs. VDD

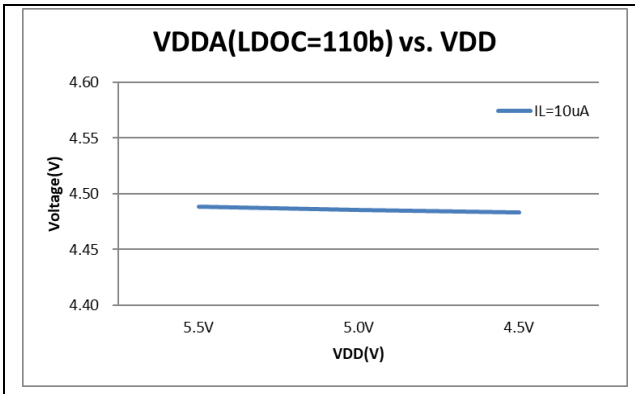


Figure 6.6-3 VDDA(110b) vs. VDD

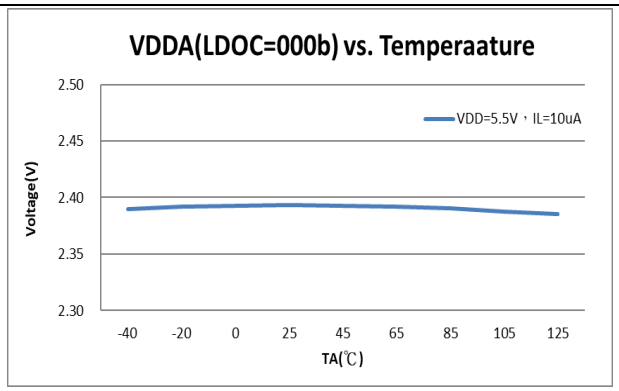


Figure 6.6-4 VDDA(000b) vs. Temperature

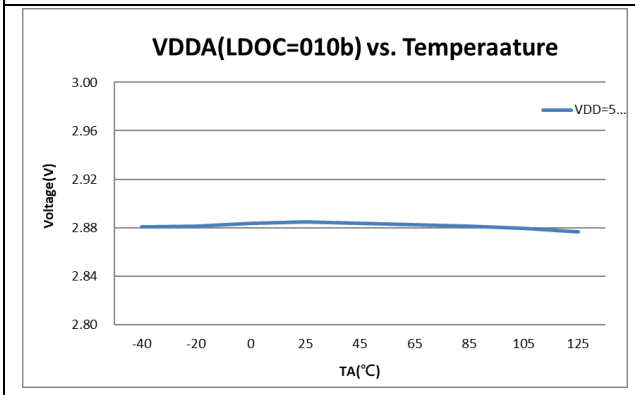


Figure 6.6-5 VDDA(010b) vs. Temperature

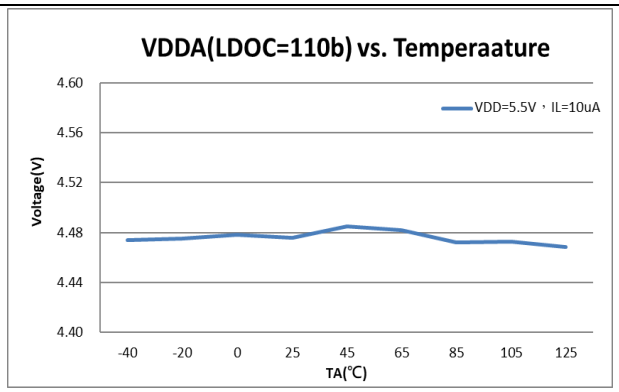


Figure 6.6-6 VDDA(110b) vs. Temperature

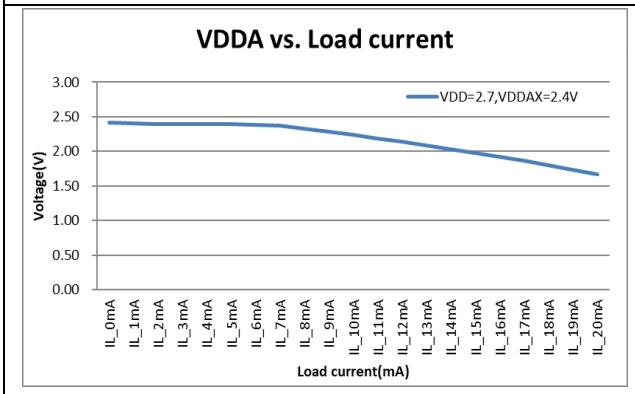


Figure 6.6-7 VDDA vs. Load current

6.8. LCD

T_A = 25℃,V_{DD} = 3.3V, C_{VLCD} =4.7uF,unless otherwise noted.

Sym.	Parameter	Test Conditions		Min.	Typ.	Max.	unit
I_{LCD}	Operation supply current with output buffer.(all segment turn on, No load)	ENLCP[0]=1	V_{DD} = 3.0V		8		uA
V_{LCD}	Supply Voltage at VLCD pin	ENLCP [0]=0		2.4		5	V
	Embedded Charge Pump output voltage at VLCD pin	V_{DD} = 3.3V, ENLCP [0]=1, C_{VLCD} =4.7uF	LCDV[2:0]=111b	-10%	2.45	+10%	V
			LCDV[2:0]=110b	-10%	2.70	+10%	
			LCDV[2:0]=101b	-10%	2.85	+10%	
			LCDV[2:0]=100b	-10%	3.10	+10%	
			LCDV[2:0]=011b	-10%	3.30	+10%	
			LCDV[2:0]=010b	-10%	4.10	+10%	
			LCDV[2:0]=001b (VDD>2.4V mode)	-10%	4.55	+10%	
			LCDV[2:0]=000b (VDD>2.75V)	-10%	5.1	+10%	
	VDD Voltage drift	ENLCP [0]=1, C_{VLCD} =4.7uF, LCDV[2:0]>010b,VDD=2.2V~ 5.5V; LCDV[2:0]=001b,VDD>2.4V; LCDV[2:0]=000b,VDD>2.75V;			4		%/V
Z_{LCD}	Output impedance with LCD buffer	f_{LCD} =128Hz,VLCD=3.05V			10		kΩ

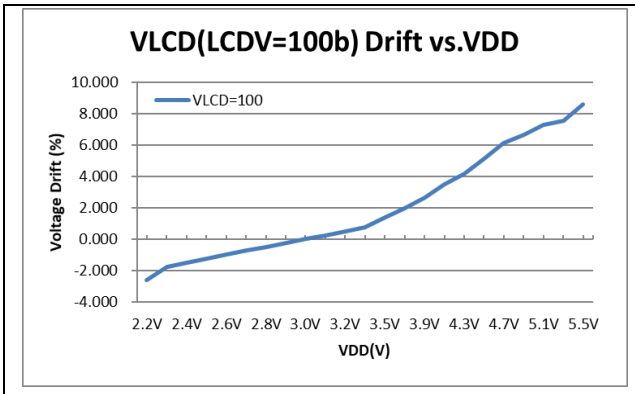


Figure 6.7-1 VLCD(LCDV=100b) vs. VDD

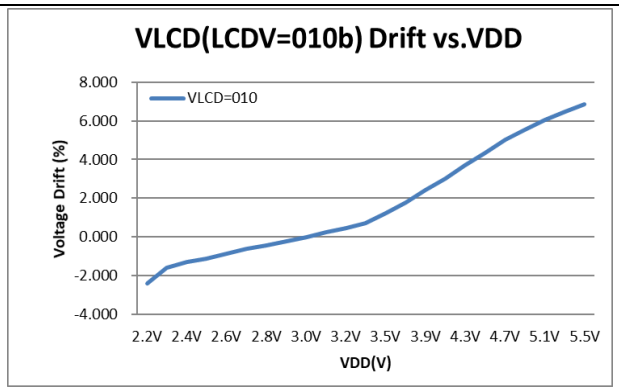


Figure 6.7-2 VLCD(LCDV=010b) vs. VDD

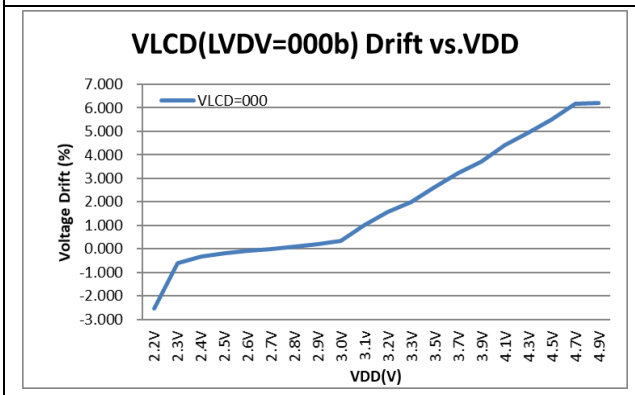
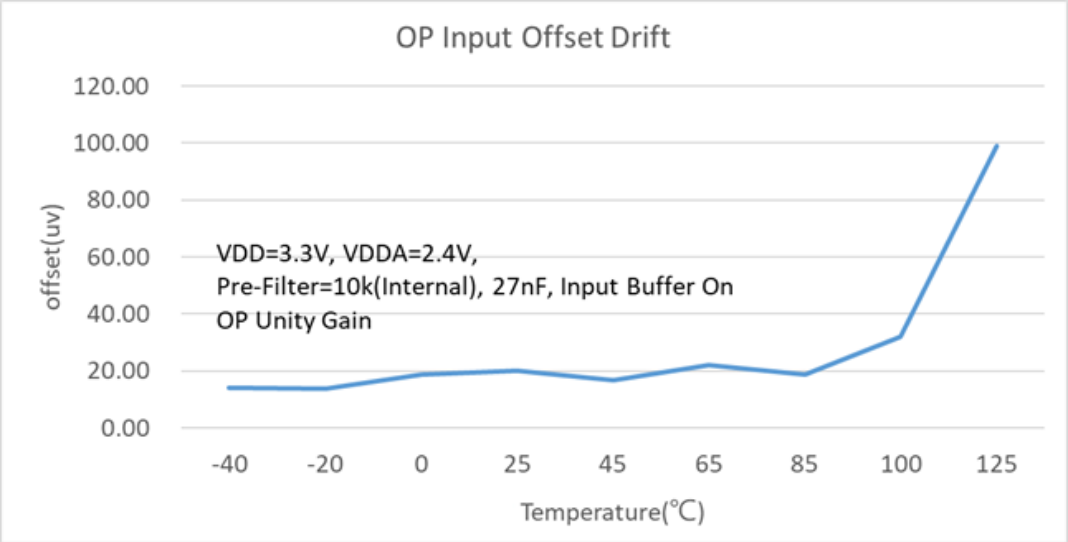


Figure 6.7-3 VLCD(LCDV=000b) vs. VDD

6.9. OPAMP

TA = 25℃,VDD = 3.3V, VDDA=2.4V, AGND=0.3VDDA, Input buffer on unless otherwise noted

Sym.	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V_{os-op}	Input offset voltage	Pre-Filter=10K(Inside) / 27nF(Outside) OP Unity Gain, HS=1b,OP1CHOP=00b			800	uV
V_{os-td}	OP Input offset temperature drift	TA=-40℃ ~ 85℃		0.5		uV/℃
CMVR	Common-mode voltage input range		VSS+0.1		VDDA - 1.1	V



6.10. ΣADC, Power Supply and recommended operating conditions

T_A = 25℃,VDD = 3.0V, VDDA=2.4V,unless otherwise noted

Sym.	Parameter	Test Conditions		Min.	Typ.	Max.	unit
V_{SD18}	Supply Voltage at VDDA	ENLDO[0]=0		2.4		5.5	V
f_{SD18}	Modulator sample frequency, ADC_CK				0.5		MHz
	Over Sample Ratio, OSR			32		61440	
Eos	Input offset voltage	Chopper on OSR=61440 Input Buffer On Pre-Filter:10k, 27nF	Input gain=1, reference gain=1		-3		uV
			Input gain=8, reference gain=1		-3		
Rev	Roll-over error voltage	Chopper on OSR=61440	Input gain=1, reference gain=1				uV
			Input gain=8, reference gain=1				
Vrms	Input RMS Noise	Chopper on, OSR=61440, input gain=1.0 reference gain=1			.3.5		uV
		Chopper on, OSR=61440, input gain=8.0 reference gain=1			1.2		
		Chopper off, OSR=32, input gain=1.0 reference gain=1, ADC_CK=1MHz			750		
		Chopper off, OSR=32, input gain=8.0 reference gain=1, ADC_CK=1MHz			330		
NM	Normal Rejection ratio	Chopper On OSR=61440 ADCLK=1	Input gain=1.0, reference gain=1. Vin=200mVrms 50/60Hz		60		dB
AC_{bw}	AC Measurement Bandwidth	OSR=32, LPFBW=2048 Without Voltage Dividers	0.5% error	20		4k	Hz
			3dB				
			Square wave, 0.5% error			0.3k	
			Triangle wave, 0.5% error				

	A/D Clock=1MHz	ENOB(RMS) with OSR/GAIN at A/D Clock=0.5MHz, VDD=3.3V, VDDA=2.4V, AGND=0.3VDDA, VREF=1.2,Vin=Ext.Short, Chopper Off;						
OSR	32	64	128	256	7680	15360	30720	61140
Output rate(Hz) / Gain	31250	7813	3906	1953	65	33	16	8
0.5	11.97	13.74	14.8	15.43	17.87	18.29	18.67	18.89
1	11.66	13.56	14.76	15.65	17.77	18.24	18.49	18.73
2	11.23	12.43	14.85	15.18	17.56	17.88	18.21	18.32
4	10.61	12.67	14.52	15.03	17.14	17.5	17.47	17.68
8	9.82	11.92	14.1	14.57	16.42	16.66	16.88	16.67
	A/D Clock=1MHz	RMS Noise(uV) with OSR/GAIN at A/D Clock=0.5MHz, VDD=3.3V, VDDA=2.4V, AGND=0.3VDDA, VREF=1.2,Vin=Ext.Short, Chopper Off;						
OSR	32	64	128	256	7680	15360	30720	61140
Output rate(Hz) / Gain	31250	7813	3906	1953	65	33	16	8
0.5	1197.70	349.75	168.30	108.85	20.02	14.99	11.49	9.87
1	744.08	198.44	86.65	46.74	10.77	7.75	6.53	5.52
2	499.79	217.13	40.69	32.42	6.19	4.96	3.95	3.67
4	383.17	92.21	25.53	17.98	4.15	3.25	3.29	2.85
8	331.64	77.68	17.12	12.37	3.43	2.89	2.48	2.88

ENOB(RMS) with OSR/GAIN at A/D Clock=0.5MHz, VDD=3.3V, VDDA=2.4V, AGND=0.3VDDA, VREF=1.2,Vin=Ext.Short, Chopper On;							
OSR	64	128	256	7680	15360	30720	61140
Output rate(Hz) / Gain	3906	1953	977	33	16	8	4
0.5	14.75	15.36	15.9	18.27	18.65	19.06	19.43
1	14.69	15.32	15.91	18.24	18.65	19.06	19.41
2	14.62	15.31	15.84	18.27	18.55	18.9	19.16
4	14.51	15.11	15.66	17.91	18.23	18.52	18.73
8	14.19	14.77	15.18	17.29	17.61	17.84	17.9
RMS Noise(uV) with OSR/GAIN at A/D Clock=0.5MHz, VDD=3.3V, VDDA=2.4V, AGND=0.3VDDA, VREF=1.2,Vin=Ext.Short, Chopper On;							
OSR	64	128	256	7680	15360	30720	61140
Output rate(Hz) / Gain	3906	1953	977	33	16	8	4
0.5	174.57	114.32	78.73	15.16	11.70	8.77	6.79
1	90.77	58.72	39.09	7.75	5.85	4.39	3.45
2	47.53	29.46	20.47	3.79	3.13	2.45	2.05
4	25.75	16.97	11.57	2.43	1.95	1.60	1.38
8	16.08	10.75	8.07	1.88	1.50	1.28	1.23

6.10.1. ΣADC ,Temperature Sensor

T_A = 25℃,V_{DD} = 3.0V, VDDA=2.4V,unless otherwise noted

Sym.	Parameter	Test Conditions	Min.	Typ.	Max.	unit
TC_S	Sensor temperature drift			173		uV/℃
KT	Absolute Temperature Scale 0°K			-263		℃
TC_{ERR}	One point calibrate error temperature	Calibration at 25℃ of -40℃~85℃		±2		℃

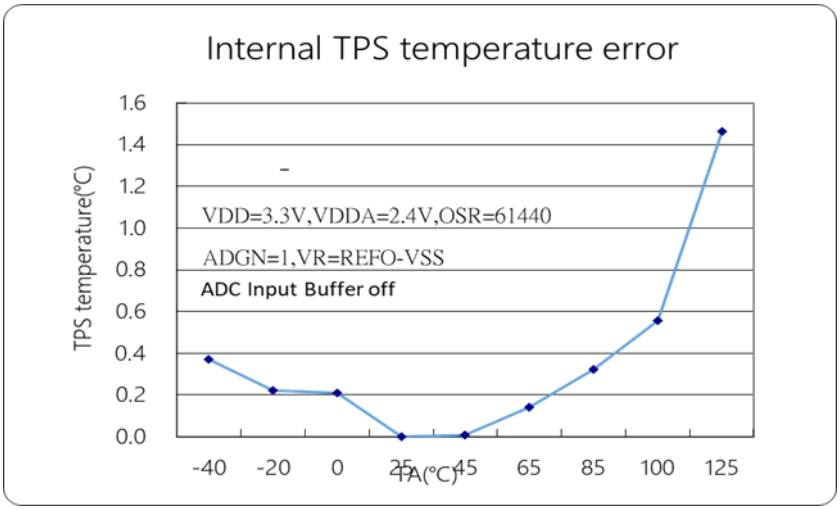


Figure 6.8-4 ADC Temperature Error

6.11. Analog input and switch performance

T_A = 25℃,V_{DD} = 3.0V, VDDA=2.4V AGND=0.5 x VDDA, unless otherwise noted

Sym.	Parameter	Test Conditions	Min.	Typ.	Max.	unit
I_{AL}	Analog Input Leakage Current	AGND=0.5 x VDDA		10	100	pA
		AGND=0.4 x VDDA		10	100	
		AGND=0.3 x VDDA		10	100	
		AGND=0.1 x VDDA		100	500	
Rsw	Switch Turn On Resistance	PS0,PS1		20		Ohm
		DS0,DS1		40		
		DS2~DS8, PS2~PS8		80		
		SS0~SS8,FS0~FS8		400		

6.12. Windows Comparator

T_A = 25℃,V_{DD} = 3.0V, VDDA=2.4V AGND=0.5 x VDDA ,unless otherwise noted

Sym.	Parameter	Test Conditions	Min.	Typ.	Max.	unit
I_{CMP}	Comparator Supply Current					uA
V_I	Comparator Input Range	CMPL	0		VDDA-0.7	V
		CMPH	0.4		VDDA	

Vos	Comparator Input Offset Voltage	CMPL , VRLCMP=AGND	5	mV
		CMPH VRHCMP=AGND	5	
Vn	Comparator Input peak to peak noise	CMPL	5	mV
		CMPH	5	
		CMPH&CMPL	10	
CMP_{BW}	Comparator Bandwidth	VRHCMP=AGNDP<2>, VRLCMP=AGNDN<2> VIN=100mVrms	1	MHz

6.13. Build-In EPROM(BIE)

T_A = 25℃,V_{DD} = 3.0V, unless otherwise noted

Sym.	Parameter	Test Conditions	Min.	Typ.	Max.	unit
V_{BIE}	Supply Voltage at VPP PIN			8.5	8.75	V
I_{BIE}	Operation supply current			3		mA
V_{SS}	Supply Voltage			0		V
When connecting to the external V_{BIE} power source to program the BIE block, users can use the instruction to program the words one by one into the BIE block.						

6.14. Build-In EPROM(BIE) Low voltage control circuit

T_A = 25℃,V_{DD} = 3.05V, unless otherwise noted

Sym.	Parameter	Test Conditions	Min.	Typ.	Max.	unit
T_O	Operation temperature range		0	25	40	℃
V_{DD}	Operation supply Voltage		2.75		5.5	V
V_{SS}	Supply Voltage			0		V
When the 2.75V low voltage programming control circuit is activated, users can program the BIE block without connecting to the external V_{BIE} power source.						

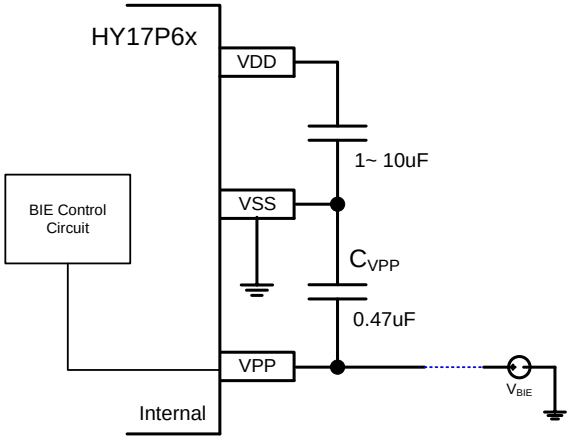


圖 6.14-1 BIE typical application 方塊圖

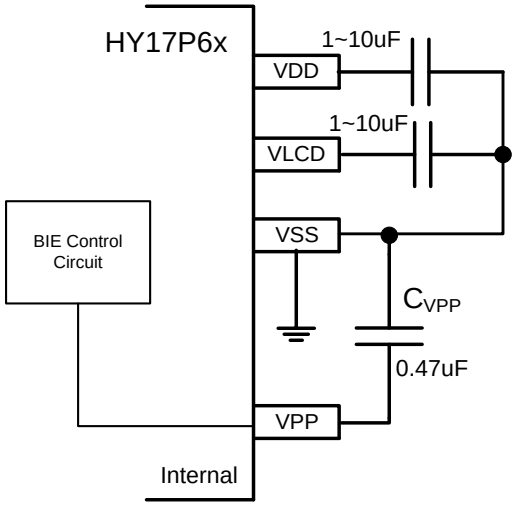


圖 6.14-2 BIE typical application use low voltage control circuit 方塊圖

7. 修訂貨資訊

下單品名 1	封裝型式	引腳數	封裝型式		程式碼	出貨包裝形式	個裝數量	材料組成	MSL3
			描述方式		編號 2				
HY17P68-D000	Die	-	D	000	000	Tray	200	Green[4]	-
HY17P68-L064	LQFP	64	L	064	000	Tray	250	Green[4]	MSL-3
HY17P68-L100	LQFP	100	L	100	000	Tray	90	Green[4]	MSL-3

[1] **產品名稱 品名封裝型式描述方式 裝型程式碼編號（空白片 / 標準品 / 代客燒錄碼）**

例如：您的 HY17P68 代客燒錄服務申請的程式碼編號為 001，且需要的產品是裸 片出貨。則下單品名為 HY17P68-D000-001。

例如：您的需求是 HY17P68 不帶程式碼的空白片且需要的產品是裸片出貨。則下單品名為 HY17P68-D000。

例如：您的需求是 HY17P68 不帶程式碼的空白片且需要的產品是封裝片 LQFP64 出貨，則下單品名為 HY17P68-L064，且需以 Tray 出貨，則除下單品名外，請特別註明出貨包裝形式為 Tray。

例如：您的 HY17P68 代客燒錄服務申請的程式碼編號為 001，而需求的產品是封裝片 LQFP64 出貨，則下單品名為 HY17P68-L064-001，且需以 Tray 出貨，則除下單品名外，請特別註明出貨包裝形式為 Tray。

[2] 程式碼編號

“式碼編號式為品名外，請為標準品或代客燒錄申請的程式碼編號，而空白晶片不帶此碼。

[3] MSL:

濕度敏感性等級係依據 IPC/JEDEC J-STD-020 的規範加以試驗分級，並參考 IPC/JEDEC J-STD-033 的標準處理、包裝、運輸與使用。

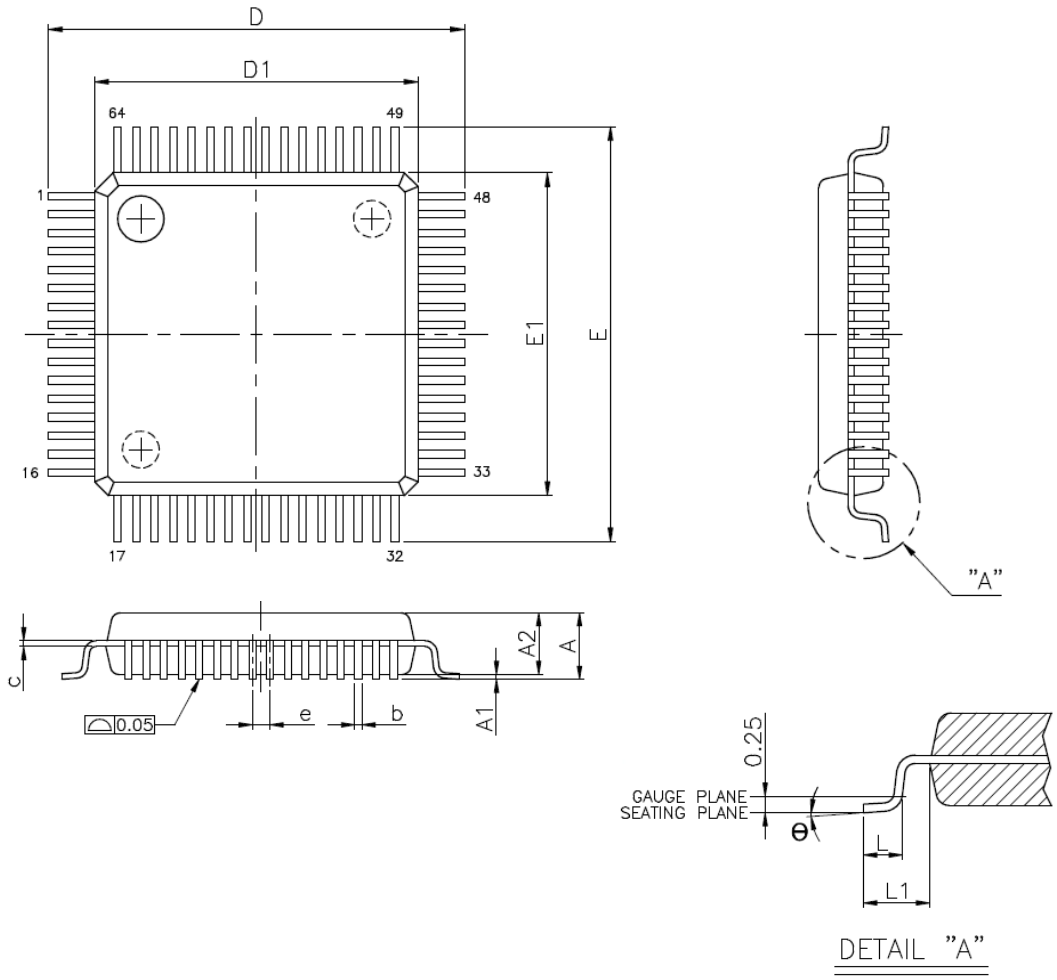
[4] Green (RoHS & no Cl/Br):

HYCON 產品皆為 Green Product，符合 RoHS 指令，REACH 高關注物質(SVHC)以及無鹵素規定 (Br<900ppm or Cl<900ppm or (Br+Cl)<1500ppm)。

8. 封裝型式資訊

8.1. LQFP64(L064)

8.1.1. Package Dimensions LQFP64(7x7)



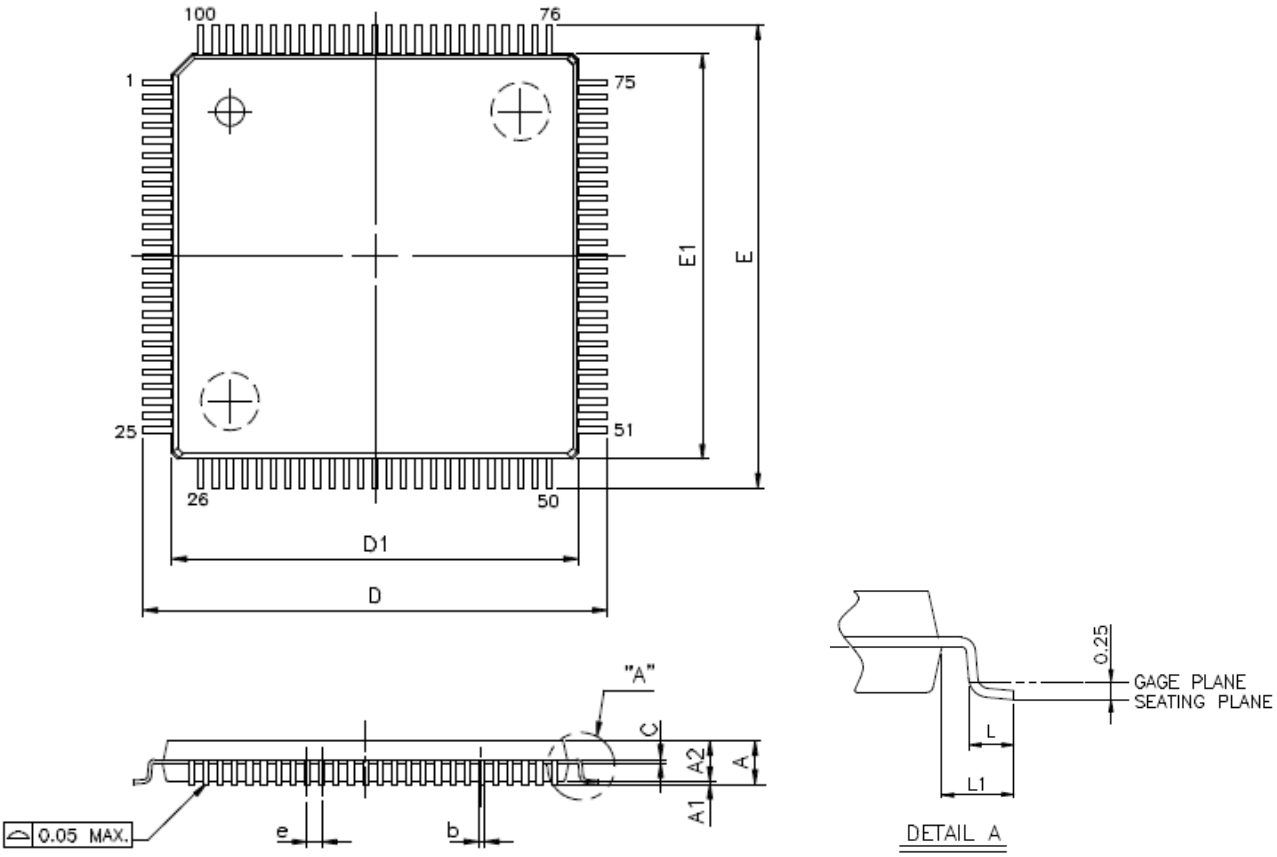
SYMBOLS	MIN.	NOM.	MAX.
A	—	—	1.60
A1	0.05	—	0.15
A2	1.35	1.40	1.45
b	0.13	0.18	0.23
c	0.09	—	0.20
D		9.00 BSC	
D1		7.00 BSC	
e		0.40 BSC	
E		9.00 BSC	
E1		7.00 BSC	
L	0.45	0.60	0.75
L1		1.00 REF	
θ	0°	3.5°	7°

Note:

1. All dimensions refer to JEDEC OUTLINE MS-026.
2. Do not include Mold Flash or Protrusions.
3. Unit: mm.

8.2. LQFP100(L100)

8.2.1. Package Dimensions LQFP100(14x14)



SYMBOLS	MIN.	NOM.	MAX.
A	--	--	1.60
A1	0.05	--	0.15
A2	1.35	1.40	1.45
b	0.17	0.20	0.27
c	0.09	0.127	0.20
D	16.00 BSC		
D1	14.00 BSC		
E	16.00 BSC		
E1	14.00 BSC		
e	0.50 BSC		
L	0.45	0.60	0.75
L1	1.00 REF		

Note:

1. All dimensions refer to JEDEC OUTLINE MS-026.
2. Do not include Mold Flash or Protrusions.
3. Unit: mm.

9. 修訂記錄

以下描述本檔差異較大的地方，而標點符號與字形的改變不在此描述範圍。

文件版次	頁次	日期	摘要
V01	All	2021/10/21	初版發行
V02	All	2022/12/16	修改 4.11 OPAMP 方塊圖