



# **HY17P58**

## **Datasheet**

8-Bit RISC-like Mixed Signal Microcontroller

Embedded 4x40 LCD Driver

18-Bit  $\Sigma\Delta$ ADC

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## 1. 特點

- 8 位元加強型精簡指令集，共有 71 個指令包含硬體乘法指令及查表指令 H08D
- 數位電源工作電壓範圍 2.2V to 5.5V，類比電源工作電壓 2.4V to 4.5V，-40~85°C 工作溫度範圍。
- 支援外部石英震盪器 1MHz~16MHz /32768Hz 及內部高精度 RC 震盪器  
1.6MHz/3.2MHz/7.0MHz Mode 多種 CPU 工作時脈切換選擇，可讓使用者達到最佳省電規劃
- 8KWord OTP (One Time Programmable) Type 程式記憶體，512Byte 資料記憶體
- Brownout detector 及 Watch dog Timer，可防止 CPU 進入死機模式。
- 2 個軌對軌運算放大器 OPAMP
  - CMOS 輸入，1MHz 增益帶寬
- 身體阻抗測量線路
  - 任意波形輸出功能，支援 64bytes 獨立記憶體控制，輸出頻率可達 5KHz~ 250KHz 範圍
  - 4 電極身體阻抗與相位測量
- 定電壓昇壓穩壓線路 15mA 驅動能力
- 4x40 LCD 液晶驅動器
  - 1/4 Duty、1/3 Bias
  - 支援 TypeA 及 TypeB 兩種 LCD 驅動波形
  - 內建 Charge Pump 穩壓線路，可提供多種 LCD 偏壓
  - 44 個 LCD 埠可設定數位輸入輸出埠
- LVD 低電壓檢測功能具 14 段檢測電壓設置與外部輸入電壓檢測功能
- 類比電壓源 VDDA 具 10mA 穩壓電壓源輸出，快速啟動功能，可提供傳感器驅動電壓
- 24-Bit  $\Sigma$ ADC 類比數位轉換器
  - 內置 R type PGA(Programmable Gain Amplifier)及可有 1/4、1/2、1....512 倍多種輸入信號放大倍率選擇
  - 梳狀濾波器採二階/三階設計，轉換頻率達 7.2Ksps
  - 取樣頻率 1MHz
  - 超取樣頻率設置 64 ~ 65536
  - 內置絕對溫度感測器
- 2 個 8-bit Timer A1
- 16-bit Timer B 模組具 Compare/PWM 功能
- Timer C 模組具 Capture/Compare 功能
- 64 words Built-In EPROM (BIE)，內建 2.75V 低壓燒錄控制電路
- 串列通訊 2\*EUART 模組
- Support 8 stack Level.

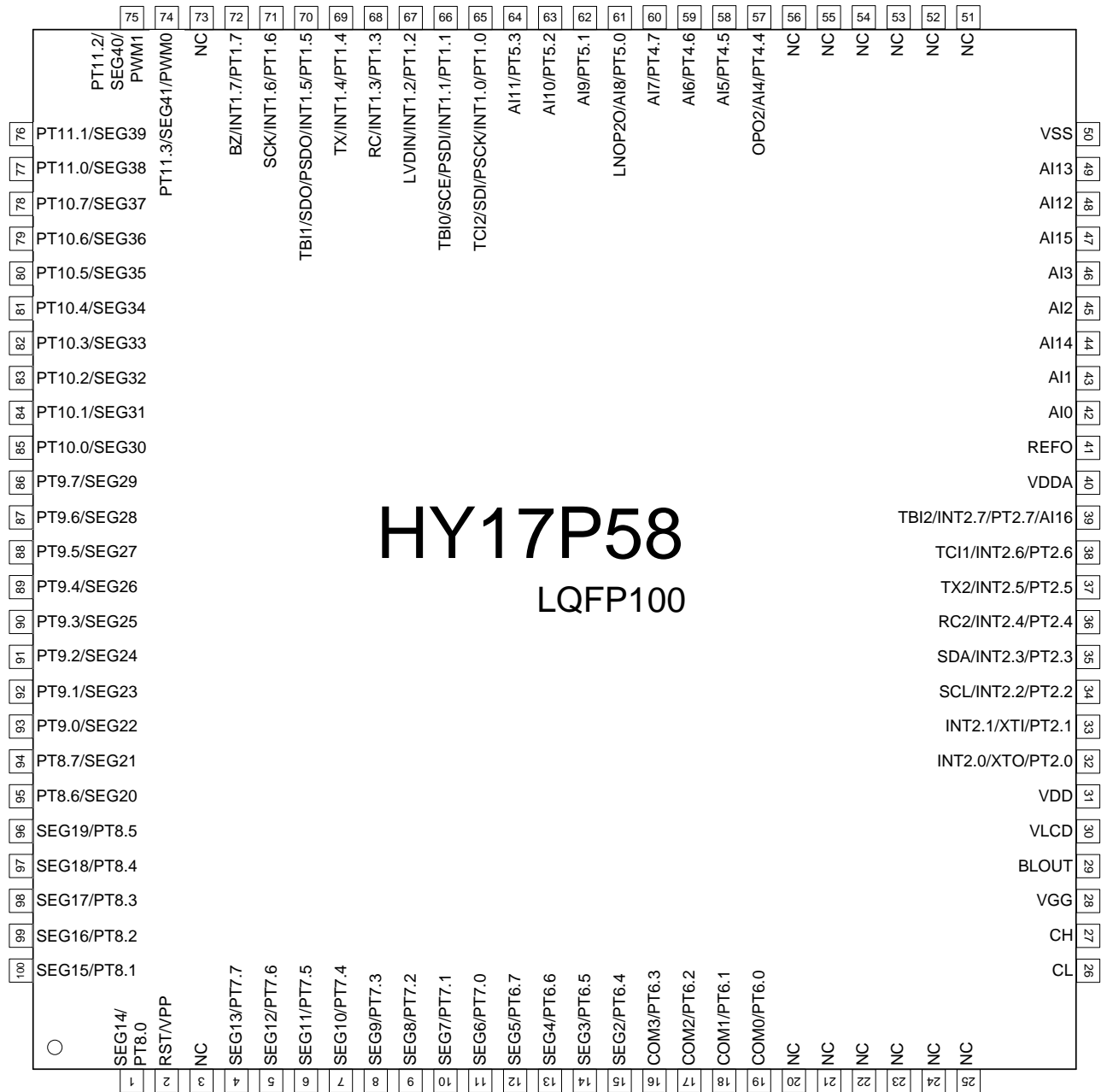
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## 2. 引腳定義

### 2.1. LQFP100 引腳圖



註：VPP 與 RST 復用同一接口，非燒錄 OTP 時禁止輸入高電壓

## 2.2. I/O 定義與說明

“I/O”輸入/輸出,“I”輸入,“O”輸出,“S”史密斯觸發,“C”CMOS 特性兼容輸出與輸入,“P”電壓源,“A”類比通道

引腳編號	引腳名稱	引腳特性		功能說明
		格式	緩衝	
1	SEG14/PT8.0	O	A	LCD Segment 輸出 數位輸入/輸出
	SEG14 PT8.0	I/O	S/C	
2	RST/VPP	I	S	復位晶片 OTP 讀/寫時的電壓源
	RST VPP	P	P	
4	SEG13/PT7.7	O	A	LCD Segment 輸出 數位輸入/輸出
	SEG13 PT7.7	I/O	S/C	
5	SEG12/PT7.6	O	A	LCD Segment 輸出 數位輸入/輸出
	SEG12 PT7.6	I/O	S/C	
6	SEG11/PT7.5	O	A	LCD Segment 輸出 數位輸入/輸出
	SEG11 PT7.5	I/O	S/C	
7	SEG10/PT7.4	O	A	LCD Segment 輸出 數位輸入/輸出
	SEG10 PT7.4	I/O	S/C	
8	SEG9/PT7.3	O	A	LCD Segment 輸出 數位輸入/輸出
	SEG9 PT7.3	I/O	S/C	
9	SEG8/PT7.2	O	A	LCD Segment 輸出 數位輸入/輸出
	SEG8 PT7.2	I/O	S/C	
10	SEG7/PT7.1	O	A	LCD Segment 輸出 數位輸入/輸出
	SEG7 PT7.1	I/O	S/C	
11	SEG6/PT7.0	O	A	LCD Segment 輸出 數位輸入/輸出
	SEG6 PT7.0	I/O	S/C	
12	SEG5/PT6.7	O	A	LCD Segment 輸出 數位輸入/輸出
	SEG5 PT6.7	I/O	S/C	



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13	SEG4/PT6.6 SEG4 PT6.6	O I/O	A S/C	LCD Segment 輸出 數位輸入/輸出
14	SEG3/PT6.5 SEG3 PT6.5	O I/O	A S/C	LCD Segment 輸出 數位輸入/輸出
15	SEG2/PT6.4 SEG2 PT6.4	O I/O	A S/C	LCD Segment 輸出 數位輸入/輸出
16	COM3/PT6.3 COM3 PT6.3	O I/O	A S/C	LCD Segment 輸出 數位輸入/輸出
17	COM2/PT6.2 COM2 PT6.2	O I/O	A S/C	LCD Segment 輸出 數位輸入/輸出
18	COM1/PT6.1 COM1 PT6.1	O I/O	A S/C	LCD Segment 輸出 數位輸入/輸出
19	COM0/PT6.0 COM0 PT6.0	O I/O	A S/C	LCD Segment 輸出 數位輸入/輸出
26	CL	A	A	倍壓電容接口
27	CH	A	A	倍壓電容接口 · 1~10uF to CL Pin.
28	VGG	P	P	倍壓電源輸出 · 10uF need. (Source: VDD)
29	BLOUT	P	P	穩壓電源輸出 · 1~10uF need.(Source: VGG)
30	VLCD	P	P	LCD 的電壓源 · 1~10uF need. (Source: VDD)
31	VDD	P	P	晶片工作電壓源 · 1~10uF need.
32	PT2.0/XTO/INT2.0 PT2.0 XTO INT2.0	I/O A I	S/C A S	數位輸入/輸出 外接振盪器輸出端 中斷源 INTF2.0
33	PT2.1/XTI/INT2.1 PT2.1 XTI INT2.1	I/O A I	S/C A S	數位輸入/輸出 外接振盪器輸入端 中斷源 INTF2.1

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34	PT2.2/INT2.2/SCL PT2.2 INT2.2 SCL	I/O I I/O	S/C S S	數位輸入/輸出 中斷源 INTF2.2 I2C 通訊介面引腳
35	PT2.3/INT2.3/SDA PT2.3 INT2.3 SDA	I/O I I/O	S/C S S	數位輸入/輸出 中斷源 INTF2.3 I2C 通訊介面引腳
36	PT2.4/INT2.4/RC2 PT2.4 INT2.4 RC2	I/O I I	S/C S S	數位輸入/輸出 中斷源 INTF2.4 EUART 通訊介面接口
37	PT2.5/INT2.5/TX2 PT2.5 INT2.5 TX2	I/O I O	S/C S S	數位輸入/輸出 中斷源 INTF2.5 EUART 通訊介面接口
38	PT2.6/INT2.6/TCI1 PT2.6 INT2.6 TCI1	I/O I I	S/C S S	數位輸入/輸出 中斷源 INTF2.6 TimerC 頻率輸入接口
39	PT2.7/INT2.7/TBI2/AI16 PT2.7 INT2.7 TBI2 AI16	I/O I I A	S/C S S A	數位輸入/輸出 中斷源 INTF2.7 TimerB 啟動輸入接口 類比輸入通道
40	VDDA	P	P	穩壓器輸出・類比電路電壓源 (source:VDD)
41	REFO	P	P	類比電路基準電壓源(source:VDDA)
42	A10	A	A	類比輸入通道
43	A11	A	A	類比輸入通道
45	A12	A	A	類比輸入通道
46	A13	A	A	類比輸入通道
48	A12 A12	A	A	類比輸入通道
49	A13 A13	A	A	類比輸入通道
50	VSS	P	P	晶片工作電壓源接地端
57	PT4.4/AI4/OPO2			

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	PT4.4 AI4 OPO2	I A A	S A A	數位輸入 類比輸入通道 R2ROP2 輸出
58	PT4.5/AI5/ PT4.5 AI5	I AA	S A	數位輸入 類比輸入通道
59	PT4.6/AI6 PT4.6 AI6	I A	S A	數位輸入 類比輸入通道
60	PT4.7/AI7 PT4.7 AI7	I A	S A	數位輸入 類比輸入通道
61	PT5.0/AI8/LNOP2O PT5.0 AI8 LNOP2O	I A A	S A A	數位輸入 類比輸入通道 LNOP2 輸出
62	PT5.1/AI9 PT5.1 AI9	I A	S A	數位輸入 類比輸入通道
63	PT5.2/AI10 PT5.2 AI10	I A	S A	數位輸入 類比輸入通道
64	PT5.3/AI11 PT5.3 AI11	I A	S A	數位輸入 類比輸入通道
65	PT1.0/INT1.0/PSCK/SDI/TCI2 PT1.0 INT1.0 PSCK SDI TCI2	I/O I I I/O I	S/C S S S S	數位輸入/輸出 中斷源 E0IF OTP 讀/寫介面接口 SPI 通訊介面接口 TimerC 頻率輸入接口
66	PT1.1/INT1.1/PSDI/SCE/TBI0 PT1.1 INT1.1 PSDI SCE TBI0	I/O I I I I	S/C S S S S	數位輸入/輸出 中斷源 E1IF OTP 讀/寫介面接口 SPI 通訊介面接口 TimerB 啟動輸入接口
67	PT1.2/INT1.2/LVDIN			

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	PT1.2 INT1.2 LVDIN	I/O I A	S/C S A	數位輸入/輸出 中斷源 E2IF LVD 外部信號輸入接口
68	PT1.3/INT1.3/RC PT1.3 INT1.3 RC	I/O I I	S/C S S	數位輸入/輸出 中斷源 E3IF EUART 通訊介面接口
69	PT1.4/INT1.4/TX PT1.4 INT1.4 TX	I/O I O	S/C S C	數位輸入/輸出 中斷源 INTF1.4 EUART 通訊介面接口
70	PT1.5/INT1.5/PSDO/SDO/TBI1 PT1.5 INT1.5 PSDO SDO TBI1	I/O I O I/O I	S/C S S S S	數位輸入/輸出 中斷源 INTF1.5 OTP 讀/寫介面接口 SPI 通訊介面接口 TimerB 啟動輸入接口
71	PT1.6/INT1.6/SCK PT1.6 INT1.6 SCK	I/O I I/O	S/C S S	數位輸入/輸出 中斷源 INTF1.6 SPI 通訊介面接口
72	PT1.7/INT1.7/BZ PT1.7 INT1.7 BZ	I/O I O	S/C S C	數位輸入/輸出 中斷源 INTF1.7 蜂鳴器輸出端
74	SEG41/PT11.3/PWM0 SEG41 PT11.3 PWM0	O I/O O	A S/C C	LCD Segment 輸出 數位輸入/輸出 PWM0 輸出接口
75	SEG40/PT11.2/PWM1 SEG40 PT11.2 PWM1	O I/O O	A S/C C	LCD Segment 輸出 數位輸入/輸出 PWM1 輸出接口
76	SEG39/PT11.1 SEG39 PT11.1	O I/O	A S/C	LCD Segment 輸出 數位輸入/輸出
77	SEG38/PT11.0 SEG38	O	A	LCD Segment 輸出

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	PT11.0	I/O	S/C	數位輸入/輸出
78	SEG37/PT10.7			
	SEG37	O	A	LCD Segment 輸出
	PT10.7	I/O	S/C	數位輸入/輸出
79	SEG36/PT10.6			
	SEG36	O	A	LCD Segment 輸出
	PT10.6	I/O	S/C	數位輸入/輸出
80	SEG35/PT10.5			
	SEG35	O	A	LCD Segment 輸出
	PT10.5	I/O	S/C	數位輸入/輸出
81	SEG34/PT10.4			
	SEG34	O	A	LCD Segment 輸出
	PT10.4	I/O	S/C	數位輸入/輸出
82	SEG33/PT10.3			
	SEG33	O	A	LCD Segment 輸出
	PT10.3	I/O	S/C	數位輸入/輸出
83	SEG32/PT10.2			
	SEG32	O	A	LCD Segment 輸出
	PT10.2	I/O	S/C	數位輸入/輸出
84	SEG31/PT10.1			
	SEG31	O	A	LCD Segment 輸出
	PT10.1	I/O	S/C	數位輸入/輸出
85	SEG30/PT10.0			
	SEG30	O	A	LCD Segment 輸出
	PT10.0	I/O	S/C	數位輸入/輸出
86	SEG29/PT9.7			
	SEG29	O	A	LCD Segment 輸出
	PT9.7	I/O	S/C	數位輸入/輸出
87	SEG28/PT9.6			
	SEG28	O	A	LCD Segment 輸出
	PT9.6	I/O	S/C	數位輸入/輸出
88	SEG27/PT9.5			
	SEG27	O	A	LCD Segment 輸出
	PT9.5	I/O	S/C	數位輸入/輸出
89	SEG26/PT9.4			
	SEG26	O	A	LCD Segment 輸出
	PT9.4	I/O	S/C	數位輸入/輸出
90	SEG25/PT9.3			

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	SEG25 PT9.3	O I/O	A S/C	LCD Segment 輸出 數位輸入/輸出
91	SEG24/PT9.2 SEG24 PT9.2	O I/O	A S/C	LCD Segment 輸出 數位輸入/輸出
92	SEG23/PT9.1 SEG23 PT9.1	O I/O	A S/C	LCD Segment 輸出 數位輸入/輸出
93	SEG22/PT9.0 SEG22 PT9.0	O I/O	A S/C	LCD Segment 輸出 數位輸入/輸出
94	SEG21/PT8.7 SEG21 PT8.7	O I/O	A S/C	LCD Segment 輸出 數位輸入/輸出
95	SEG20/PT8.6 SEG20 PT8.6	O I/O	A S/C	LCD Segment 輸出 數位輸入/輸出
96	SEG19/PT8.5 SEG19 PT8.5	O I/O	A S/C	LCD Segment 輸出 數位輸入/輸出
97	SEG18/PT8.4 SEG18 PT8.4	O I/O	A S/C	LCD Segment 輸出 數位輸入/輸出
98	SEG17/PT8.3 SEG17 PT8.3	O I/O	A S/C	LCD Segment 輸出 數位輸入/輸出
99	SEG16/PT8.2 SEG16 PT8.2	O I/O	A S/C	LCD Segment 輸出 數位輸入/輸出
100	SEG15/PT8.1 SEG15 PT8.1	O I/O	A S/C	LCD Segment 輸出 數位輸入/輸出
	NC	-	-	不可連接

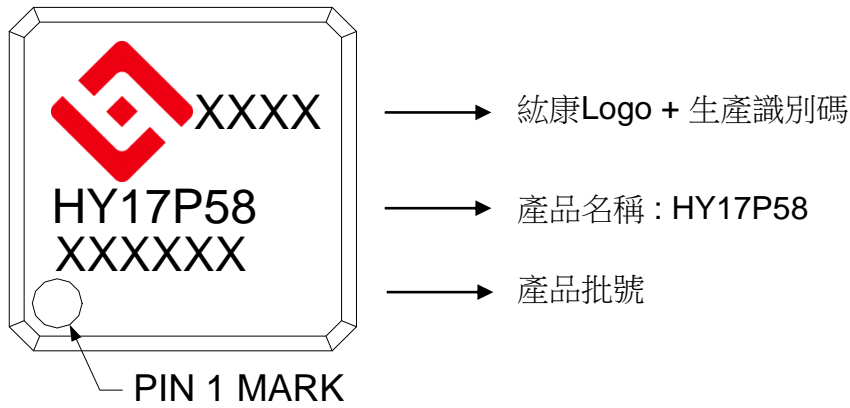
## 2.3. 封裝片標記信息

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## 2.3.1. LQFP 封裝片標記信息



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## 3. 應用電路

### 3.1. 四電極 AC 體脂秤

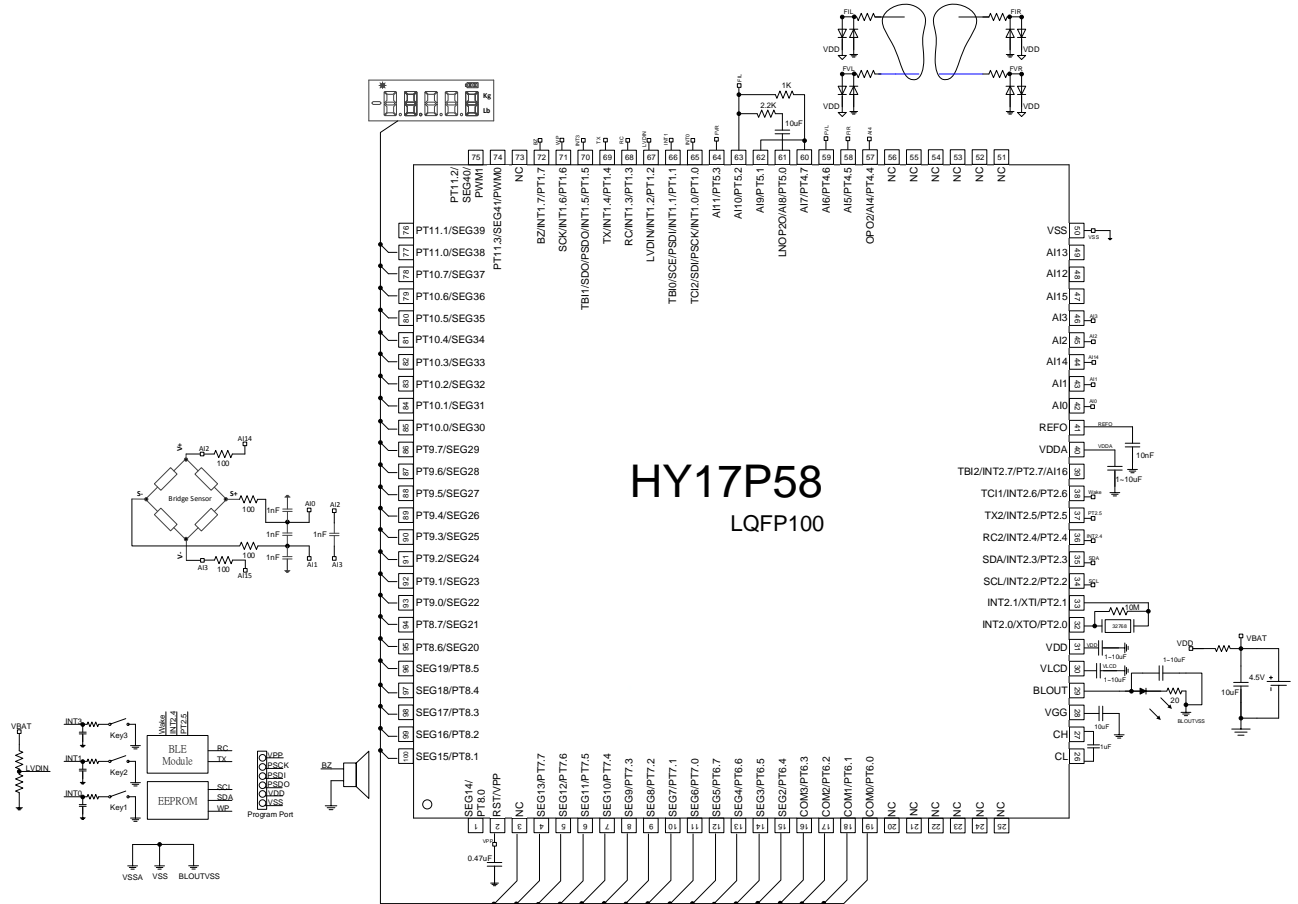


圖 3-1 四電極 AC 體脂秤應用電路





## 4. 功能概述

### 4.1. 內部方塊圖

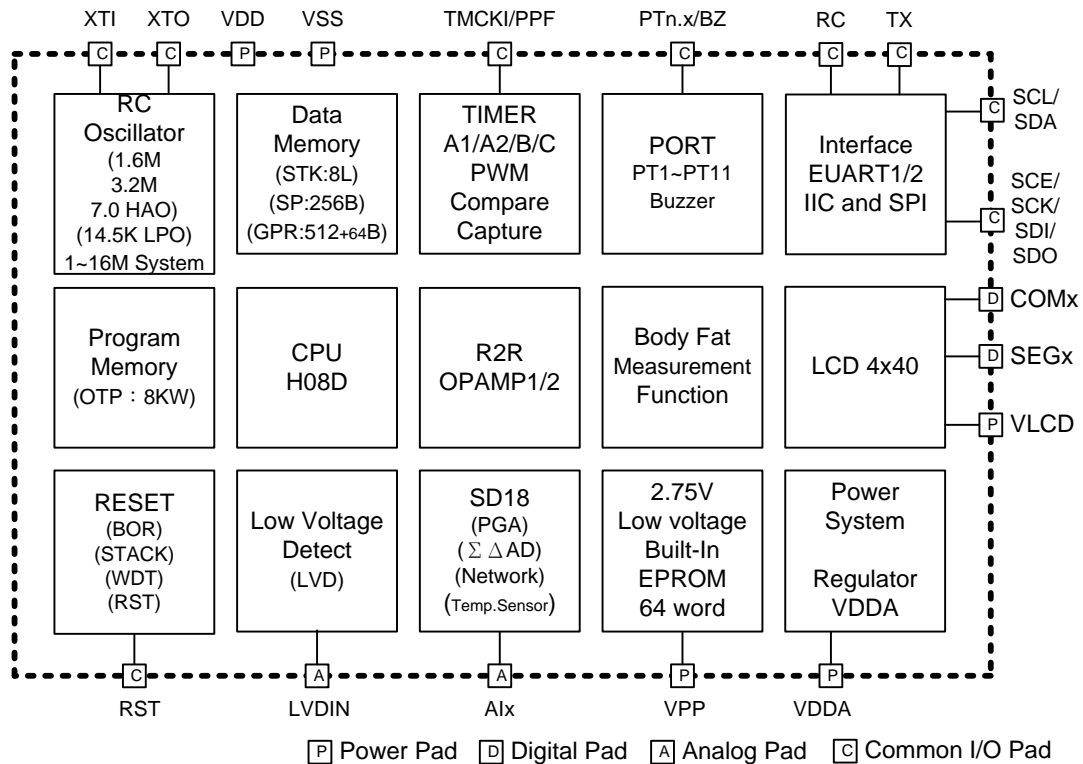


圖 4-1HY17P58 內部方塊圖

### 4.2. 相關說明與支援文件

#### 晶片功能相關使用說明書

DS-HY17P58	HY17P58 說明書
UG-HY17S58	HY17S58 使用說明書
APD-CORE002	H08D 指令集說明書

#### 開發工具相關使用說明書

APD-HY17PIDE001	HY17P 系列開發工具軟體使用說明書
APD-HY17PIDE002	HY17P 系列開發工具硬體使用說明書
APD-OTP006	HY17P OTP 燒錄引腳資訊

#### 產品生產相關使用說明書

APD-HY17PIDE004	HY17P 系列生產線專用燒錄器說明書
BDI-HY17P58	HY17P58 個別產品的裸片打線訊息

## 4.3. Clock System

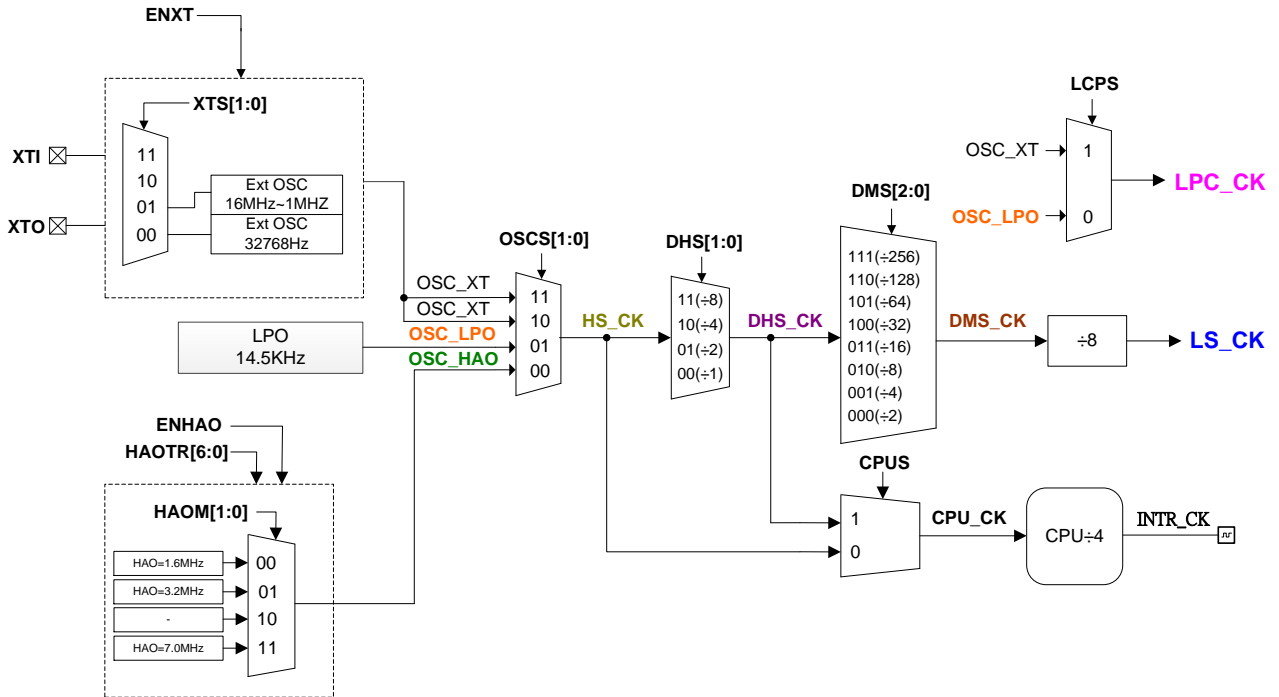


圖 4-2 Clock System 方塊圖(一)

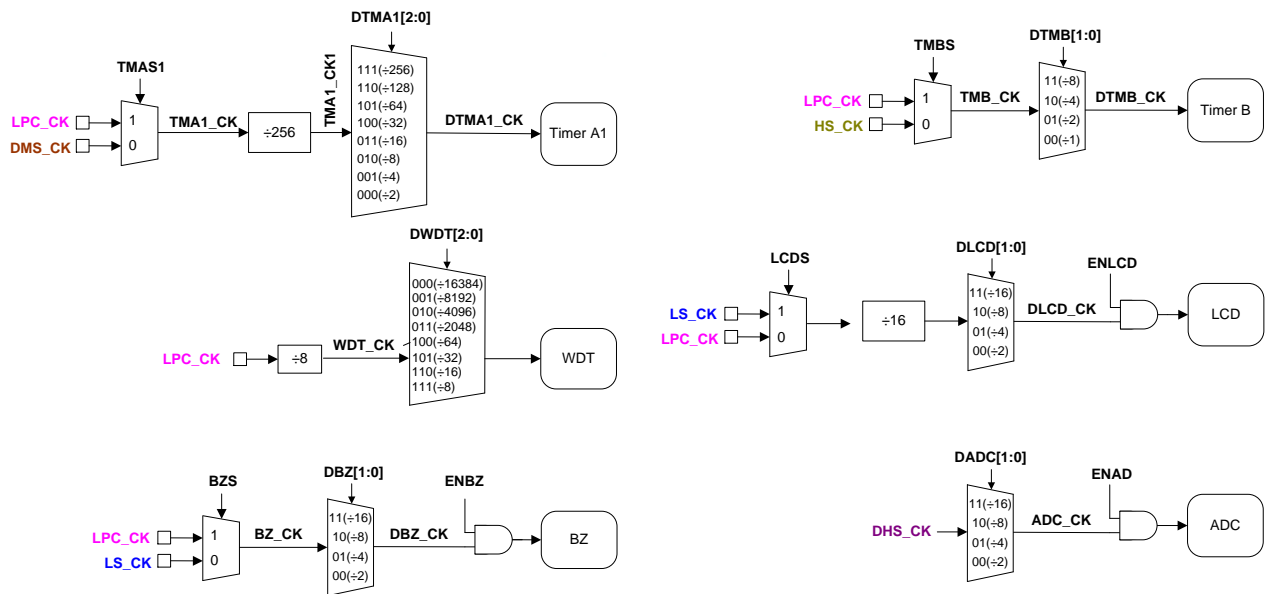


圖 4-3 Clock System 方塊圖(二)

## 4.4. Low Voltage Detect(LVD)

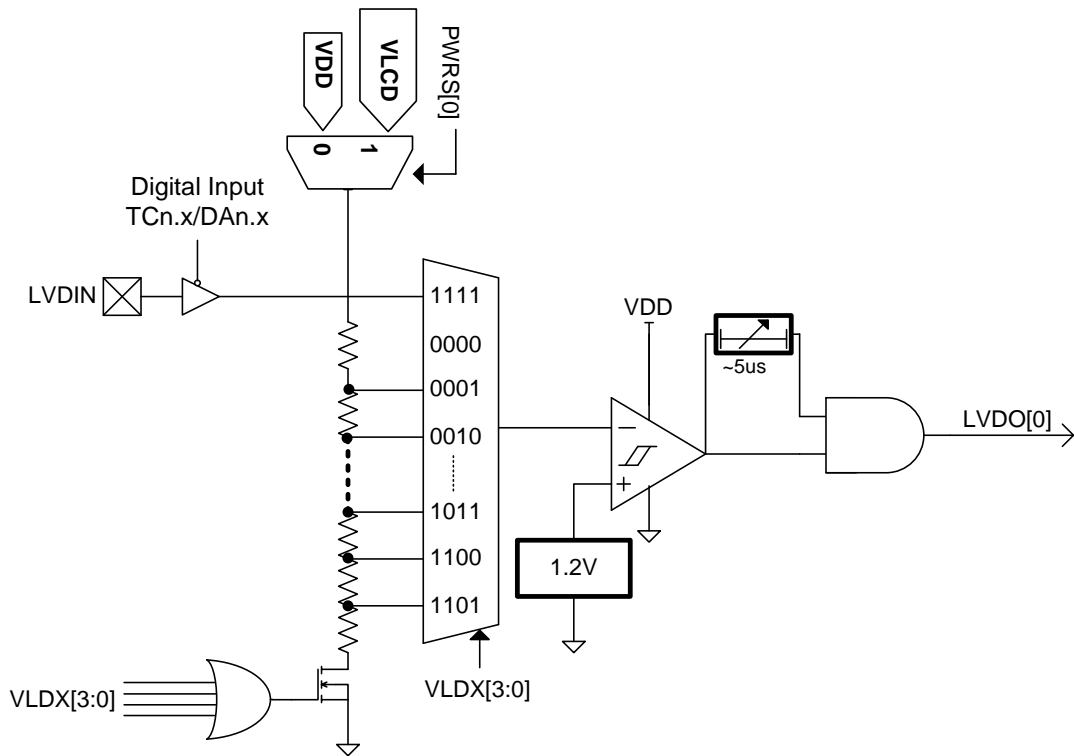


圖 4-4 Low Voltage Detect 方塊圖

## 4.5. Reset

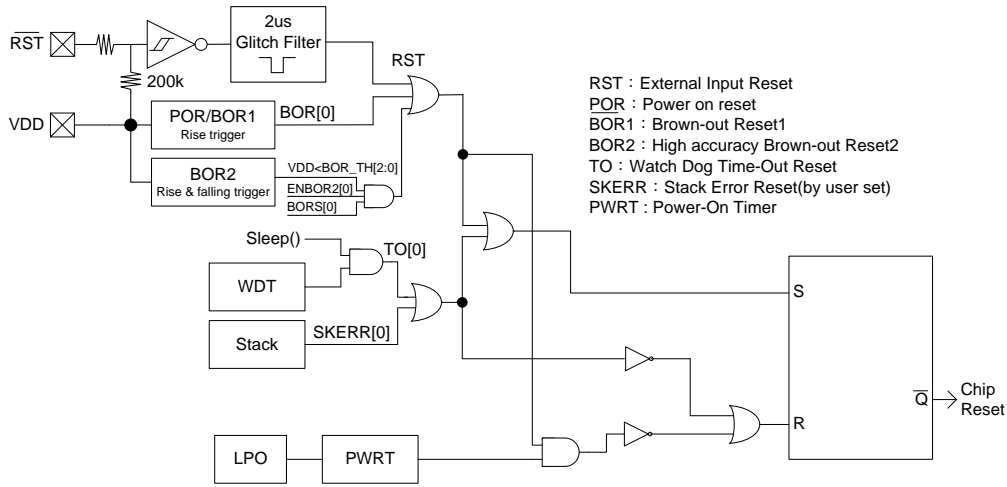


圖 4-5 Reset 方塊圖

## 4.6. Power System

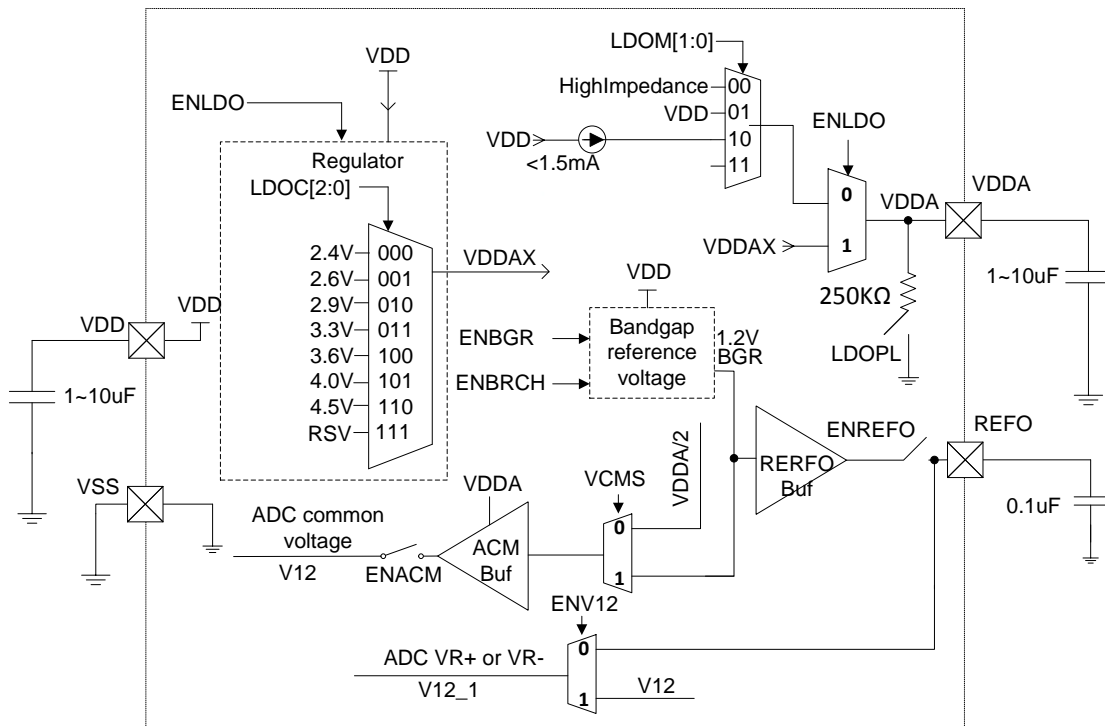


圖 4-6 Power System 方塊圖

## 4.7. SD18 Network

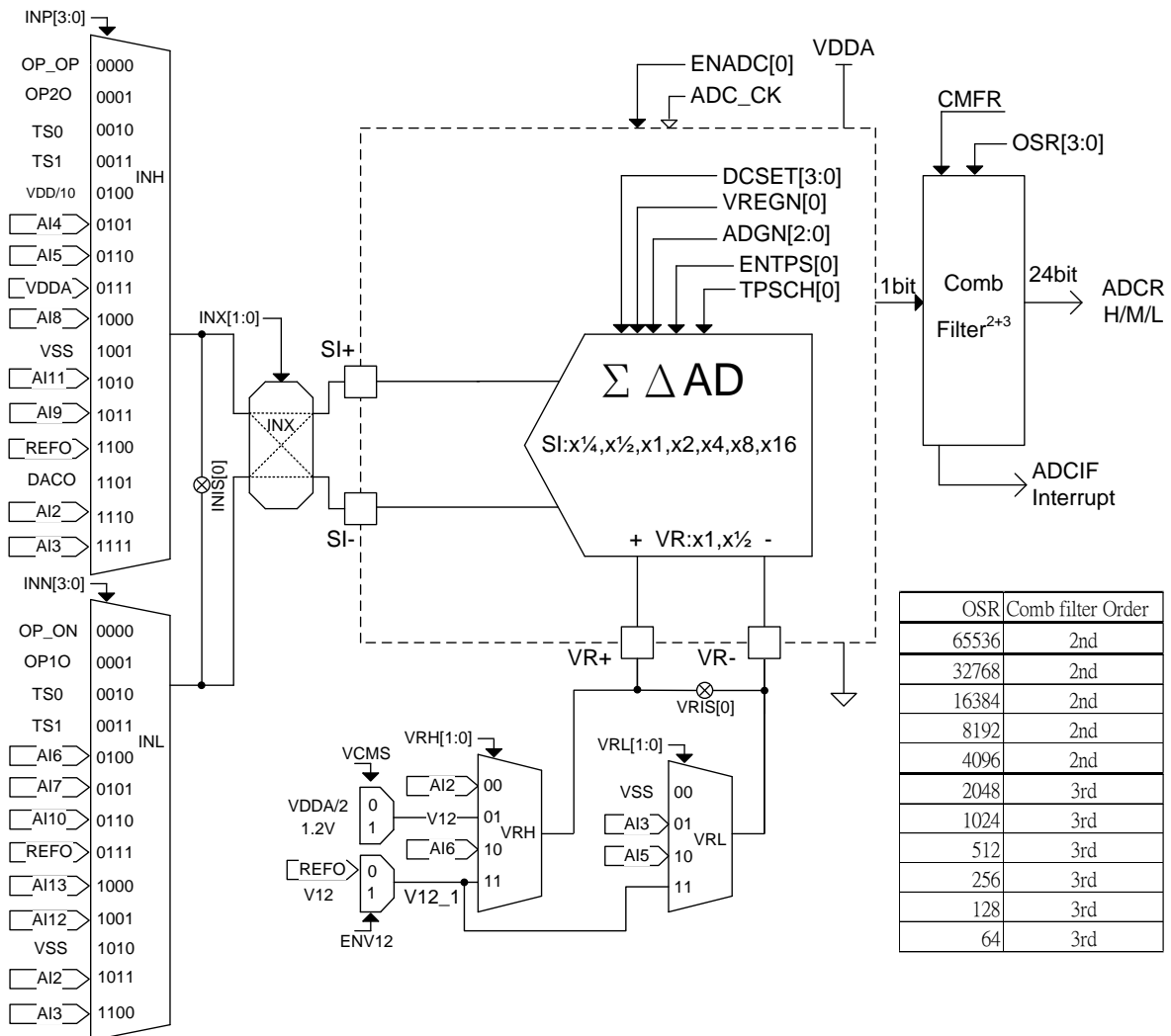


圖 4-7 SD18 Network 方塊圖

## 4.8. GPIO PT1 and PT2

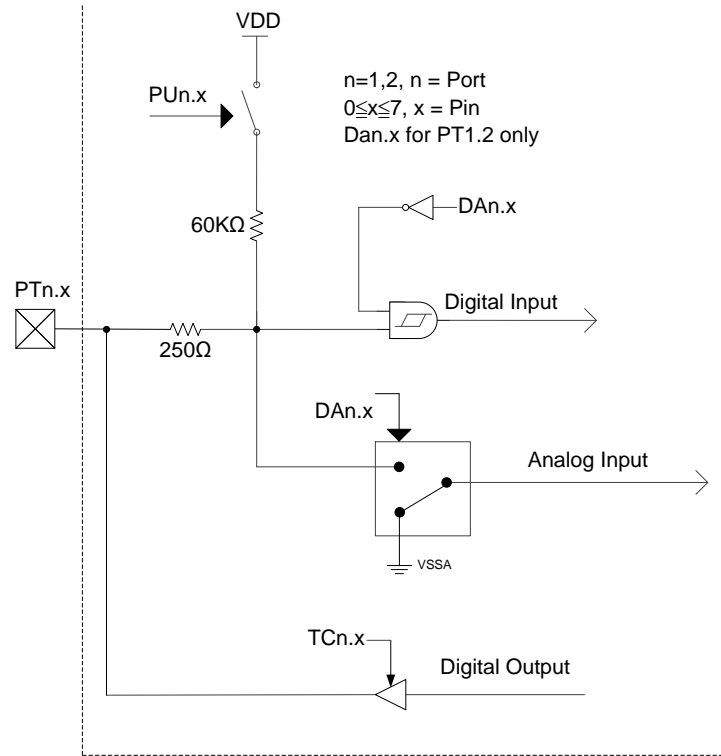


圖 4-8 GPIO PT1 and PT2 方塊圖

## 4.9. GPIO PORT4~5

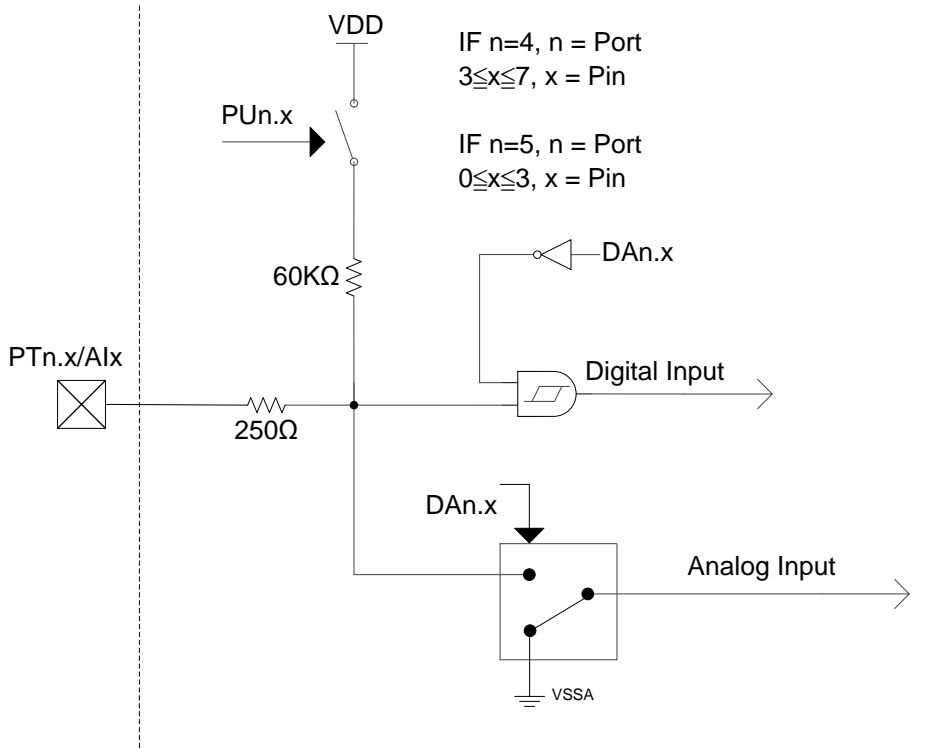


圖 4-9 GPIO PORT4~5 方塊圖

## 4.10. GPIO PT6~PT7/LCD COM0~COM3

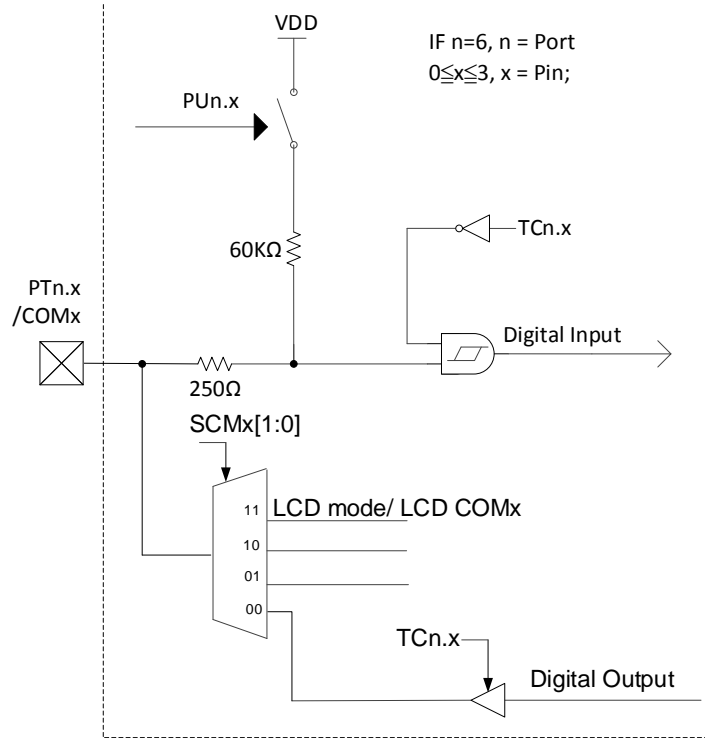


圖 4-10 GPIO PT6~PT7/COM0~COM3 方塊圖

## 4.11. GPIO PORT6~7/LCD SEG2~SEG13

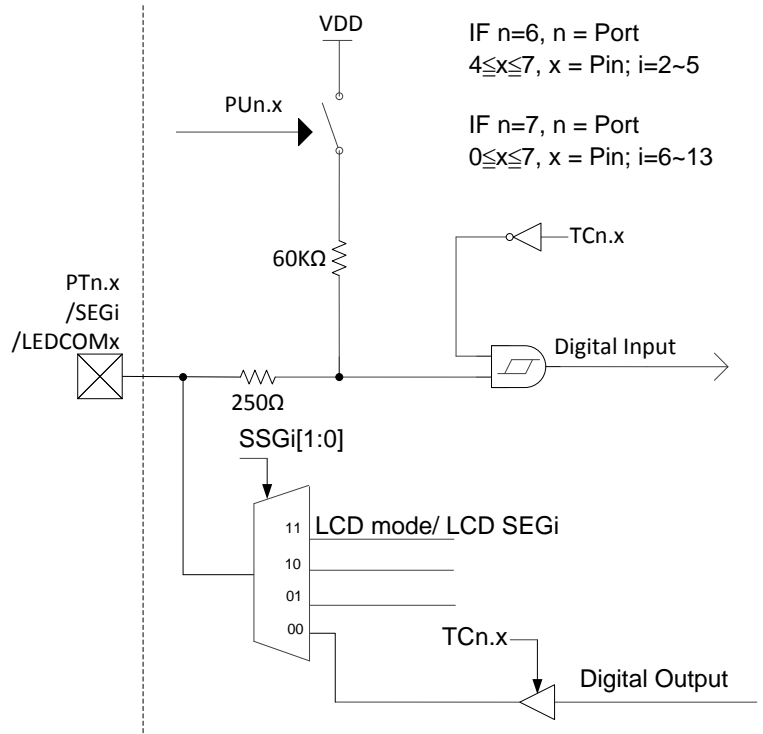


圖 4-11 GPIO PT8/SEG14~SEG21 方塊圖



## 4.12. GPIO PORT 8,10,11/LCD SEG14~21, SEG34~41

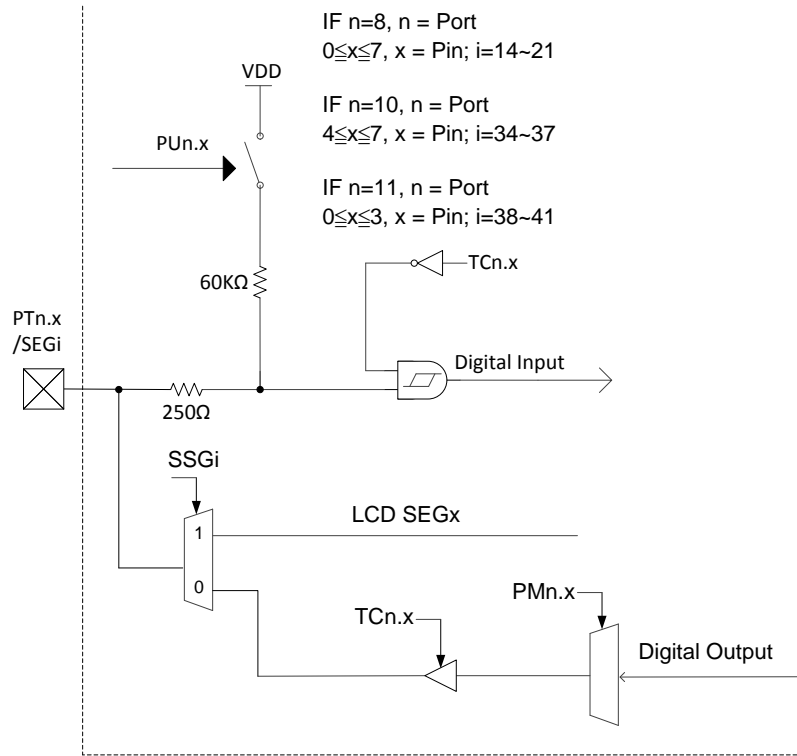


圖 4-12 GPIO 方塊圖

## 4.13. GPIO PORT 9~10/LCD SEG22~33

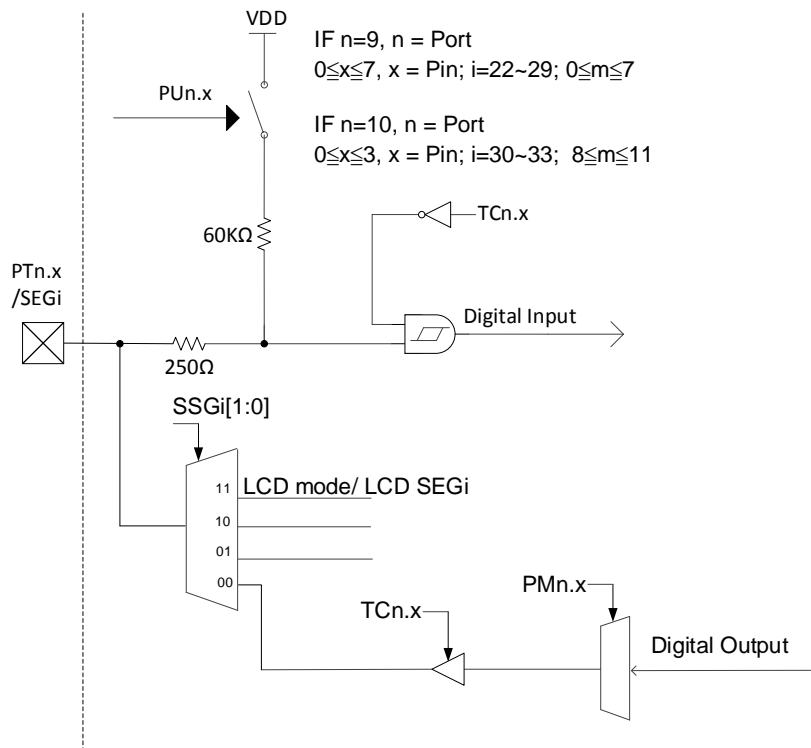


圖 4-13 GPIO 方塊圖

## 4.14. Watch Dog

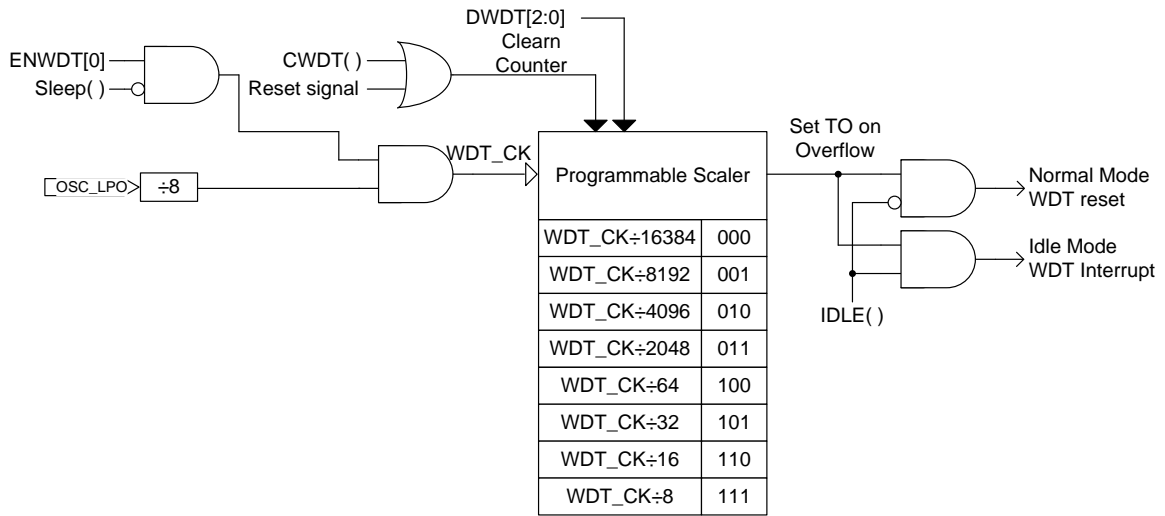


圖 4-14 Watch Dog 方塊圖

## 4.15. 8-bit Timer A1

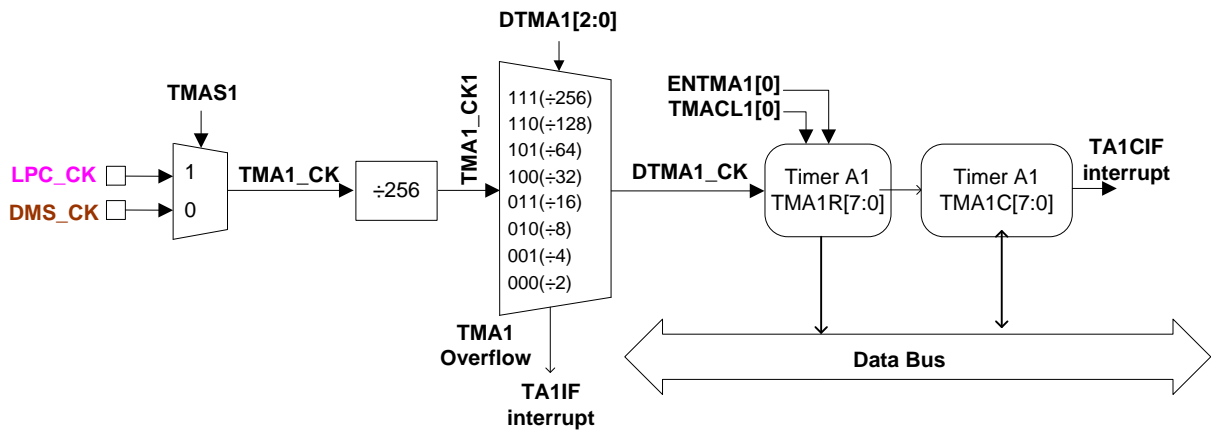


圖 4-15 8-bit Timer A1 方塊圖

## 4.16. 8-bit Timer A2

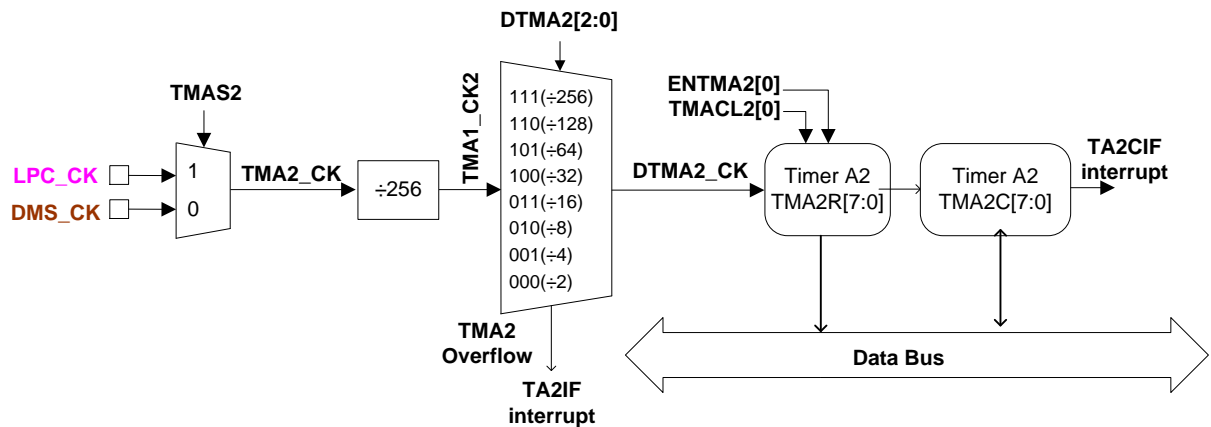


圖 4-16 8-bit Timer A2 方塊圖

## 4.17. 16-bit Timer B

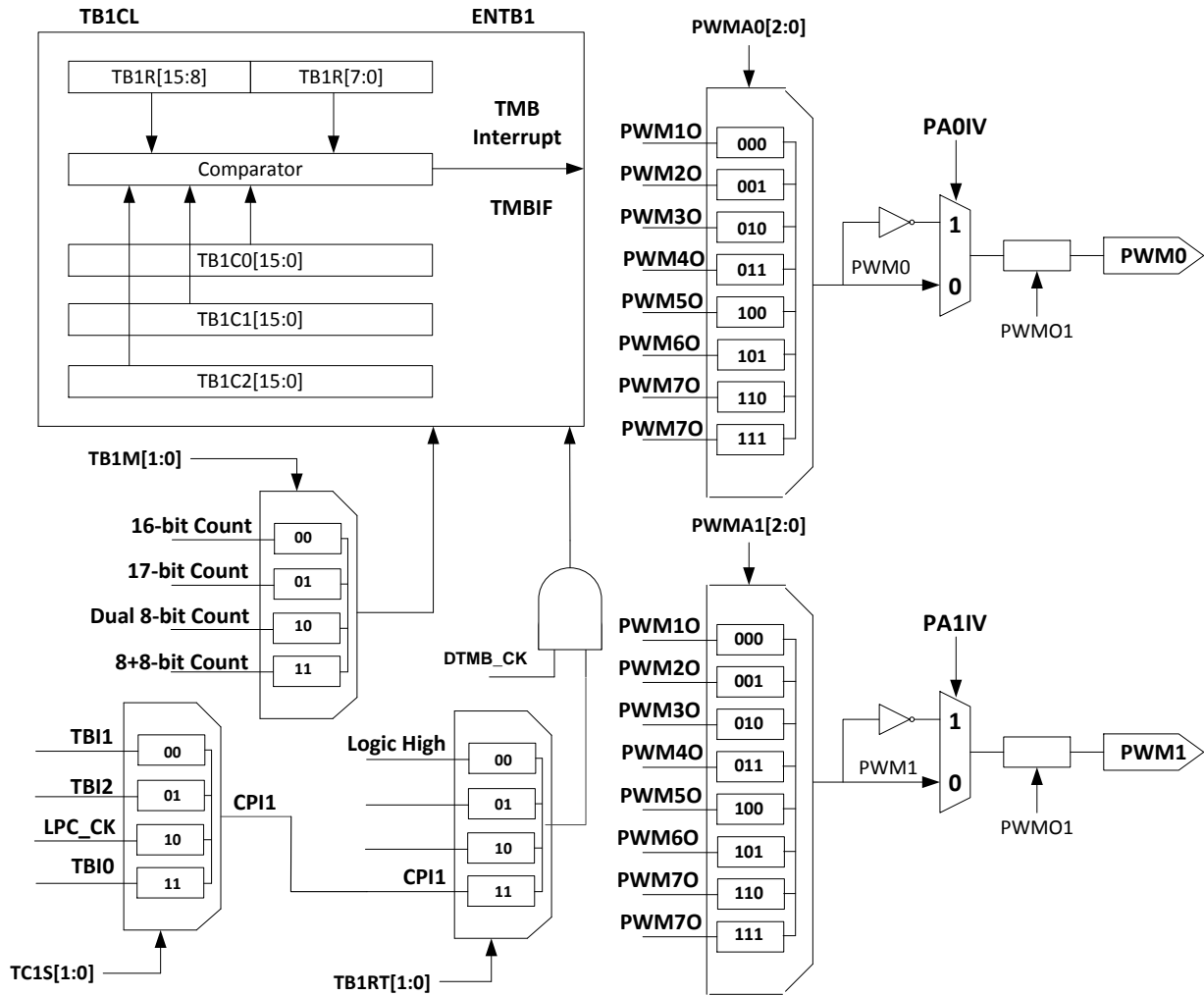


圖 4-17 16-bit Timer B 方塊圖

## 4.18. Time C

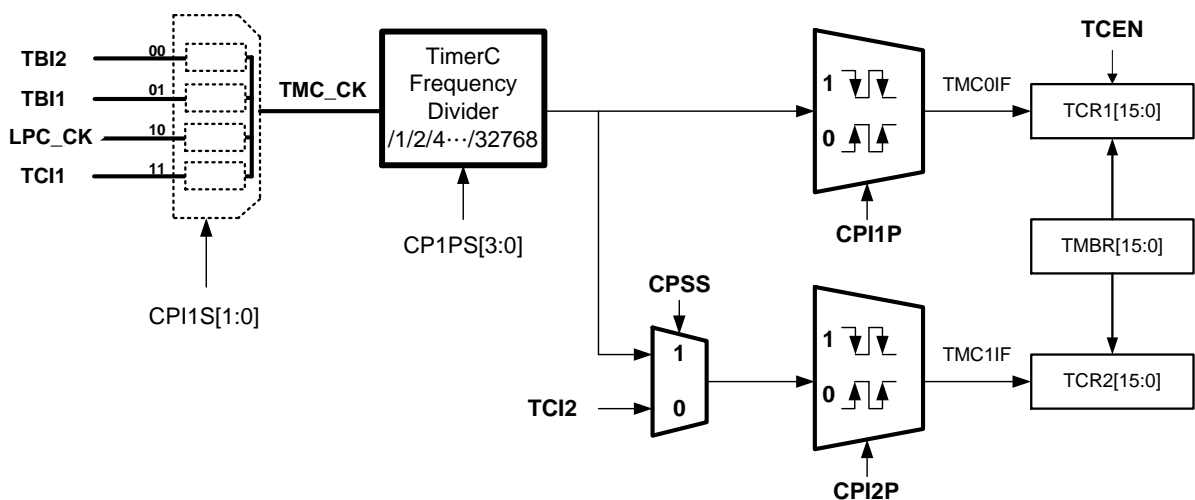


圖 4-18 Timer C 方塊圖

## 4.19. LCD

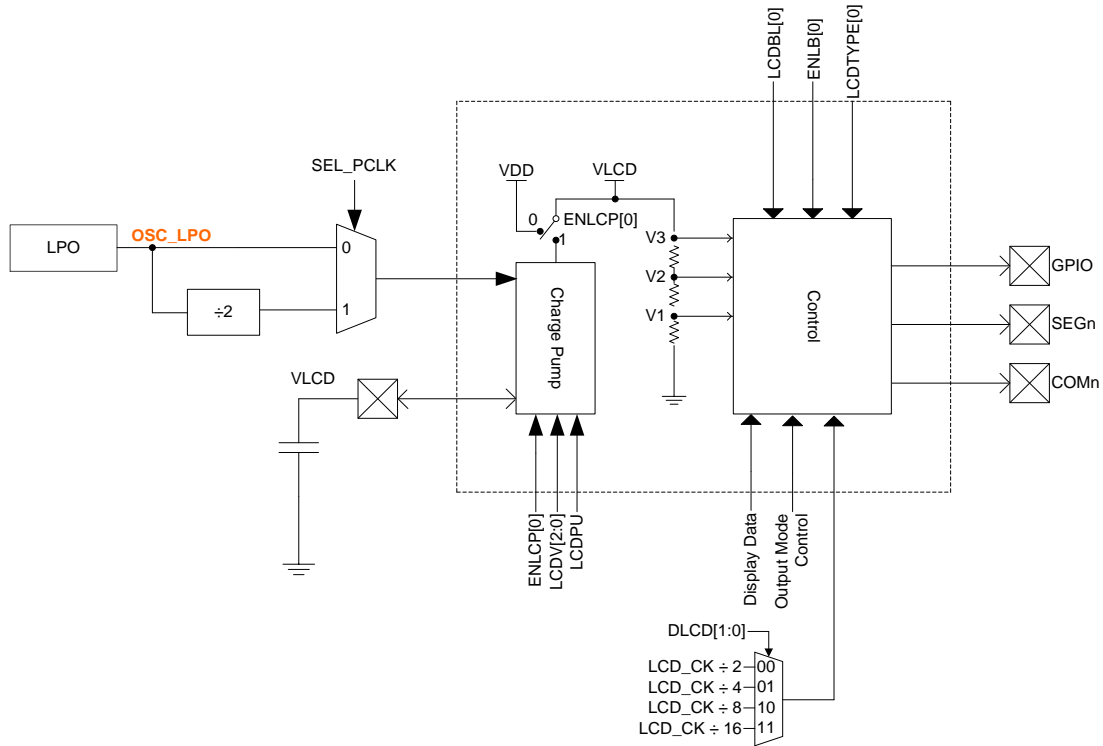


圖 4-18 LCD 方塊圖

## 4.20. EUART and EUART2

### EUART TRANSMIT BLOCK DIAGRAM

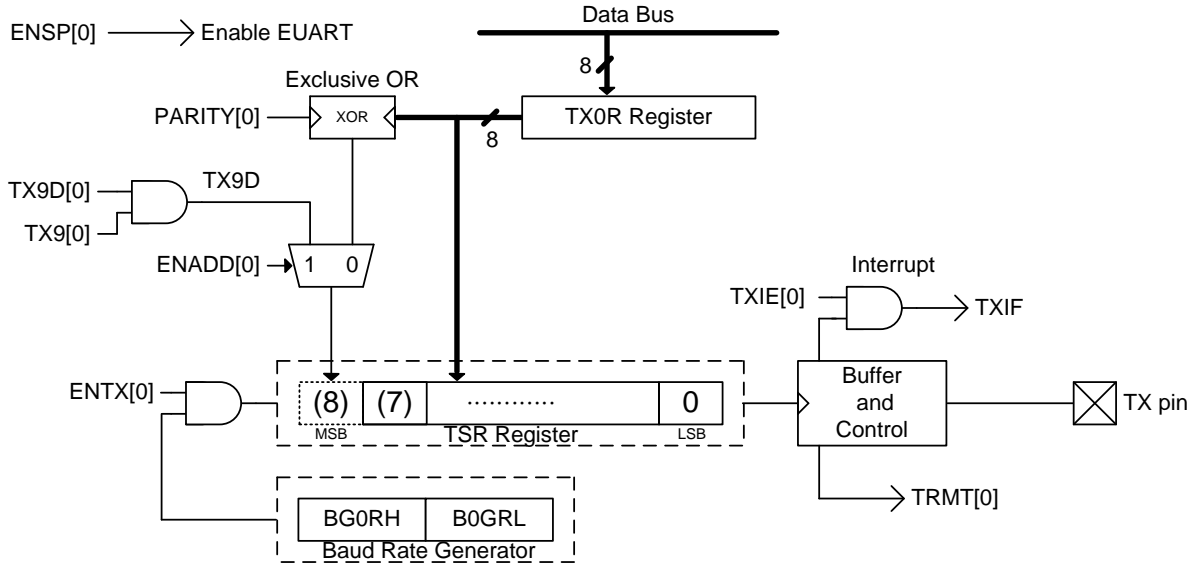
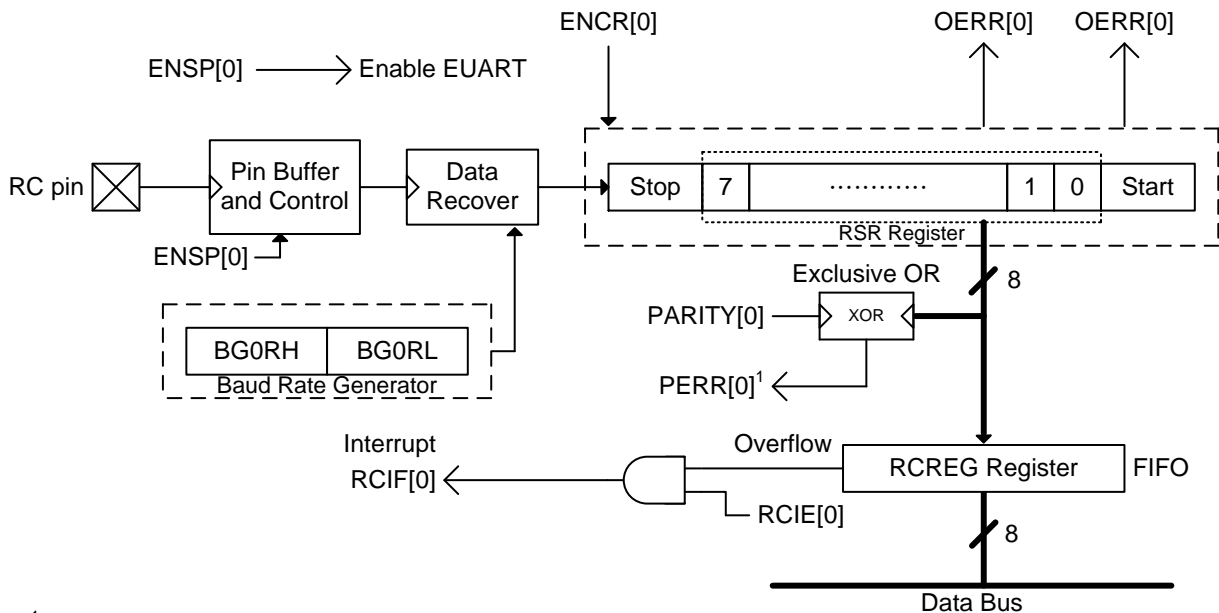


圖 4-19 EUART 傳送方塊圖

### EUART 8-BITS RECEIVE BLOCK DIAGRAM



<sup>1</sup>Don't care PERR[0] state of 8-bits receive mode

圖 4-20 EUART 8-bits 接收方塊圖

## 4.21. SPI

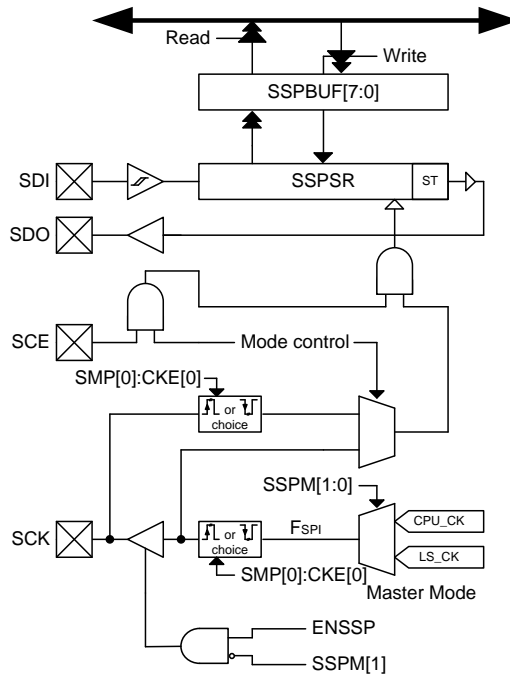


圖 4-21 SPI 方塊圖

## 4.22. I2C

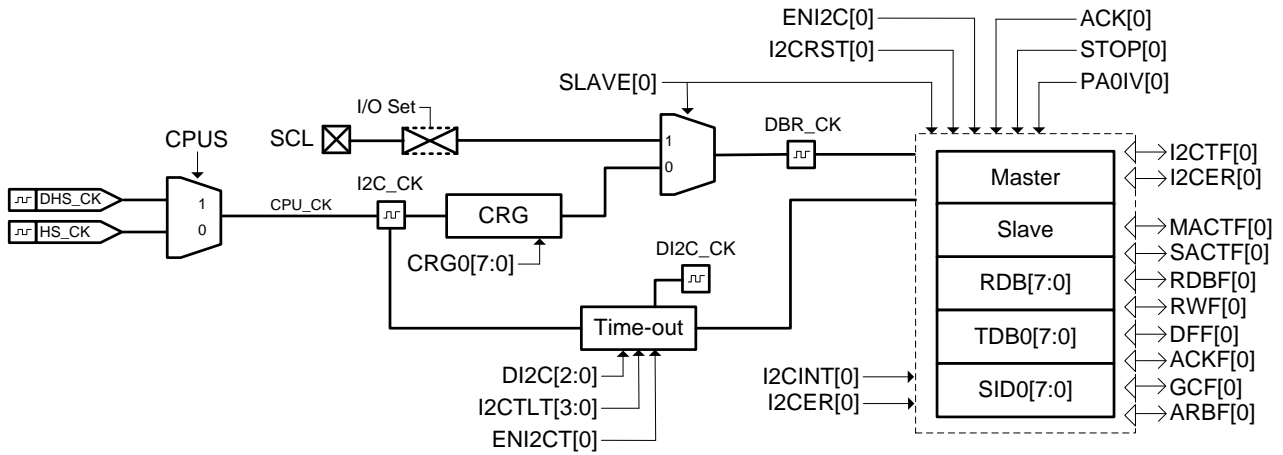


圖 4-22 I2C 方塊圖

## 4.23. 8-Bit DAC

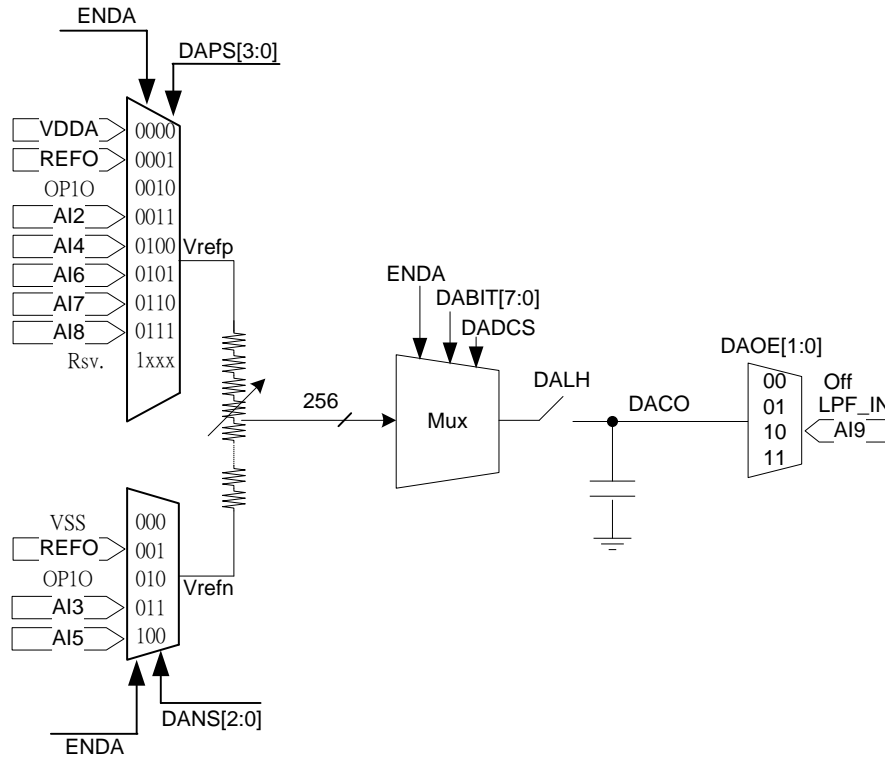


圖 4-23 8-Bit DAC 方塊圖

## 4.24. Rail to Rail OPAMP1

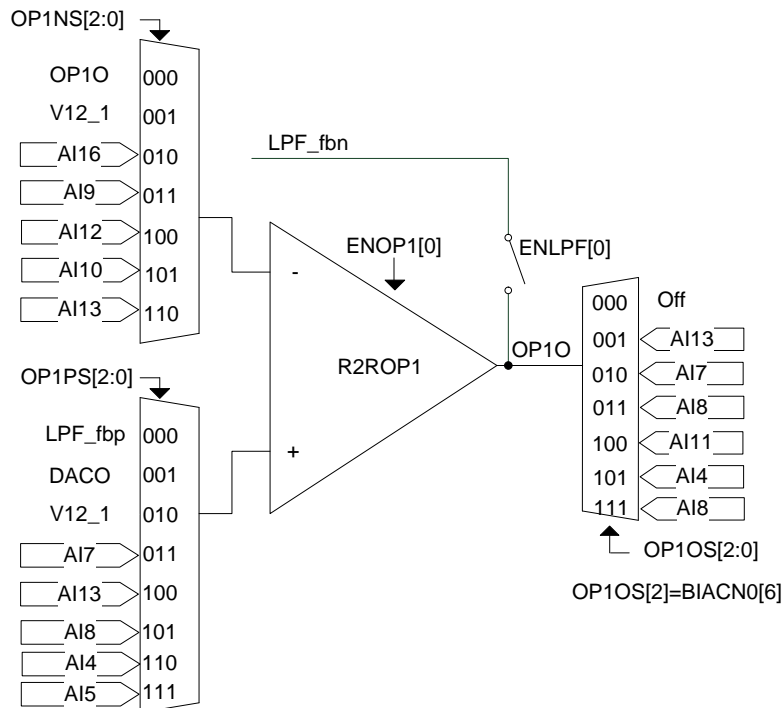


圖 4-24 Rail to Rail OPAMP1 方塊圖

## 4.25. Rail to Rail OPAMP2

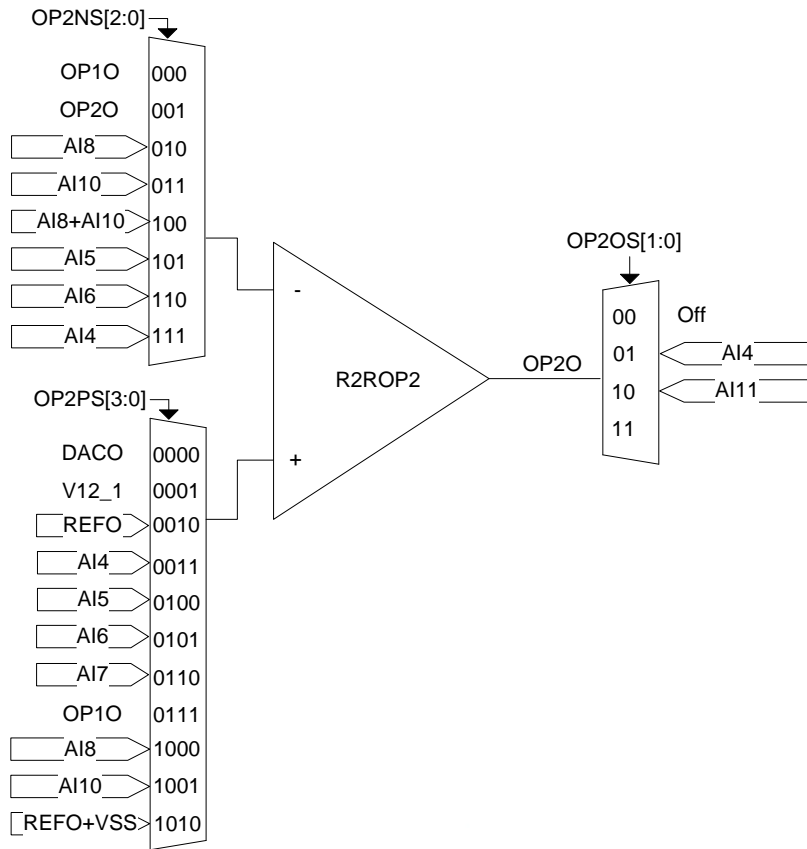


圖 4-25 Rail to Rail OPAMP1 方塊圖



## 4.26. R-type PGA

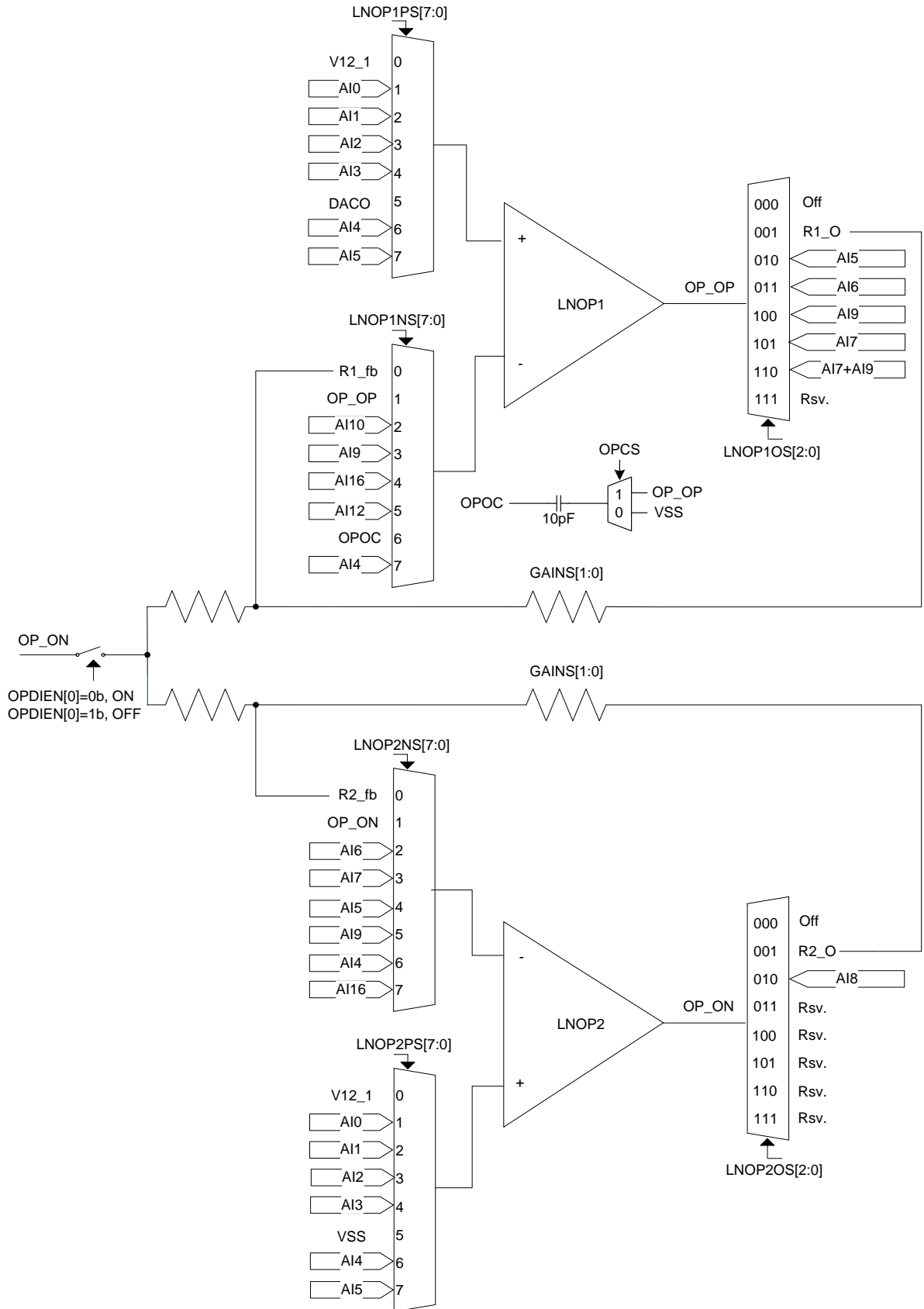


圖 4-26 R type PGA 方塊圖

## 4.27. LED Backlight Function

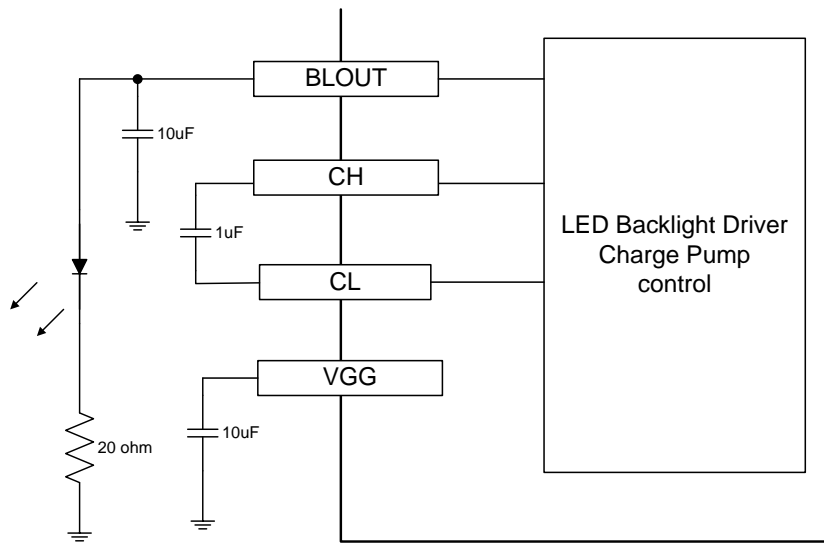


圖 4-27 LED Backlight 方塊圖

## 5. 暫存器列表

“-”no use, “\*”read/write, “w”write, “r”read, “r0”only read 0, “r1”only read 1, “w0”only write 0, “w1”only write 1

“\$”for event status, “.”unimplemented bit, “x”unknown, “u”unchanged, “d”depends on condition

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	ARST	IRST	R/W	
000h	INDF0	Contents of FSR0 to address data memoryvalue of FSR0 not changed								xxxx xxxx	uuuu uuuu	***** r r r r	
001h	POINC0	Contents of FSR0 to address data memoryvalue of FSR0 post-incremented								xxxx xxxx	uuuu uuuu	***** r r r r	
002h	PODEC0	Contents of FSR0 to address data memoryvalue of FSR0 post-decremented								xxxx xxxx	uuuu uuuu	***** r r r r	
003h	PRINC0	Contents of FSR0 to address data memoryvalue of FSR0 pre-incremented								xxxx xxxx	uuuu uuuu	***** r r r r	
004h	PLUSW0	Contents of FSR0 to address data memoryvalue of FSR0 offset by W								xxxx xxxx	uuuu uuuu	***** r r r r	
005h	INDF1	Contents of FSR1 to address data memoryvalue of FSR1 not changed								xxxx xxxx	uuuu uuuu	***** r r r r	
006h	POINC1	Contents of FSR1 to address data memoryvalue of FSR1 post-incremented								xxxx xxxx	uuuu uuuu	***** r r r r	
007h	PODEC1	Contents of FSR1 to address data memoryvalue of FSR1 post-decremented								xxxx xxxx	uuuu uuuu	***** r r r r	
008h	PRINC1	Contents of FSR1 to address data memoryvalue of FSR1 pre-incremented								xxxx xxxx	uuuu uuuu	***** r r r r	
009h	PLUSW1	Contents of FSR1 to address data memoryvalue of FSR1 offset by W								xxxx xxxx	uuuu uuuu	***** r r r r	
00Ah	INDF2	Contents of FSR2 to address data memoryvalue of FSR2 not changed								xxxx xxxx	uuuu uuuu	***** r r r r	
00Bh	POINC2	Contents of FSR2 to address data memoryvalue of FSR2 post-incremented								xxxx xxxx	uuuu uuuu	***** r r r r	
00Ch	PODEC2	Contents of FSR2 to address data memoryvalue of FSR2 post-decremented								xxxx xxxx	uuuu uuuu	***** r r r r	
00Dh	PRINC2	Contents of FSR2 to address data memoryvalue of FSR2 pre-incremented								xxxx xxxx	uuuu uuuu	***** r r r r	
00Eh	PLUSW2	Contents of FSR2 to address data memoryvalue of FSR2 offset by W								xxxx xxxx	uuuu uuuu	***** r r r r	
00Fh	FSROH	-	-	-	-	-	-	-	FSR0[9:8]	.... xxxx	.... uuuu	***** r r r r	
010h	FSROL	Indirect Data Memory Address Pointer 0 Low Byte,FSR0[7:0]								xxxx xxxx	uuuu uuuu	***** r r r r	
011h	FSR1H	-	-	-	-	-	-	-	FSR1[9:8]	.... .xxx	.... .uuu	***** r r r r	
012h	FSR1L	Indirect Data Memory Address Pointer 0 Low Byte,FSR1[7:0]								xxxx xxxx	uuuu uuuu	***** r r r r	
013h	FSR2H	-	-	-	-	-	-	-	FSR2[9:8]	.... .xxx	.... .uuu	***** r r r r	
014h	FSR2L	Indirect Data Memory Address Pointer 0 Low Byte,FSR2[7:0]								xxxx xxxx	uuuu uuuu	***** r r r r	
016h	TOSH	-	-	-	-	-	-	-	TOS[12:8]	.xxx xxxx	.uuu uuuu	***** r r r r	
017h	TOSL	Top-of-Stack Low Byte (TOS<7:0>)								xxxx xxxx	uuuu uuuu	***** r r r r	
018h	SKCN	SKFL	SKUN	SKOV	-	-	-	-	SKPRT[3:0]	000. 0000	u\$\$.\$\$\$	rw0,rw0,rw0,- ****	
01Ah	PCLATH	-	-	-	-	-	-	-	PC[12:8]	..00 0000	..00 0000	***** r r r r	
01Bh	PCLATL	PC Low Byte for PC<7:0>								0000 0000	0000 0000	***** r r r r	
01Ch	TBLPTRU	-	-	-	-	-	-	-	-	xxxx xxxx	uuuu uuuu	***** r r r r	
01Dh	TBLPTRH	-	-	-	-	-	-	-	TBLPTR[12:8]	..xx xxxx	..uu uuuu	***** r r r r	
01Eh	TBLPTRL	Program Memory Table Pointer Low Byte (TBLPTR<7:0>)								xxxx xxxx	uuuu uuuu	***** r r r r	
01Fh	TBLDH	Program Memory Table Latch High Byte								xxxx xxxx	uuuu uuuu	***** r r r r	
020h	TBLDL	Program Memory Table Latch Low Byte								xxxx xxxx	uuuu uuuu	***** r r r r	
021h	PRODH	Product Register of Multiply High Byte								xxxx xxxx	uuuu uuuu	***** r r r r	
022h	PRODL	Product Register of Multiply Low Byte								xxxx xxxx	uuuu uuuu	***** r r r r	
023h	INTE0	GIE	TA1CIE	ADIE	WDTIE	TB1IE	TMAIE	E1IE	E0IE	0000 0000	0uuu uuuu	***** r r r r	
024h	INTE1	TA1IE	SPIIE	TXIE	RCIE	I2CERIE	I2CIE	E3IE	E2IE	0000 0000	uuuu uuuu	***** r r r r	
025h	INTE2	TA2IE	TA2CIE	TC11IE	TC10IE	TX2IE	RC2IE	-	BOR2IE	0000 0000	uuuu uuuu	***** r r r r	
026h	INTF0	-	TA1CIF	ADIF	WDTIF	TB1IF	TMAIF	E1IF	E0IF	.000 0000	.uuu uuuu	***** r r r r	
027h	INTF1	TA1IF	SPIIF	TXIF	RCIF	I2CERIF	I2CIF	E3IF	E2IF	0000 0000	uuuu uuuu	***** r,r,r,r	
028h	INTF2	TA2IF	TA2CIF	TC1IF	TC0IF	TX2IF	RC2IF	-	BOR2IF	0000 0000	uuuu uuuu	***** r r r r	
029h	WREG	Working Register								xxxx xxxx	uuuu uuuu	***** r r r r	
02Ah	BSRCN	-	-	-	-	-	-	-	BSR[1:0]	.... xxxx	.... uuuu	***** r r r r	
02Bh	MSTAT	-	-	-	C	DC	N	OV	Z	...x xxxx	...u uuuu	***** r r r r	
02Ch	PSTAT	BOR	PD	TO	IDL	RST	SKERR	BOR2LV	GCRstIF	\$000 \$000	uu\$u u\$uu	rw0,rw0,rw0,rw0,rw0,r,r,rw0	
031h	BIECN	1	-	-	ENBVD	VPPHV	ENBCP	BIEWR	BIERD	1.00 \$000	1.00 \$uuu	r1,-,*,*,*,*,*	
032h	BIEARH	-	-	1	1	1	1	1	1	0.xx xxxx	u.uu uuuu	***** r r r r	
033h	BIEARL	BIE Address Register as BIEAL[5:0]								xxxx xxxx	uuuu uuuu	***** r r r r	
034h	BIEDRH	BIE High Byte Data Register								xxxx xxxx	uuuu uuuu	***** r r r r	
035h	BIEDRL	BIE Low Byte Data Register								xxxx xxxx	uuuu uuuu	***** r r r r	
036h	PWRCN	ENBGR	LDOC[2:0]		LDOM[1:0]		ENLDO	CSFON		1000 0000	uuuu uu0u	***** r r r r	
037h	OSCCN0	OSCS[1:0]		DHS[1:0]		DMS[2:0]		CUPS		0000 0000	uuuu uuuu	***** r r r r	
038h	OSCCN1	CCOPT	LCPS	DADC[1:0]		DTMB[1:0]		TMBS	LCDS	0000 0000	uuuu uu.	***** r r r r	
039h	OSCCN2	DLCD[1:0]		ENXT	XTS[1:0]		HAOM[1:0]		ENHAO	0000 0001	uuuu uu01	***** r r r r	
03Ah	CSFCN0	SKRST	HAOTR[6:0]								.1. ....	.... ....	***** r,r,r,r,r,r,r
03Bh	CSFCN1	BOR_TH[2:0]				BORS		ENBOR2		...0 0011		uuuu uuuu	***** r,r,r,r

表 5-1 資料記憶體列表

# HY17P58

## Embedded 18-Bit ΣADC 8-Bit RISC-like Mixed Signal Microcontroller



"0"no use,"1"read/write,"w"write,"r"read,"r0"only read 0,"r1"only read 1,"w0"only write 0,"w1"only write 1  
"\$"for event status,"-"unimplemented bit,"x"unknown,"u"unchanged,"d"depends on condition

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	ARST	IRST	R/W		
03Eh	WDTCN	ENBZ	BZS	DBZ[1:0]		ENWDT	DWDIT[2:0]			0000 0000	uuuu \$000	-,*rw 1,*		
03Fh	AD1H	ADC1 conversion high byte data register												
040h	AD1M	ADC1 conversion middle byte data register												
041h	AD1L	ADC1 conversion low byte data register												
042h	AD1CN0	ENAD1				OSR[3:0]			CMFR	000. 0000	uuu. uuuu	*****		
043h	AD1CN1			VREGN			ADGN[2:0]			xxxx xxxx	uuuu uuuu	*****		
044h	AD1CN2	INIS1				DCSET[3:0]			xxxx xxxx	uuuu uuuu	*****			
045h	AD1CN3	INF[3:0]			INN[3:0]					xxxx xxxx	uuuu uuuu	*****		
046h	AD1CN4	VRH[1:0]	VRL[1:0]	INX[1:0]	VRIS	INIS				0000 0000	uuuu uuuu	*****		
047h	AD1CN5	ENACM	ENV12	VCMS	LDOPL	-	ENTPS	TPSCH			0000 0000	uuuu uuuu	*****	
048h	LVDCN			PWRS	LVDS[3:0]			LVDO			0000 0000	uuuu uuuu	*****	
049h	BIACN0	ENPK	OP1OS[2]	ENPKD	PKRST	ENLPF	LPFS[1:0]	ENREFO			0000 0000	uuuu uuuu	*****	
04Ah	DACCN0	DANS[2:0]			DAPS[3:0]					0000 0000	uuuu uuuu	*****		
04Bh	DACCN1			DADCS	DALH	DAOE[1:0]	ENDA			0000 0000	uuuu uuuu	*****		
04Ch	DACCN2	DABIT[7:0]									0000 0000	uuuu uuuu	*****	
04Dh	OP1CN0						OP1OS[1:0]	ENOP1			0000 0000	uuuu uuuu	*****	
04Eh	OP1NET	OP1PS[2:0]			OP1NS[2:0]					0000 0000	uuuu uuuu	*****		
04Fh	OP2CN0						OP2OS[1:0]	ENOP2			0000 0000	uuuu uuuu	*****	
050h	OP2NET	OP2PS[3:0]			OP2NS[2:0]					0000 0000	uuuu uuuu	*****		
051h	PGACN0	ENCHP	CHM[1:0]	ENHS	-	ENPGA[1:0]				0000 0000	uuuu uuuu	*****		
052h	PGACN1			GAINS[1:0]		OPDIEN	-			0000 0000	uuuu uuuu	*****		
053h	PGANET1	LNOP1NS[7:0]									0000 0000	uuuu uuuu	*****	
054h	PGANET2	LNOP1PS[7:0]									0000 0000	uuuu uuuu	*****	
055h	PGANET3	LNOP2NS[7:0]									0000 0000	uuuu uuuu	*****	
056h	PGANET4	LNOP2PS[7:0]									0000 0000	uuuu uuuu	*****	
057h	PGANET5	LNOP2OS[2:0]		OPCS	LNOP1OS[2:0]				0000 0000	uuuu uuuu	*****			
058h	TMA1CN	ENTMA1	TMACL1	TMAS1	DTMA1[2:0]		-	-	0000 00.0	u0uu uu.u	*rw 1,*			
059h	TMA1R	TMA1 counter Register												
05Ah	TMA1C	TMA1C counter Register												
05Bh	TB1Flag			PWM7A	PWM6A	PWM5A	PWM4A	PWM3A	PWM2A	PWM1A	.000 0000	.uuu uuuu	-,r,r,r r,r,r,r	
05Ch	TB1CN0	ENTB1	TB1M[1:0]	TB1RT[1:0]	TB1CL	PWMO1	PWMO0			0000 0000	uuuu u0uu	****,rw 1,*		
05Dh	TB1CN1	PA1IV	PWMA1[2:0]		PA0IV	PWMA0[2:0]				0000 0000	uuuu uuuu	*****		
05Eh	TB1RH	TimerB1 counter Register [15:8]												
05Fh	TB1RL	TimerB1 counter Register [7:0]												
060h	TB1C0H	TimerB1 counter Condition Register [15:8]												
061h	TB1C0L	TimerB1 counter Condition Register [7:0]												
062h	TB1C1H	TimerB1 counter Condition Register [15:8]												
063h	TB1C1L	TimerB1 counter Condition Register [7:0]												
064h	TB1C2H	TimerB1 counter Condition Register [15:8]												
065h	TB1C2L	TimerB1 counter Condition Register [7:0]												
066h	TC1CN0	TC1S[1:0]					CP12P	CP11P	TCEN			0000 0000	uuuu uuuu	uuuu uuuu
067h	TC1CN1	CP1R	CPSS	CP1S[1:0]		CP1PS[3:0]					0000 0000	uuuu uuuu	uuuu uuuu	
068h	TC10RH	Capture 0 High Byte Data Register												
069h	TC10RL	Capture 0 Low Byte Data Register												
06Ah	TC11RH	Capture 1 High Byte Data Register												
06Bh	TC11RL	Capture 1 Low Byte Data Register												
06Ch	PT1	PT1.7	PT1.6	PT1.5	PT1.4	PT1.3	PT1.2	PT1.1	PT1.0	xxxx xxxx	xxxx xxxx	*****		
06Dh	TRISC1	TC1.7	TC1.6	TC1.5	TC1.4	TC1.3	TC1.2	TC1.1	TC1.0	0000 0000	uuuu uuuu	*****		
06Eh	PT1DA	DA1.7	DA1.6	DA1.5	DA1.4	DA1.3	DA1.2	DA1.1	DA1.0	1111 1111	uuuu uuuu	*****		
06Fh	PT1PU	PU1.7	PU1.6	PU1.5	PU1.4	PU1.3	PU1.2	PU1.1	PU1.0	0000 0000	uuuu uuuu	*****		
070h	PT1M1	-	-	-	-	INTEG1[1:0]		INTEG0[1:0]		0000 0000	uuuu uuuu	*****		
071h	PT1M2	-	PM1.7[0]	-	PM1.6[0]	-	PM1.5[0]	-	PM1.4[0]	xxxx xxxx	xxxx xxxx	*****		
072h	PT1INT	INTEG7	INTEG6	INTEG5	INTEG4	INTEG3	INTEG2	-	-	0000 0000	uuuu uuuu	*****		
073h	PT1INTE	INTE1.7	INTE1.6	INTE1.5	INTE1.4	-	-	-	-	0000 0000	uuuu uuuu	*****		
074h	PT1INTF	INTF1.7	INTF1.6	INTF1.5	INTF1.4	-	-	-	-	0000 0000	uuuu uuuu	*****		

表 5-2 資料記憶體列表(續)

# HY17P58

## Embedded 18-Bit ΣADC 8-Bit RISC-like Mixed Signal Microcontroller



“-”no use,“r”read/write,“w”write,“r”read,“r0”only read 0,“r1”only read 1,“w0”only write 0,“w1”only write 1  
“\$”for event status,“.”unimplemented bit,“x”unknown,“u”unchanged,“d”depends on condition

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	ARST	IRST	R/W
075h	PT2	PT2.7	PT2.6	PT2.5	PT2.4	PT2.3	PT2.2	PT2.1	PT2.0	0000 0000	uuuu uuuu	***** 1 1 1 1 1 1 1
076h	TRISC2	TC2.7	TC2.6	TC2.5	TC2.4	TC2.3	TC2.2	TC2.1	TC2.0	0000 0000	uuuu uuuu	***** 1 1 1 1 1 1 1
077h	PT2DA	DA2.7	DA2.6	DA2.5	DA2.4	DA2.3	DA2.2	DA2.1	DA2.0	1111 1111	uuuu uuuu	***** 1 1 1 1 1 1 1
078h	PT2PU	PU2.7	PU2.6	PU2.5	PU2.4	PU2.3	PU2.2	PU2.1	PU2.0	0000 0000	uuuu uuuu	***** 1 1 1 1 1 1 1
07Bh	PT2INT	INTG2.7	INTG2.6	INTG2.5	INTG2.4	INTG2.3	INTG2.2	INTG2.1	INTG2.0	0000 0000	uuuu uuuu	***** 1 1 1 1 1 1 1
07Ch	PT2INTE	INTE2.7	INTE2.6	INTE2.5	INTE2.4	INTE2.3	INTE2.2	INTE2.1	INTE2.0	0000 0000	uuuu uuuu	***** 1 1 1 1 1 1 1
07Dh	PT2INTF	INTF2.7	INTF2.6	INTF2.5	INTF2.4	INTF2.3	INTF2.2	INTF2.1	INTF2.0	0000 0000	uuuu uuuu	***** 1 1 1 1 1 1 1
180h	LCDCN1	ENLCP	LCDV[2:0]			ENLB	SELPCLK	-	LCDPU	0000 00.0	uuuu uu.u	***** 1 1 1 1 1 1 1
181h	LCDCN2					LCDTYPE	LCDBL			0000 00..	uuuu uu..	***** 1 1 1 1 1 1 1
182h	LCDCN3	SCM3[1:0]		SCM2[1:0]		SCM1[1:0]		SCM0[1:0]		0000 0000	uuuu uuuu	***** 1 1 1 1 1 1 1
183h	LCDCN4	SSG21	SSG20	SSG19	SSG18	SSG17	SSG16	SSG15	SSG14	0000 0000	uuuu uuuu	***** 1 1 1 1 1 1 1
184h	LCDCN5	SSG41	SSG40	SSG39	SSG38	SSG37	SSG36	SSG35	SSG34	0000 0000	uuuu uuuu	***** 1 1 1 1 1 1 1
185h	LCDCN6	SSG5[1:0]		SSG4[1:0]		SSG3[1:0]		SSG2[1:0]		0000 0000	uuuu uuuu	***** 1 1 1 1 1 1 1
186h	LCDCN7	SSG9[1:0]		SSG8[1:0]		SSG7[1:0]		SSG6[1:0]		0000 0000	uuuu uuuu	***** 1 1 1 1 1 1 1
187h	LCDCN8	SSG13[1:0]		SSG12[1:0]		SSG11[1:0]		SSG10[1:0]		0000 0000	uuuu uuuu	***** 1 1 1 1 1 1 1
188h	LCDCN9	SSG25[1:0]		SSG24[1:0]		SSG23[1:0]		SSG22[1:0]		0000 0000	uuuu uuuu	***** 1 1 1 1 1 1 1
189h	LCDCN10	SSG29[1:1]		SSG28[1:1]		SSG27[1:1]		SSG26[1:1]		0000 0000	uuuu uuuu	***** 1 1 1 1 1 1 1
18Ah	LCDCN11	SSG33[1:1]		SSG32[1:1]		SSG31[1:1]		SSG30[1:1]		0000 0000	uuuu uuuu	***** 1 1 1 1 1 1 1
18Bh	LCD0	LCD SEG3[4:7] data				LCD SEG2[3:0] data				xxxx xxxx	uuuu uuuu	***** 1 1 1 1 1 1 1
18Ch	LCD1	LCD SEG5[4:7] data				LCD SEG4[3:0] data				xxxx xxxx	uuuu uuuu	***** 1 1 1 1 1 1 1
18Dh	LCD2	LCD SEG7[7:4] data				LCD SEG6[3:0] data				xxxx xxxx	uuuu uuuu	***** 1 1 1 1 1 1 1
18Eh	LCD3	LCD SEG9[7:4] data				LCD SEG8[3:0] data				xxxx xxxx	uuuu uuuu	***** 1 1 1 1 1 1 1
18Fh	LCD4	LCD SEG11[7:4] data				LCD SEG10[3:0] data				xxxx xxxx	uuuu uuuu	***** 1 1 1 1 1 1 1
190h	LCD5	LCD SEG13[7:4] data				LCD SEG12[3:0] data				xxxx xxxx	uuuu uuuu	***** 1 1 1 1 1 1 1
191h	LCD6	LCD SEG15[4:7] data				LCD SEG14[3:0] data				xxxx xxxx	uuuu uuuu	***** 1 1 1 1 1 1 1
192h	LCD7	LCD SEG17[4:7] data				LCD SEG16[3:0] data				xxxx xxxx	uuuu uuuu	***** 1 1 1 1 1 1 1
193h	LCD8	LCD SEG19[4:7] data				LCD SEG18[3:0] data				xxxx xxxx	uuuu uuuu	***** 1 1 1 1 1 1 1
194h	LCD9	LCD SEG21[4:7] data				LCD SEG20[3:0] data				xxxx xxxx	uuuu uuuu	***** 1 1 1 1 1 1 1
195h	LCD10	LCD SEG23[4:7] data				LCD SEG22[3:0] data				xxxx xxxx	uuuu uuuu	***** 1 1 1 1 1 1 1
196h	LCD11	LCD SEG25[4:7] data				LCD SEG24[3:0] data				xxxx xxxx	uuuu uuuu	***** 1 1 1 1 1 1 1
197h	LCD12	LCD SEG27[4:7] data				LCD SEG26[3:0] data				xxxx xxxx	uuuu uuuu	***** 1 1 1 1 1 1 1
198h	LCD13	LCD SEG29[4:7] data				LCD SEG28[3:0] data				xxxx xxxx	uuuu uuuu	***** 1 1 1 1 1 1 1
199h	LCD14	LCD SEG31[4:7] data				LCD SEG30[3:0] data				xxxx xxxx	uuuu uuuu	***** 1 1 1 1 1 1 1
19Ah	LCD15	LCD SEG33[4:7] data				LCD SEG32[3:0] data				xxxx xxxx	uuuu uuuu	***** 1 1 1 1 1 1 1
19Bh	LCD16	LCD SEG35[4:7] data				LCD SEG34[3:0] data				xxxx xxxx	uuuu uuuu	***** 1 1 1 1 1 1 1
19Ch	LCD17	LCD SEG37[4:7] data				LCD SEG36[3:0] data				xxxx xxxx	uuuu uuuu	***** 1 1 1 1 1 1 1
19Dh	LCD18	LCD SEG39[4:7] data				LCD SEG38[3:0] data				xxxx xxxx	uuuu uuuu	***** 1 1 1 1 1 1 1
19Eh	LCD19	LCD SEG41[4:7] data				LCD SEG40[3:0] data				xxxx xxxx	uuuu uuuu	***** 1 1 1 1 1 1 1
19Fh	PT4	PT4.7	PT4.6	PT4.5	PT4.4	-	-	-	-	xxxx xxxx	xxxx xxxx	***** 1 1 1 1 1 1 1
1A1h	PT4DA	DA4.7	DA4.6	DA4.5	DA4.4	-	-	-	-	1111 0000	uuuu uuuu	***** 1 1 1 1 1 1 1
1A2h	PT4PU	PU4.7	PU4.6	PU4.5	PU4.4	-	-	-	-	0000 0000	uuuu uuuu	***** 1 1 1 1 1 1 1
1A5h	PT4INT	INTG4.7	INTG4.6	INTG4.5	INTG4.4	-	-	-	-	0000 0000	uuuu uuuu	***** 1 1 1 1 1 1 1
1A6h	PT4INTE	INTE4.7	INTE4.6	INTE4.5	INTE4.4	-	-	-	-	0000 0000	uuuu uuuu	***** 1 1 1 1 1 1 1
1A7h	PT4INTF	INTF4.7	INTF4.6	INTF4.5	INTF4.4	-	-	-	-	0000 0000	uuuu uuuu	***** 1 1 1 1 1 1 1
1AAh	PT5	-	-	-	-	PT5.3	PT5.2	PT5.1	PT5.0	xxxx xxxx	xxxx xxxx	***** 1 1 1 1 1 1 1
1ACh	PT5DA	-	-	-	-	DA5.3	DA5.2	DA5.1	DA5.0	0000 1111	uuuu uuuu	***** 1 1 1 1 1 1 1
1ADh	PT5PU	-	-	-	-	PU5.3	PU5.2	PU5.1	PU5.0	0000 0000	uuuu uuuu	***** 1 1 1 1 1 1 1
1B0h	PT5INT	-	-	-	-	INTG5.3	INTG5.2	INTG5.1	INTG5.0	0000 0000	uuuu uuuu	***** 1 1 1 1 1 1 1
1B1h	PT5INTE	-	-	-	-	INTE5.3	INTE5.2	INTE5.1	INTE5.0	0000 0000	uuuu uuuu	***** 1 1 1 1 1 1 1
1B2h	PT5INTF	-	-	-	-	INTF5.3	INTF5.2	INTF5.1	INTF5.0	0000 0000	uuuu uuuu	***** 1 1 1 1 1 1 1
1B5h	PT6	PT6.7	PT6.6	PT6.5	PT6.4	PT6.3	PT6.2	PT6.1	PT6.0	xxxx xxxx	uuuu uuuu	***** 1 1 1 1 1 1 1
1B6h	TRISC6	TC6.7	TC6.6	TC6.5	TC6.4	TC6.3	TC6.2	TC6.1	TC6.0	0000 0000	uuuu uuuu	***** 1 1 1 1 1 1 1
1B7h	PT6DA	DA6.7	DA6.6	DA6.5	DA6.4	DA6.3	DA6.2	DA6.1	DA6.0	1111 1111	uuuu uuuu	***** 1 1 1 1 1 1 1
1B8h	PT6PU	PU6.7	PU6.6	PU6.5	PU6.4	PU6.3	PU6.2	PU6.1	PU6.0	0000 0000	uuuu uuuu	***** 1 1 1 1 1 1 1
1B9h	PT7	PT7.7	PT7.6	PT7.5	PT7.4	PT7.3	PT7.2	PT7.1	PT7.0	xxxx xxxx	uuuu uuuu	***** 1 1 1 1 1 1 1
1BAh	TRISC7	TC7.7	TC7.6	TC7.5	TC7.4	TC7.3	TC7.2	TC7.1	TC7.0	0000 0000	uuuu uuuu	***** 1 1 1 1 1 1 1
1BBh	PT7DA	DA7.7	DA7.6	DA7.5	DA7.4	DA7.3	DA7.2	DA7.1	DA7.0	1111 1111	uuuu uuuu	***** 1 1 1 1 1 1 1
1BCh	PT7PU	PU7.7	PU7.6	PU7.5	PU7.4	PU7.3	PU7.2	PU7.1	PU7.0	0000 0000	uuuu uuuu	***** 1 1 1 1 1 1 1

表 5-3 資料記憶體列表(續)

# HY17P58

## Embedded 18-Bit ΣADC 8-Bit RISC-like Mixed Signal Microcontroller



“-”no use, “\*”read/write, “w”write, “r”read, “r0”only read 0, “r1”only read 1, “w0”only write 0, “w1”only write 1  
“\$”for event status, “.”unimplemented bit, “x”unknown, “u”unchanged, “d”depends on condition

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	ARST	IRST	R/W			
1BDh	PT8	PT8.7	PT8.6	PT8.5	PT8.4	PT8.3	PT8.2	PT8.1	PT8.0	xxxx xxxx	uuuu uuuu	***** r r r r			
1BEh	TRISC8	TC8.7	TC8.6	TC8.5	TC8.4	TC8.3	TC8.2	TC8.1	TC8.0	0000 0000	uuuu uuuu	***** r r r r			
1BFh	PT8DA	DA8.7	DA8.6	DA8.5	DA8.4	DA8.3	DA8.2	DA8.1	DA8.0	1111 1111	uuuu uuuu	***** r r r r			
1C0h	PT8PU	PU8.7	PU8.6	PU8.5	PU8.4	PU8.3	PU8.2	PU8.1	PU8.0	0000 0000	uuuu uuuu	***** r r r r			
1C1h	PT9	PT9.7	PT9.6	PT9.5	PT9.4	PT9.3	PT9.2	PT9.1	PT9.0	xxxx xxxx	uuuu uuuu	***** r r r r			
1C2h	TRISC9	TC9.7	TC9.6	TC9.5	TC9.4	TC9.3	TC9.2	TC9.1	TC9.0	0000 0000	uuuu uuuu	***** r r r r			
1C3h	PT9DA	DA9.7	DA9.6	DA9.5	DA9.4	DA9.3	DA9.2	DA9.1	DA9.0	1111 1111	uuuu uuuu	***** r r r r			
1C4h	PT9PU	PU9.7	PU9.6	PU9.5	PU9.4	PU9.3	PU9.2	PU9.1	PU9.0	0000 0000	uuuu uuuu	***** r r r r			
1C5h	PT10	PT10.7	PT10.6	PT10.5	PT10.4	PT10.3	PT10.2	PT10.1	PT10.0	xxxx xxxx	uuuu uuuu	***** r r r r			
1C6h	TRISC10	TC10.7	TC10.6	TC10.5	TC10.4	TC10.3	TC10.2	TC10.1	TC10.0	0000 0000	uuuu uuuu	***** r r r r			
1C7h	PT10DA	DA10.7	DA10.6	DA10.5	DA10.4	DA10.3	DA10.2	DA10.1	DA10.0	1111 1111	uuuu uuuu	***** r r r r			
1C8h	PT10PU	PU10.7	PU10.6	PU10.5	PU10.4	PU10.3	PU10.2	PU10.1	PU10.0	0000 0000	uuuu uuuu	***** r r r r			
1C9h	PT11	-	-	-	-	PT11.3	PT11.2	PT11.1	PT11.0	xxxx xxxx	uuuu uuuu	***** r r r r			
1CAh	TRISC11	-	-	-	-	TC11.3	TC11.2	TC11.1	TC11.0	0000 0000	uuuu uuuu	***** r r r r			
1CBh	PT11DA	-	-	-	-	DA11.3	DA11.2	DA11.1	DA11.0	0000 1111	uuuu uuuu	***** r r r r			
1CCh	PT11PU	-	-	-	-	PU11.3	PU11.2	PU11.1	PU11.0	0000 0000	uuuu uuuu	***** r r r r			
1CDh	PT11M2	-	-	-	-	-	-	-	-	0000 0000	uuuu uuuu	***** r r r r			
1CEh	SSPCN0	ENSSP	CKP	CKE	SMP	-	-	-	SSPM[1:0]	0000 ..00	uuuu ..uu	**** r r r r			
1CFh	SSPSTA0	SSPBY	SSPOV	-	-	-	-	-	BF	00.. ..0	uu.. ..u	** r r r r			
1D0h	SSPBUF0	SSP Receive/Transmit Buffer Register								xxxx xxxx	uuuu uuuu	***** r r r r			
1D1h	CFG0	-	-	-	-	-	GCRst	ENI2CT	ENI2C	0000 0000	.... .uuu	-,-,-,-,*** r r r r			
1D2h	ACT0	SLAVE	-	-	I2CER	START	STOP	I2CINT	ACK	0000 0000	uuuu uuuu	***** r r r r			
1D3h	STA0	MACTF	SACTF	RDBF	RWF	DFB	ACKF	GCF	ARBF	0001 0000	uuuu uuuu	***** r r r r			
1D4h	CRG0	CRG[7:0]								0000 0000	uuuu uuuu	***** r r r r			
1D5h	TOC0	I2CTF	DI2C[2:0]			I2CTL[3:0]				0000 0000	uuuu uuuu	***** r r r r			
1D6h	RDB0	RDB[7:1]							RDB[0]	xxxx xxxx	uuuu uuuu	***** r r r r			
1D7h	TDB0	TDB0[7:1]							TDB0[0]	xxxx xxxx	uuuu uuuu	***** r r r r			
1D8h	SID0	SID0[7:1],The corresponding address of the 7-bit mode								SID0V[0]	0000 0000	uuuu uuuu	***** r r r r		
1D9h	UR0CN	ENSP	ENTX	TX9	TX9D	PARITY	-	-	WUE	0000 0..0	uuuu u..u	***** r r r r			
1DAh	UR0STA	-	RC9D	PERR	FERR	OERR	RCIDL	TRMT	ABDOVF	.000 0010	.uuu uuuu	-,r,r,r,r,r,r,rw0			
1DBh	BA0CN	-	-	-	-	ENCR	RC9	ENADD	ENABD	.... 0000	.... uuuu	-,-,-,-,***! r r r r			
1DCh	BG0RH	-	-	-	Baud Rate Generator Register High Byte					...x xxxx	...u uuuu	-,-,-,-,*** r r r r			
1DDh	BG0RL	Baud Rate Generator Register Low Byte								xxxx xxxx	uuuu uuuu	***** r r r r			
1DEh	TX0R	UART Transmit Register											xxxx xxxx	uuuu uuuu	***** r r r r
1DFh	RC0REG	UART Receive Register											xxxx xxxx	uuuu uuuu	***** r r r r
1E0h	UR2CN	ENSP2	ENTX2	TX92	TX9D2	PARITY2	-	-	WUE2	0000 0..0	uuuu u..u	***** r r r r			
1E1h	UR2STA	-	RC9D2	PERR2	FERR2	OERR2	RCIDL2	TRMT2	ABDOVF2	.000 0010	.uuu uuuu	-,r,r,r,r,r,r,rw0			
1E2h	BA2CN	-	-	-	-	ENCR2	RC92	ENADD2	ENABD2	.... 0000	.... uuuu	-,-,-,-,***! r r r r			
1E3h	BG2RH	-	-	-	Baud Rate Generator Register High Byte					...x xxxx	...u uuuu	-,-,-,-,*** r r r r			
1E4h	BG2RL	Baud Rate2 Generator Register Low Byte								xxxx xxxx	uuuu uuuu	***** r r r r			
1E5h	TX2R	UART2 Transmit Register											xxxx xxxx	uuuu uuuu	***** r r r r
1E6h	RC2REG	UART2 Receive Register											xxxx xxxx	uuuu uuuu	***** r r r r
1E7h	TMA2CN	ENTMA2	TMACL2	TMAS2	DTMA2[2:0]			-	-	0000 00..	u0uu uu..	*,rw1,*,*,*,*-			
1E8h	TMA2R	TMA2 counter Register											0000 0000	uuuu uuuu	rw0,rw0,rw0,rw0,rw0,rw0,rw0,rw0
1E9h	TMA2C	TMA2C counter Register											0000 0000	uuuu uuuu	rw0,rw0,rw0,rw0,rw0,rw0,rw0,rw0
1EAh	LEDCN			ENLEDP	VGGS	ENBLOUT	LEDS[2:0]			0000 0000	uuuu uuuu	***** r r r r			
1EBh	IQ0								ENIQ	0000 0000	uuuu uuuu	***** r r r r			
1ECh	IQ1	IQOffset[5:0]						IQMODE	IQINV	0000 0000	uuuu uuuu	***** r r r r			
1EDh	DGCON1				DGRST	DGDiv[2:0]		DGEN	0000 0000	uuuu uuuu	***** r r r r				
1EEh	DGCON2			DGRP[5:0]					0000 0000	uuuu uuuu	***** r r r r				
080h ~ 0FFh		SRAM as 128Byte											uuuu uuuu	uuuu uuuu	***** r r r r
100h ~ 17Fh		SRAM as 128Byte											uuuu uuuu	uuuu uuuu	***** r r r r
200h ~ 2FFh		SRAM as 256Byte											uuuu uuuu	uuuu uuuu	***** r r r r
300h ~ 33Fh		SRAM as 64Byte, 300h~33Fh set for hardware sinewave first.											uuuu uuuu	uuuu uuuu	***** r r r r

## 6. 電氣特性

### Absolute Maximum Ratings :

Absolute maximum ratings over operating free-air temperature (unless otherwise noted)

Voltage applied at VDD to VSS .....	-0.2 V to 6.0 V
Voltage applied to any pin .....	-0.2 V to VDD + 0.3 V
Voltage applied to RST/VPP pin .....	-0.2 V to 8.75 V
Diode current at any device terminal .....	±2 mA
Storage temperature, Tstg: (unprogrammed device) .....	-55°C to 155°C
(programmed device) .....	-40°C to 85°C
Total power dissipation.....	0.5w
Maximum output current sink by any I/O pin.....	.20mA

### 6.1. Recommended operating conditions

TA = -40°C ~ 85°C, unless otherwise noted

Sym.	Parameter		Test Conditions	Min.	Typ.	Max.	Unit		
VDD	Supply Voltage		All digital peripherals and CPU	2.2		5.5	V		
VDDA	Supply Voltage		Analog peripherals	2.4		4.5			
VSS	Supply Voltage			0		0			
XT	External	Watch crystal	V <sub>DD</sub> = 2.2V~5.5V, ENXT[0]=1		32768		Hz		
		Ceramic resonator		XTS[1:0]=10	450K			8M	
	Oscillator	Crystal	XTS[1:0]=11	1M		8M			
		Frequency	Ceramic resonator	V <sub>DD</sub> = 3.6V~5.5V, ENXT[0]=1	XTS[1:0]=10	450K			16M
			Crystal	XTS[1:0]=11	1M			16M	

### 6.2. Internal RC Oscillator

TA = 25°C, VDD = 3.0V, unless otherwise noted

Sym.	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
HAO	High Speed Oscillator frequency	ENHAO[0]=1, HAOM[1:0]=00b	-20%	1.6	+20%	MHz
		ENHAO[0]=1, HAOM[1:0]=01b	-20%	3.2	+20%	
		ENHAO[0]=1, HAOM[1:0]=11b	-20%	7.0	+20%	
LPO	Low Power Oscillator frequency	VDD supply voltage be enable LPO	-20%	14.5	+20%	KHz

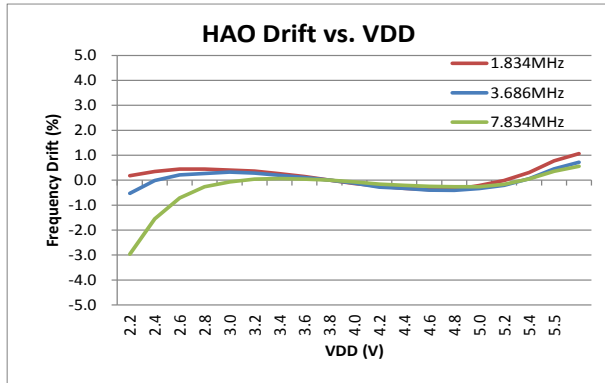


Figure 6.2- 1HAO vs. VDD

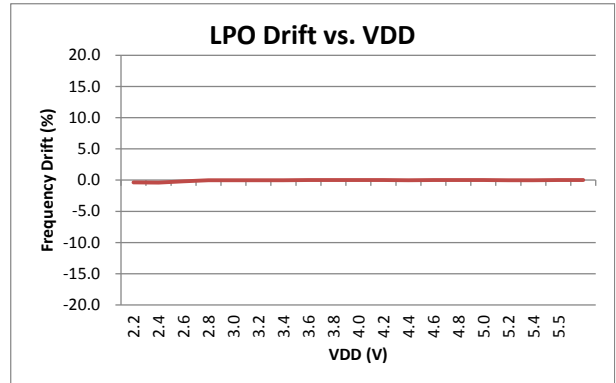


Figure 6.2- 2 LPO vs. VDD

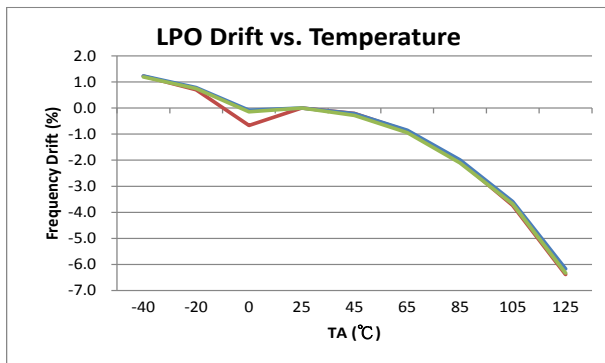


Figure 6.2- 3LPO vs. Temperature

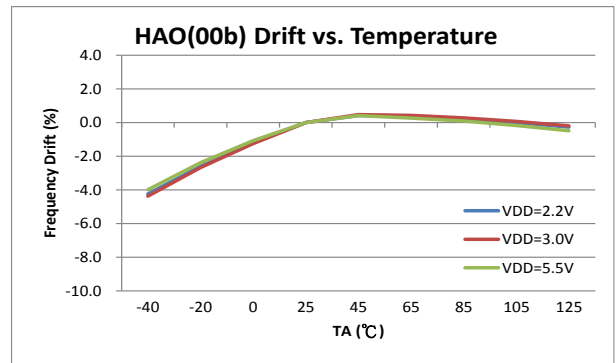


Figure 6.2- 4HAO(HAOM=00b) vs. Temperature

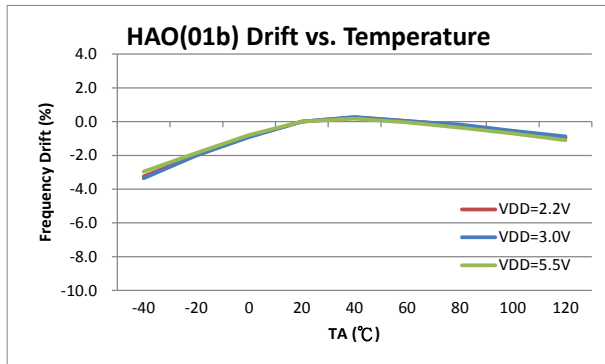


Figure 6.2- 5HAO(HAOM=01b) vs. Temperature

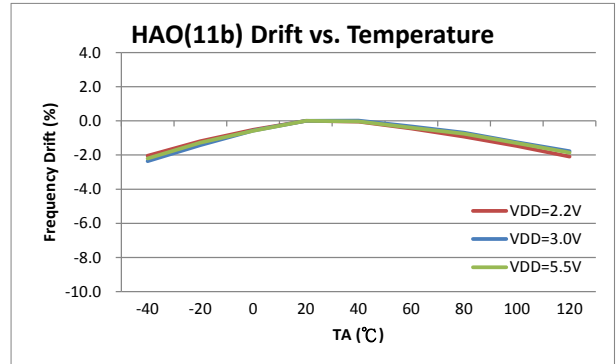


Figure 6.2- 6HAO(HAOM=10b) vs. Temperature



### 6.3. Supply current into VDD excluding peripherals current

TA = 25°C, VDD = 3.0V, OSC\_LPO = 14.5KHz, unless otherwise noted

Sym.	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
I <sub>AM1</sub>	Active mode 1	OSC_CY = off, OSC_HAO = 7.834MHz, CPU_CK = 7.834MHz		660		uA
I <sub>AM2</sub>	Active mode 2	OSC_CY = off, OSC_HAO = 3.686MHz, CPU_CK = 3.686MHz		360		uA
I <sub>AM3</sub>	Active mode 3	OSC_CY = off, OSC_HAO = 1.843MHz, CPU_CK = 1.843MHz		230		uA
I <sub>AM4</sub>	Active mode 4	OSC_CY = off, OSC_HAO = 1.843MHz, CPU_CK = 1.843MHz/2		185		uA
I <sub>LP1</sub>	Low Power 1	OSC_CY = off, OSC_HAO = off, CPU_CK = LPO,		1.6		uA
I <sub>LP2</sub>	Low Power 2	OSC_CY = off, OSC_HAO = off, CPU_CK = LPO, Idle state		0.8		uA
I <sub>LP3</sub>	Low Power 3	OSC_CY = off, OSC_HAO = off, CPU_CK = off, Sleep state		0.25		uA
I <sub>LP4</sub>	Low Power 4	OSC_CY = 32768, OSC_HAO = off, CPU_CK = 32768, Idle state		3.26		uA
I <sub>LP5</sub>	Low Power 5	OSC_CY = 32768, OSC_HAO = off, CPU_CK = off, Sleep state		1.39		uA

OSC\_CY : External Oscillator frequency.  
OSC\_HAO : Internal High Accuracy Oscillator frequency.  
CPU\_CK : CPU core work frequency.

TA = 25°C, VDD = 5.5V, OSC\_LPO = 14.5KHz, unless otherwise noted

Sym.	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
I <sub>AM1</sub>	Active mode 1	OSC_CY = off, OSC_HAO = 7.834MHz, CPU_CK = 7.834MHz		1200	1800	uA
I <sub>AM2</sub>	Active mode 2	OSC_CY = off, OSC_HAO = 3.686MHz, CPU_CK = 3.686MHz		720	1200	uA
I <sub>AM3</sub>	Active mode 3	OSC_CY = off, OSC_HAO = 1.843MHz, CPU_CK = 1.843MHz		500	1000	uA
I <sub>AM4</sub>	Active mode 4	OSC_CY = off, OSC_HAO = 1.843MHz, CPU_CK = 1.843MHz/2		400	800	uA
I <sub>LP1</sub>	Low Power 1	OSC_CY = off, OSC_HAO = off, CPU_CK = LPO,		4	10	uA
I <sub>LP2</sub>	Low Power 2	OSC_CY = off, OSC_HAO = off, CPU_CK = LPO, Idle state		2.5	5	uA
I <sub>LP3</sub>	Low Power 3	OSC_CY = off, OSC_HAO = off, CPU_CK = off, Sleep state		0.4	2	uA
I <sub>LP4</sub>	Low Power 4	OSC_CY = 32768, OSC_HAO = off, CPU_CK = 32768, Idle state		8.25		uA
I <sub>LP5</sub>	Low Power 5	OSC_CY = 32768, OSC_HAO = off, CPU_CK = off, Sleep state		4.36		uA

OSC\_CY : External Oscillator frequency.  
OSC\_HAO : Internal High Accuracy Oscillator frequency.  
CPU\_CK : CPU core work frequency.

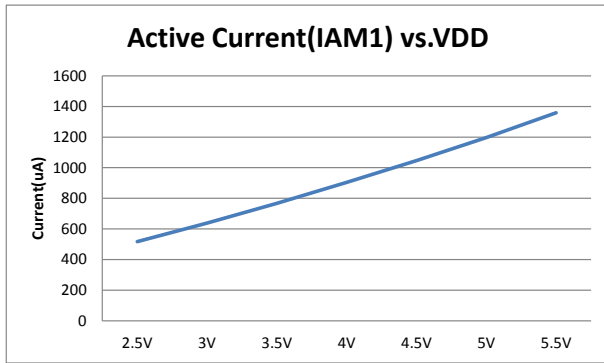


Figure 6.3- 1IAM1 vs. VDD

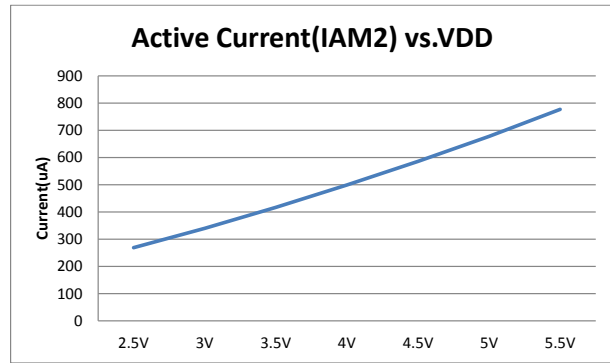


Figure 6.3- 2IAM2 vs. VDD

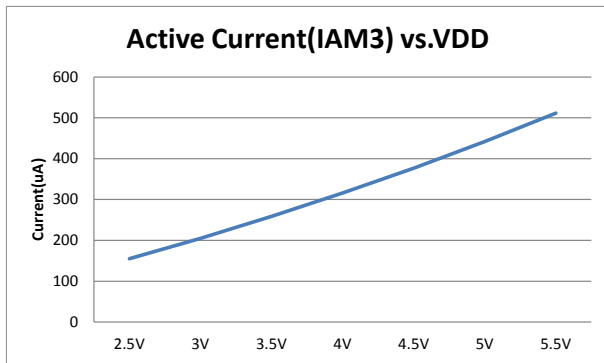


Figure 6.3- 3IAM3 vs. VDD

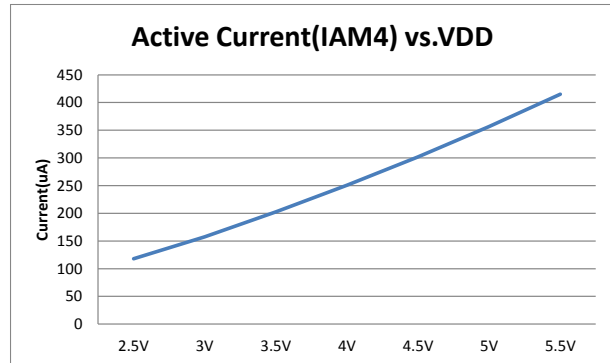


Figure 6.3- 4IAM4 vs. VDD

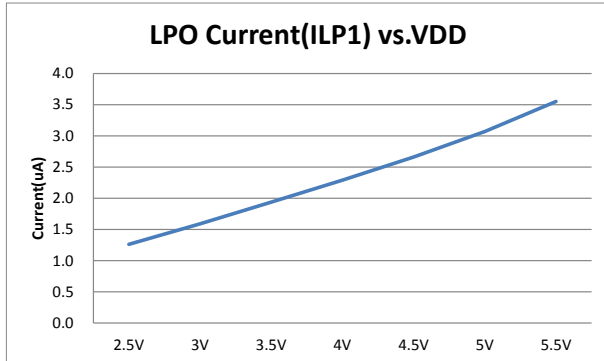


Figure 6.3- 5ILP1 vs. VDD

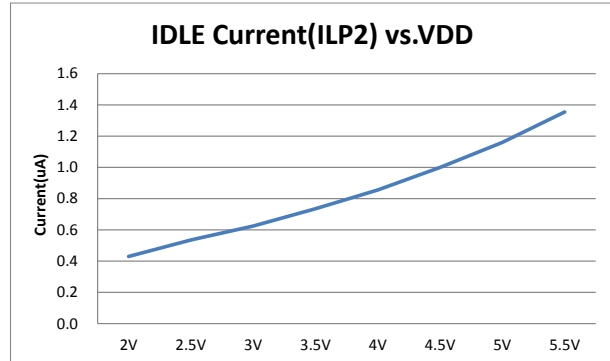


Figure 6.3- 6ILP2 vs. VDD

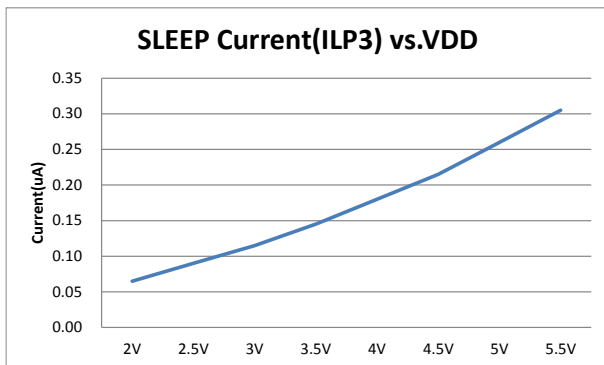


Figure 6.3- 7ILP3 vs. VDD

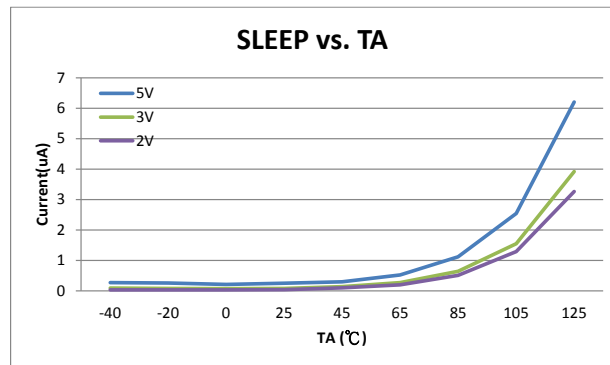


Figure 6.3- 8ILP3 vs. Temperature

## 6.4. Port

TA = 25°C, VDD = 3.0V, unless otherwise noted

Sym.	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
Input voltage and Schmitt trigger and leakage current and timing						
V <sub>IH</sub>	High-Level input voltage				2.1	V
V <sub>IL</sub>	Low-Level input voltage		0.9			
V <sub>hys</sub>	Input Voltage hysteresis(V <sub>IH</sub> - V <sub>IL</sub> )			0.8		V
ILKG	Leakage Current				0.1	uA
RPU	Port pull high resistance			60		kΩ
Output voltage and current and frequency						
V <sub>OH</sub>	High-level output voltage	VDD=3V, IOH=10mA,	VDD -0.4			V
		VDD=5V, IOH=15mA,	VDD -0.4			
V <sub>OL</sub>	Low-level output voltage	VDD=3V, IOH=10mA,			VSS +0.4	
		VDD=5V, IOH=15mA,			VSS +0.4	
I <sub>OH</sub>	High-level output source current (SEG port only)	VDD=3V, VOH =VDD -0.3			20	mA
		VDD=4V, VOH =VDD -0.4			40	
I <sub>OL</sub>	Low-level output sink current (SEG port only)	VDD=3V, VOL =VSS +0.3			20	
		VDD=4V, VOL =VSS +0.4			40	
I <sub>OH</sub>	High-level output source current (COM port only)	VDD=3V, VOH =VDD -0.3			20	mA
		VDD=4V, VOH =VDD -0.4			40	
I <sub>OL</sub>	Low-level output sink current (COM port only)	VDD=3V, VOL =VSS +0.3			20	
		VDD=4V, VOL =VSS +0.4			40	

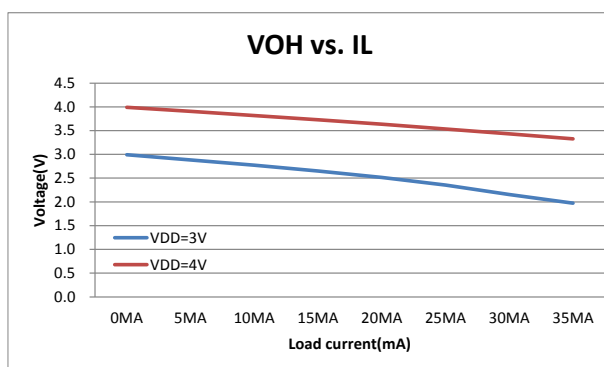


Figure6.4- 1V<sub>OH</sub> vs. I<sub>OH</sub>

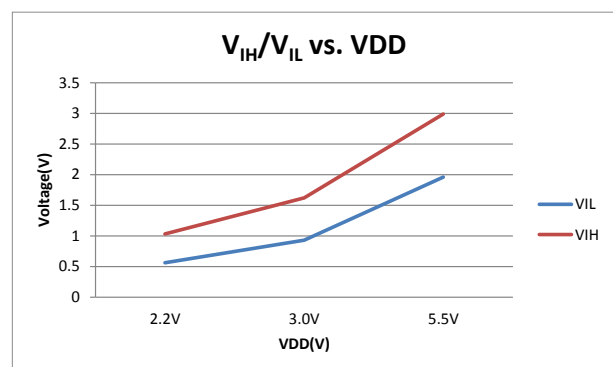


Figure6.4- 2V<sub>IH</sub>/V<sub>IL</sub> vs. VDD

# HY17P58

Embedded 18-Bit  $\Sigma\Delta$ ADC

8-Bit RISC-like Mixed Signal Microcontroller

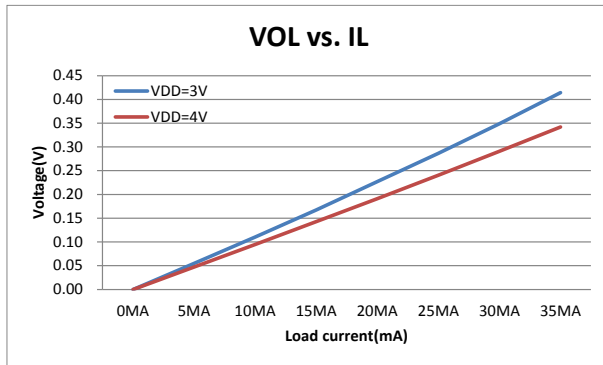


Figure6.4-  $3V_{OL}$  vs.  $I_o$

## 6.5. Reset(Brownout, External RST pin, Low Voltage Detect)

TA = 25°C, VDD = 3.0V, unless otherwise noted

Sym.	Parameter	Test Conditions	Min.	Typ.	Max.	Unit			
BOR1	Pulse length needed to accepted reset internally, td-LVR		2			uS			
	VDD Start Voltage to accepted reset internally (L→H), VLVR	TA = 25°C	1.15	1.48	1.75	V			
	VDD Start Voltage to accepted reset internally (L→H), VLVR,	TA = -40°C ~ 125 °C	TBD		TBD	V			
	Current consumption	VDD=3.3V		0.2		uA			
		VDD=5.5V		0.3		uA			
BOR2	Pulse length needed to accepted reset internally, td-LVR		2			uS			
	VDD Start Voltage to accepted reset internally (L→H)	BOR_TH[2:0]=001b, TA=25°C	-8%	1.98	+8%	V			
		BOR_TH[2:0]=001b, TA=-40°C~85°C	-8%		+8%	V			
	VDD Start Voltage to accepted reset internally (H→L)	BOR_TH[2:0]=001b, TA=25°C	-8%	1.93	+8%	V			
		BOR_TH[2:0]=001b, TA=-40°C~85°C	-8%		+8%	V			
	Hysteresis, VHYS-LVR			40		mV			
	VDD Start Voltage to accepted reset internally (L→H)	BOR_TH[2:0]=010b	-8%	2.2	+8%	V			
	VDD Start Voltage to accepted reset internally (L→H)	BOR_TH[2:0]=011b	-8%	2.47	+8%	V			
	VDD Start Voltage to accepted reset internally (L→H)	BOR_TH[2:0]=100b	-8%	2.7	+8%	V			
	VDD Start Voltage to accepted reset internally (L→H)	BOR_TH[2:0]=101b	-8%	2.97	+8%	V			
	VDD Start Voltage to accepted reset internally (L→H)	BOR_TH[2:0]=110b	-10%	3.6	+10%	V			
	VDD Start Voltage to accepted reset internally (L→H)	BOR_TH[2:0]=111b	-10%	3.95	+10%	V			
	Current consumption	VDD=3.3V		10		uA			
	VDD=5.5V		15		uA				
RST	Pulse length needed as RST/VPP pin to accepted reset internally, td-RST		2			uS			
	Input Voltage to accepted reset voltage			1.1		V			
	Reset release voltage			2		V			
LVD	Operation current, ILVD			2.5		uA			
	External input voltage to compare reference voltage		1.15	1.2	1.25	V			
	Compare reference voltage temperature drift	TA = -40°C ~ 85 °C	1.147		1.255	V			
	Detect VDD voltage rang by user option, VSVS VLDx[3:0]=1110b		-0.05	4.0	+0.05	V			
	Detect VDD voltage rang by user option, VSVS VLDx[3:0]=1101b			3.6					
	Detect VDD voltage rang by user option, VSVS VLDx[3:0]=1100b			3.3					
	Detect VDD voltage rang by user option, VSVS VLDx[3:0]=1011b			3.0					
	Detect VDD voltage rang by user option, VSVS VLDx[3:0]=1010b			2.9					
	Detect VDD voltage rang by user option, VSVS VLDx[3:0]=1001b			2.8					
	Detect VDD voltage rang by user option, VSVS VLDx[3:0]=1000b			2.7					
	Detect VDD voltage rang by user option, VSVS VLDx[3:0]=0111b			2.6					
	Detect VDD voltage rang by user option, VSVS VLDx[3:0]=0110b			2.5					
	Detect VDD voltage rang by user option, VSVS VLDx[3:0]=0101b			2.4					
	Detect VDD voltage rang by user option, VSVS VLDx[3:0]=0100b			2.3					
	Detect VDD voltage rang by user option, VSVS VLDx[3:0]=0011b			2.2					
	Detect VDD voltage rang by user option, VSVS VLDx[3:0]=0010b			2.1					
Detect VDD voltage rang by user option, VSVS VLDx[3:0]=0001b		2.0							
BOR1/BOR2 : Brownout Reset LVR : Low Voltage Reset of BOR LVD : Low Voltage Detect RST : External Reset pin									

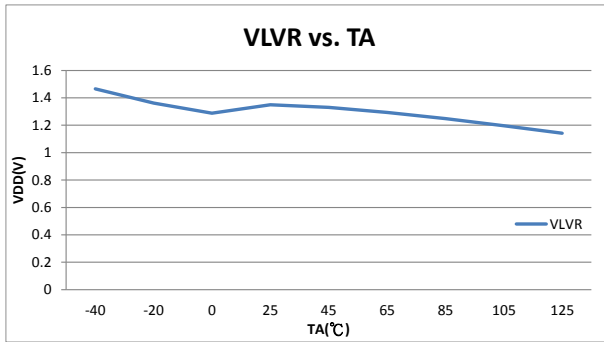


Figure6.5- 1 BOR1 vs. Temperature

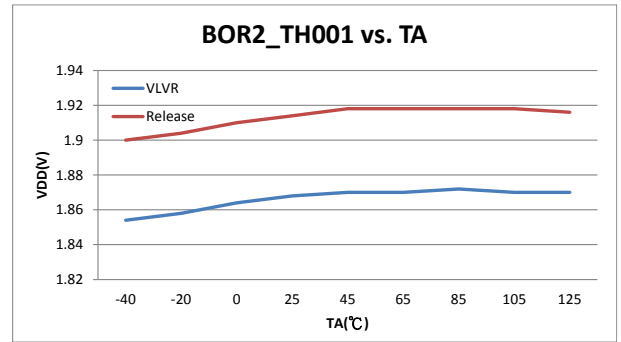


Figure6.5- 2 BOR2 vs. Temperature

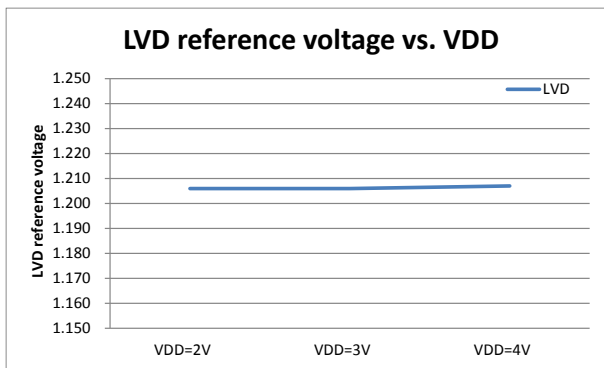


Figure6.5- 3 LVD reference voltage vs. VDD

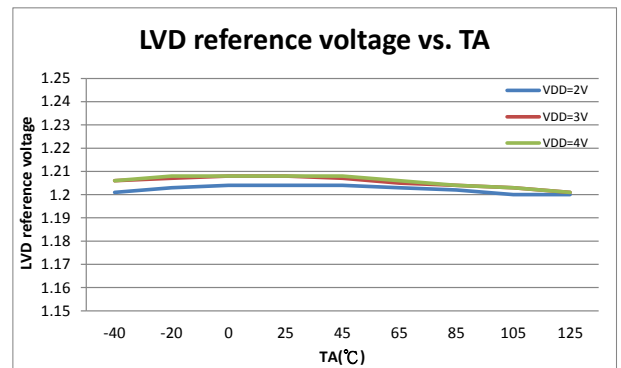


Figure6.5- 4 LVD reference voltage vs. Temperature

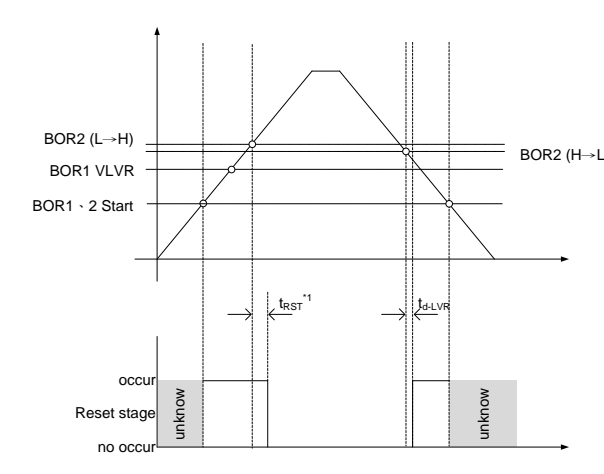


Figure6.5- 5 BOR reset diagram

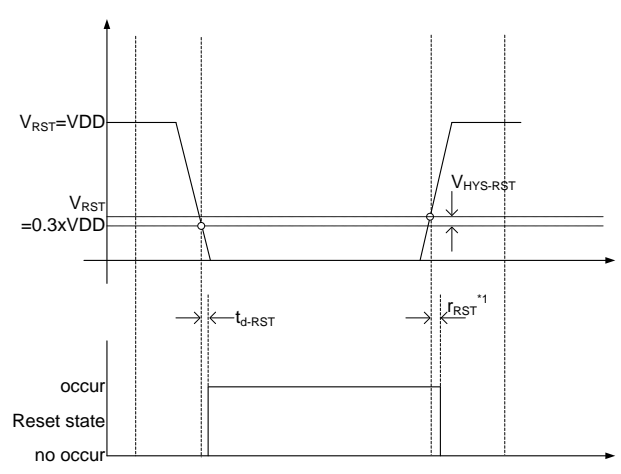


Figure6.5- 6 RST reset diagram

## 6.6. Power System

TA = 25°C, VDD = 3.0V, unless otherwise noted

Sym.	Parameter	Test Conditions		Min.	Typ.	Max.	Unit
VDDA	VDDA operation current, IVDDA	IL = 0mA	LDOC[2:0]=000b		20		uA
	Select VDDA output voltage	IL = 0.1mA, VDD ≥ VDDA+0.25V	LDOC [2:0]=000b	-5%	2.4	+5%	V
			LDOC [2:0]=001b		2.6		V
			LDOC [2:0]=010b		2.9		V
			LDOC [2:0]=011b		3.3		V
			LDOC [2:0]=100b		3.6		V
			LDOC [2:0]=101b		4.0		V
			LDOC [2:0]=110b		4.5		V
	Dropout voltage	IL = 10mA	LDOC [2:0]=000b		200		mV
Temperature drift	LDOC [2:0]=000b IL = 10uA	TA=-40°C ~85°C		50		ppm/°C	
VDD Voltage drift	LDOC [2:0]=000b	VDD=2.2V~5.5V		±0.2		%/V	
REFO	REFO operation current, IREFO	VDDA=2.4V, ENV12=1b			50		uA
	output voltage, VREFO		IL = 0mA,		1.2		V
	Temperature drift		TA=-40°C ~85°C		50		ppm/°C
	VDDA Voltage drift				100		uV/V
ACM	ACM operation current, IACM	VDDA=2.4V,	ENACM [0]=1b		50		uA
	Internal Analog Common Mode Voltage ,VACM=VDDA/2	ENADC[0]=1b,	IL = 0uA		VDDA/2		V
	Temperature drift	ENADC[0]=1b,	TA=-40°C ~85°C , ENACM [0]=1b		50		PPM/°C

VDDA : Adjust Voltage Regulator,

REFO : Analog common mode voltage,,

ACM : Internal Analog Common Mode Voltage VDDA/2 (No voltage output)

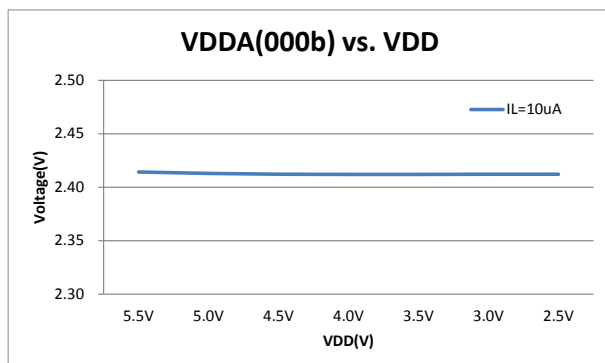


Figure6.6- 1 VDDA(000b) vs. VDD

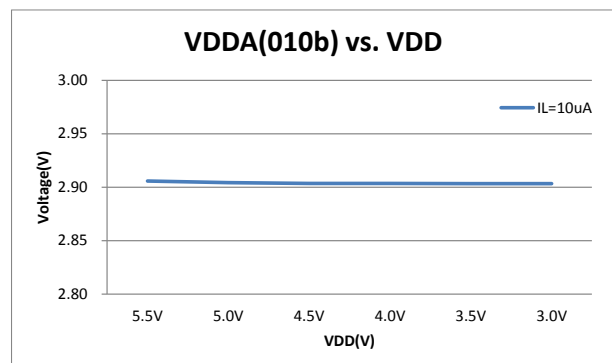


Figure6.6- 2 VDDA(010b) vs. VDD

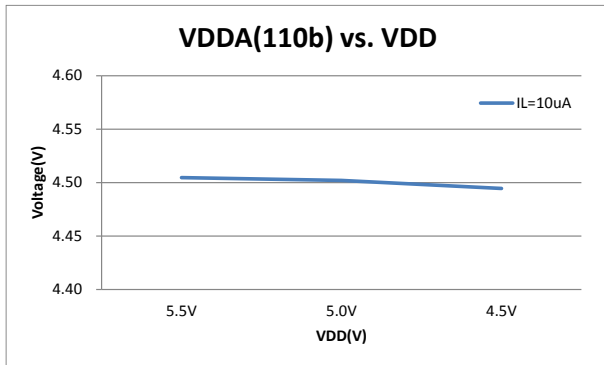


Figure6.6- 3 VDDA(110b) vs. VDD

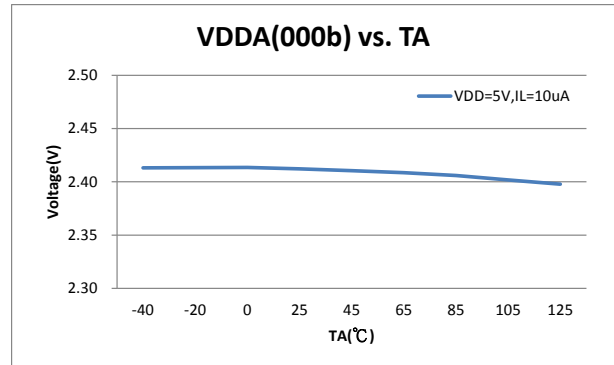


Figure6.6- 4 VDDA(000b) vs. Temperature

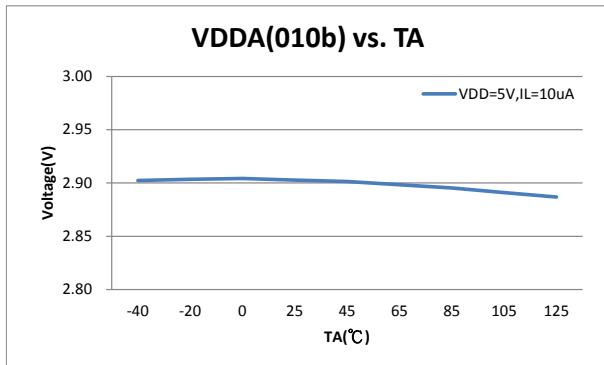


Figure6.6- 5 VDDA(010b) vs. Temperature

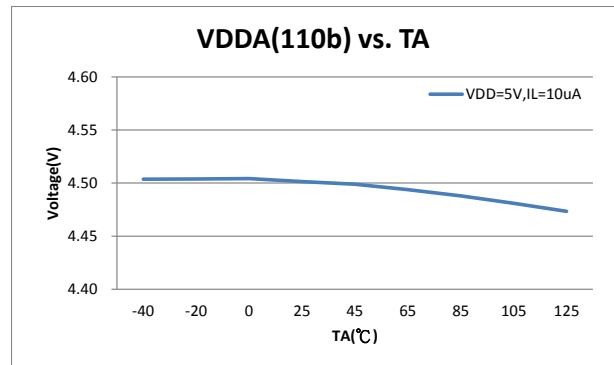


Figure6.6- 6 VDDA(110b) vs. Temperature

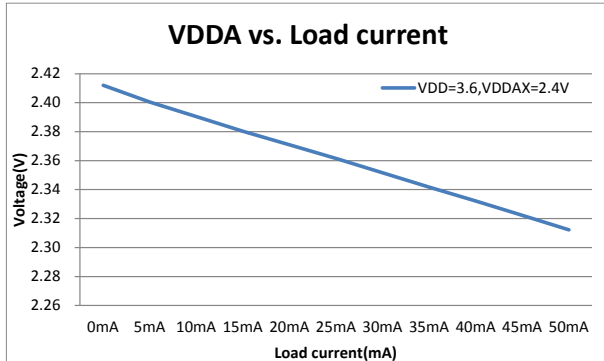


Figure6.6- 7 VDDA vs. Load current



## 6.7. LCD

$T_A = 25^\circ\text{C}, V_{DD} = 3.3\text{V}, C_{VLCD} = 4.7\mu\text{F}$ , unless otherwise noted							
Sym.	Parameter	Test Conditions	Min.	Typ.	Max.	Unit	
$I_{LCD}$	Operation supply current with output buffer.(all segment turn on, No load)	ENLCP[0]=1 $V_{DD} = 3.0\text{V}$		8		uA	
VLCD	Supply Voltage at VLCD pin	ENLCP [0]=0	2.4		5	V	
	Embedded Charge Pump output voltage at VLCD pin	$V_{DD} = 3.3\text{V}$ , ENLCP [0]=1, $C_{VLCD} = 4.7\mu\text{F}$	LCDV[2:0]=111b	-10%	2.45	+10%	V
			LCDV[2:0]=110b	-10%	2.70	+10%	
			LCDV[2:0]=101b	-10%	2.85	+10%	
			LCDV[2:0]=100b	-10%	3.10	+10%	
			LCDV[2:0]=011b	-10%	3.30	+10%	
			LCDV[2:0]=010b	-10%	4.10	+10%	
			LCDV[2:0]=001b ( $V_{DD} > 2.4\text{V}$ mode)	-10%	4.55	+10%	
LCDV[2:0]=000b ( $V_{DD} > 2.75\text{V}$ )	-10%	5.1	+10%				
	VDD Voltage drift	ENLCP [0]=1, $C_{VLCD} = 4.7\mu\text{F}$ , LCDV[2:0]>010b, $V_{DD} = 2.2\text{V} \sim 5.5\text{V}$ ; LCDV[2:0]=001b, $V_{DD} > 2.4\text{V}$ ; LCDV[2:0]=000b, $V_{DD} > 2.75\text{V}$ ;		4		%/V	
$Z_{LCD}$	Output impedance with LCD buffer	$f_{LCD} = 128\text{Hz}$ , VLCD=3.05V		10		kΩ	

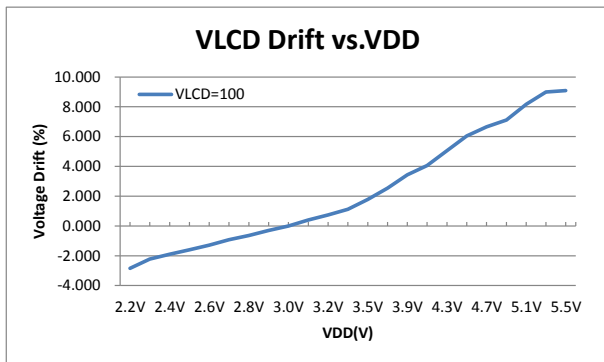


Figure 6.7-1 VLCD(LCDV=100b) vs. VDD

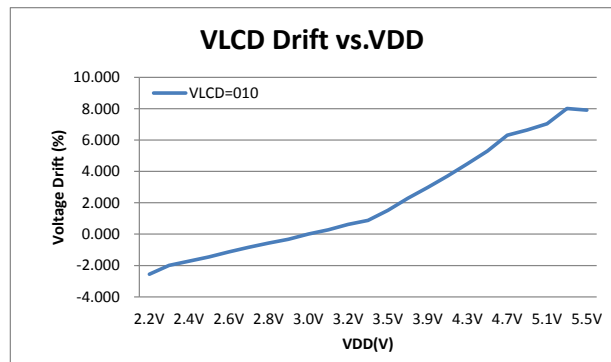


Figure 6.7-2 VLCD(LCDV=010b) vs. VDD

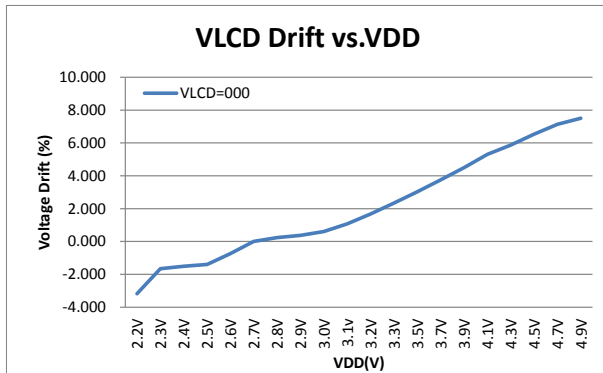


Figure 6.7-3 VLCD(LCDV=000b) vs. VDD

## 6.8. Rail to Rail OPAMP

$T_A = 25^\circ\text{C}$ ,  $V_{DD3V} = 3.0\text{V}$ ,  $V_{DDA}=2.4\text{V}$ , unless otherwise noted

Sym.	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
VDDA	Power supply		2.4		4.5	V
V <sub>OUT</sub>	Output range		0		VDDA	V
V <sub>IN</sub>	Input common range		0		VDDA	V
I <sub>OPA</sub>	OPAMP current			120		uA
I <sub>OPA_LOAD</sub>	Output current loading (push or pull)	VDDA = 3.0V, 0.3V < Output voltage < VDDA-0.3V			1	mA
		VDDA = 2.4V, 0.3V < Output voltage < VDDA-0.3V			0.5	mA
C <sub>LOAD</sub>	Max output capacitor load				1	nF
SR	Slew rate	Loading R=10K, C=100pF, 0.3V → VDDA-0.3V		0.6		V/uS
UGB	Unit gain bandwidth	Loading C=100pF		1000		KHz
V <sub>OS</sub>	Offset error	V <sub>in</sub> = 1.2V	-5		+5	mV
DFD	Digital filter delay	VDDA = 3.0V		2		uS
C <sub>SA</sub>	Sample capacitor			10		pF

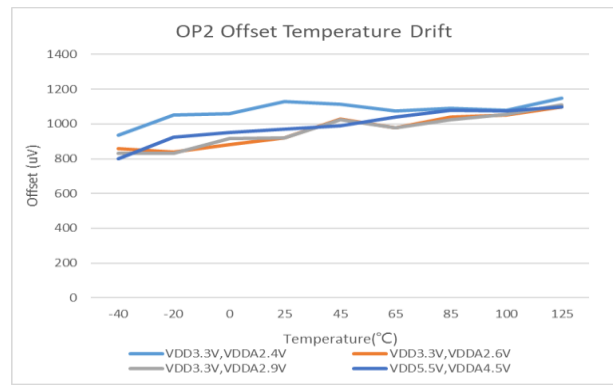
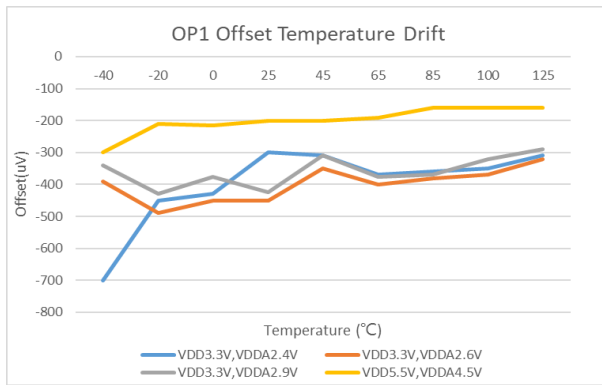


Figure 6.8-1 Offset Temperature

## 6.9. SD18, Power Supply and recommended operating conditions

$T_A = 25^\circ\text{C}$ ,  $V_{DD} = 3.0\text{V}$ ,  $V_{DDA} = 2.4\text{V}$ , unless otherwise noted

Sym.	Parameter	Test Conditions		Min.	Typ.	Max.	Unit
$V_{SD18}$	Supply Voltage at VDDA	ENVDDA[0]=0		2.4		4.5	V
$f_{SD18}$	Modulator sample frequency, ADC_CK			125	500		KHz
	Over Sample Ratio, OSR			64		65536	
$I_{SD18}$	Operation supply current without PGA	ENADC[0]=1 INBUF[0]=0, VRBUF[0]=0	GAIN =16, ADC_CK=500K Hz		260		$\mu\text{A}$

### 6.9.1. R-type GA, Power Supply and recommended operating conditions

$T_A = 25^\circ\text{C}$ ,  $V_{DD} = 3.0\text{V}$ ,  $V_{DDA} = 2.4\text{V}$ , unless otherwise noted

Sym.	Parameter	Test Conditions		Min.	Typ.	Max.	Unit
$V_{PGA}$	Supply Voltage at VDDA	ENVDDA[0]=0		2.4		4.5	V
$I_{PGA}$	Operation supply current				400		$\mu\text{A}$
$G_{PGA}$	Gain temperature drift	$T_A = -40^\circ\text{C} \sim 85^\circ\text{C}$	GAIN=8*16		60		ppm/ $^\circ\text{C}$
	Input RMS Noise	ADC CLK=500KHz, OSR=65536, ADC VR=1.2V w/ chopper mode	GAIN=32*16		40		nV

### 6.9.2. SD18, performance

$T_A = 25^\circ\text{C}$ ,  $V_{DD} = 3.0\text{V}$ ,  $V_{DDA} = 2.4\text{V}$ ,  $V_{VR} = 1.0\text{V}$ , GAIN=1 without PGA,  $f_{SD18} = 500\text{KHz}$ , unless otherwise noted

Sym.	Parameter	Test Conditions		Min.	Typ.	Max.	Unit
INL	Integral Nonlinearity(INL)	$V_{DDA} = 2.4\text{V}$ , $V_{VR} = 1.0\text{V}$ , $\Delta\text{SI} = \pm 200\text{mV}$			$\pm 0.003$	$\pm 0.01$	%FSR
		$V_{DDA} = 2.4\text{V}$ , $V_{VR} = 1.0\text{V}$ , $\Delta\text{SI} = \pm 450\text{mV}$					
	No Missing Codes <sup>3</sup>	ADC_CK=5000KHz, OSR[3:0]=0000b		23			Bits
$G_{SD18}$	Temperature drift Gain x16	$T_A = -40^\circ\text{C} \sim 85^\circ\text{C}$			10		ppm/ $^\circ\text{C}$
$E_{OS}$	Offset error of Full Scale Rang input voltage range without PGA	$\Delta\text{AI} = 0\text{V}$ $\Delta\text{VR} = 1.2\text{V}$ DCSET[3:0]=<0000> * $\Delta\text{AI}$ is external short $T_A = -40^\circ\text{C} \sim 85^\circ\text{C}$	Gain=2			1	%FSR
	Offset error temperature drift without PGA		GAIN=1		2.2		$\mu\text{V}/^\circ\text{C}$
			GAIN=2		1		
			GAIN=4		0.58		
			GAIN=16		0.4		
Offset temperature drift	GAIN=128		0.2		$\mu\text{V}/^\circ\text{C}$		
$\text{CM}_{SD18}$	Common-mode rejection	$V_{\text{CM}} = 0.7\text{V}$ to $1.7\text{V}$ , $V_{\text{VR}} = 1.0\text{V}$ , without PGA	$V_{\text{SI}} = 0\text{V}$ , GAIN=1		90		dB

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		$V_{CM}=0.7V$ to $1.7V$ , $V_{VR}=1.0V$ , without PGA	$V_{SI}=0V$ , GAIN=16		75		
PSRR	DC power supply rejection	$V_{DDA}=3.0V, \Delta V_{DDA}=\pm 100mV$ , $V_{VR}=1.0V, V_{SI}=1.2V, V_{SIL}=1.2V$ ,	GAIN=1 PGA=off		75		dB
			GAIN=16 PGA=8				

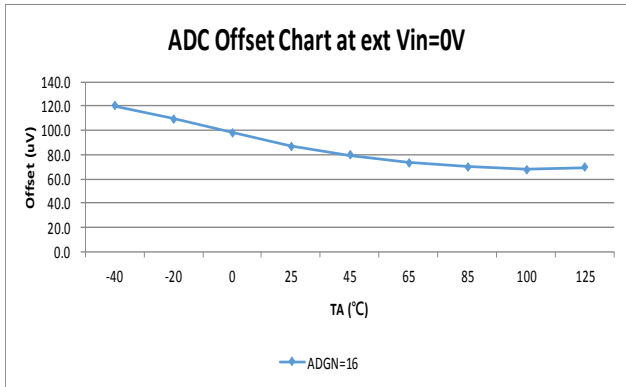


Figure 6.9-1 ADC Offset drift with Temperature

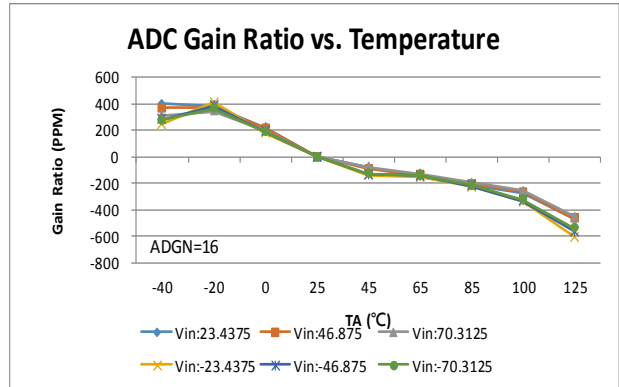


Figure 6.9-2 ADC Gain drift with Temperature

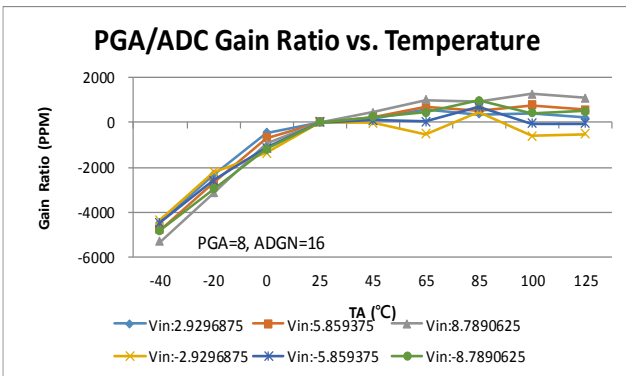


Figure 6.9-3 PGA and ADC Gain drift with Temperature

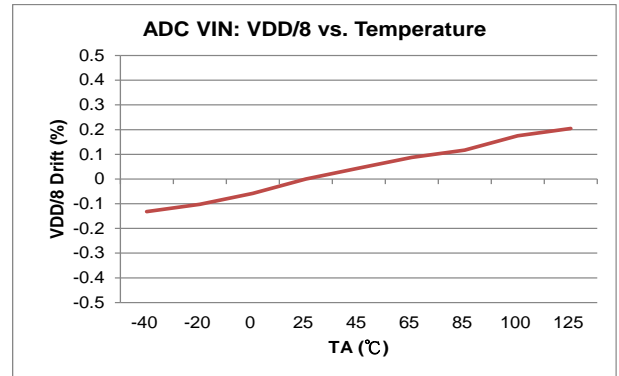


Figure 6.9-4 VDD/8 drift with Temperature

## 6.9.3. SD18 Noise Performance

TA = 25°C, VDD = 3.0V, VDDA=2.4V, unless otherwise noted

HY17P58 針對 SD18 提供了重要的輸入雜訊規格。下表列出典型的雜訊規格表與 Gain, Output rate, 及單端最大輸入電壓等關係。測試條件設定在外部輸入訊號短路，參考電壓為 1.2V，取樣 1024 筆資料。

ENOB(RMS) with OSR/GAIN at A/D Clock=1MHz, VDD=3.3V, VDDA=2.4V, VREF=SDR/2=1.2V, LNOP Chopper On(Mode11_1/16ADCLK), ADC Chopper Off													
Max. Vin(mV)	OSR												
=0.9VREF <sup>(1)</sup>	Gain	Output rate(Hz)	64	128	256	512	1024	2048	4096	8196	16384	32768	65536
±2160	0.25	= off x 0.25	15625	7813	3906	1953	977	488	244	122	61	31	15
±2160	0.5	= off x 0.5	14.8	14.77	15.31	15.68	16.39	16.8	17.17	17.73	18.21	18.64	19.08
±1080	1	= off x 1	14.85	14.8	15.23	15.79	16.28	16.78	17.09	17.56	18.27	18.74	19.19
±540	2	= off x 2	14.74	14.84	15.3	15.72	16.21	16.76	17.09	17.59	18.14	18.67	19.09
±270	4	= off x 4	14.68	14.71	15.22	15.78	16.14	16.81	17.11	17.53	18.06	18.64	19.06
±135	8	= off x 8	14.74	14.69	15.25	15.65	16.01	16.49	16.86	17.4	17.99	18.58	18.98
±68	16	= off x 16	14.62	14.59	15.17	15.55	15.96	16.4	16.7	17.16	17.89	18.48	18.9
±17	64	= 4 x 16	14.46	14.44	15.05	15.02	15.69	16.02	16.17	16.7	17.78	18.35	18.77
±8.5	128	= 8 x 16	13.54	13.65	14.15	14.67	15.12	15.62	16.01	16.52	17.18	17.48	17.85
±4.25	256	= 16 x 16	13.31	13.28	13.87	14.39	14.83	15.3	15.61	16.2	16.71	17.07	17.42
±2.125	512	= 32 x 16	12.91	12.85	13.41	13.84	14.35	14.74	15.09	15.72	16.04	16.55	16.7
			12.12	12.15	12.64	13.18	13.54	14.06	14.35	14.82	15.26	15.81	15.78

(1) Max. Vin(mV) is the max. input voltage single end to ground(VSS)

ENOB(RMS) with OSR/GAIN at A/D Clock=1MHz, VDD=3.3V, VDDA=2.4V, VREF=SDR/2=1.2V, LNOP Chopper On(Mode11_1/16ADCLK), ADC Chopper On							
Max. Vin(mV)	OSR		4096	8192	16384	32768	65536
=0.9VREF <sup>(1)</sup>	Gain	Output rate(Hz)	122	61	31	15	8
±2160	0.25	= off x 0.25	17.62	18.12	18.6	19.18	19.69
±2160	0.5	= off x 0.5	17.63	18.17	18.72	19.17	19.6
±1080	1	= off x 1	17.66	18.04	18.66	19.19	19.58
±540	2	= off x 2	17.55	17.99	18.56	19.12	19.64
±270	4	= off x 4	17.44	18.1	18.44	19.03	19.54
±135	8	= off x 8	17.01	17.74	18.43	19.04	19.4
±68	16	= off x 16	16.34	17.08	18.31	18.88	19.43
±17	64	= 4 x 16	16.49	16.86	17.36	17.94	18.79
±8.5	128	= 8 x 16	16.02	16.71	17.14	17.75	18.14
±4.25	256	= 16 x 16	15.62	16.21	16.7	17.23	17.55
±2.125	512	= 32 x 16	14.7	15.52	16.03	16.44	16.7

(1) Max. Vin(mV) is the max. input voltage single end to ground(VSS)

Table 6.9-1 SD18 ENOB Table

RMS( $\mu$ V) with OSR/GAIN at A/D Clock=1MHz, VDD=3.3V, VDDA=2.4V, VREF=SDR/2=1.2V, LNOP Chopper On(Mode11_1/16ADCLK), ADC Chopper Off													
Max. Vin(mV)	OSR												
	Gain	Output rate(Hz)	64	128	256	512	1024	2048	4096	8196	16384	32768	65536
±2160	0.25	= off x 0.25	336.44	344.32	236.33	183.34	111.99	84.10	65.09	44.19	31.71	23.53	17.34
±2160	0.5	= off x 0.5	162.90	167.71	125.28	84.45	60.42	42.64	34.35	24.88	15.22	10.93	8.04
±1080	1	= off x 1	87.46	81.60	59.56	44.36	31.74	21.55	17.26	12.18	8.32	5.73	4.30
±540	2	= off x 2	45.71	44.91	31.41	21.27	16.59	10.44	8.49	6.33	4.41	2.95	2.19
±270	4	= off x 4	21.86	22.64	15.42	11.67	9.10	6.51	5.05	3.46	2.30	1.53	1.16
±135	8	= off x 8	11.88	12.14	8.16	6.24	4.69	3.46	2.82	2.05	1.24	0.82	0.61
±68	16	= off x 16	6.64	6.75	4.42	4.53	2.84	2.26	2.04	1.41	0.67	0.45	0.33
±17	64	= 4 x 16	3.14	2.93	2.07	1.44	1.05	0.74	0.57	0.40	0.25	0.21	0.16
±8.5	128	= 8 x 16	1.85	1.88	1.26	0.87	0.64	0.46	0.37	0.25	0.17	0.14	0.11
±4.25	256	= 16 x 16	1.22	1.27	0.86	0.64	0.45	0.34	0.27	0.17	0.14	0.10	0.09
±2.125	512	= 32 x 16	1.05	1.03	0.74	0.50	0.39	0.27	0.22	0.16	0.12	0.08	0.08

(1) Max. Vin(mV) is the max. input voltage single end to ground(VSS)

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*RMS( $\mu$ V) with OSR/GAIN at A/D Clock=1MHz, VDD=3.3V, VDDA=2.4V, VREF=SDR/2=1.2V, IA  
LNOP Chopper On(Mode11\_1/16ADCLK), ADC Chopper On*

Max. Vin(mV)	OSR	4096	8192	16384	32768	65536
$\pm 0.9V_{REF}^{(1)}$	Gain = $\frac{V_{REF}}{V_{IN}}$ x ADGN	122	61	31	15	8
$\pm 2160$	<b>0.25</b> = off x <b>0.25</b>	47.73	33.81	24.19	16.15	11.35
$\pm 2160$	<b>0.5</b> = off x <b>0.5</b>	23.73	16.29	11.14	8.12	6.03
$\pm 1080$	<b>1</b> = off x <b>1</b>	11.57	8.91	5.79	4.01	3.06
$\pm 540$	<b>2</b> = off x <b>2</b>	6.24	4.60	3.10	2.10	1.46
$\pm 270$	<b>4</b> = off x <b>4</b>	3.38	2.13	1.69	1.12	0.79
$\pm 135$	<b>8</b> = off x <b>8</b>	2.27	1.37	0.85	0.56	0.43
$\pm 68$	<b>16</b> = off x <b>16</b>	1.81	1.08	0.46	0.31	0.21
$\pm 17$	<b>64</b> = <b>4</b> x <b>16</b>	0.41	0.32	0.22	0.15	0.08
$\pm 8.5$	<b>128</b> = <b>8</b> x <b>16</b>	0.28	0.18	0.13	0.09	0.06
$\pm 4.25$	<b>256</b> = <b>16</b> x <b>16</b>	0.19	0.12	0.09	0.06	0.05
$\pm 2.125$	<b>512</b> = <b>32</b> x <b>16</b>	0.18	0.10	0.07	0.05	0.04

(1) Max. Vin(mV) is the max. input voltage single end to ground(VSS)

Table 6.9-2 SD18 RMS Noise Table

The RMS Noise are referred to the input. The Effective Number of Bits (ENOB(RMS Bit)) is defined as:

$$ENOB(RMS) = \frac{\ln\left(\frac{FSR}{RMS\ Noise}\right)}{\ln(2)}$$

$$RMS\ Noise = \frac{\left(2 \times V_{REF} \times \sqrt{\sum_{k=1}^{1024} (ADO[k] - Average)^2}\right)}{2^{23}}$$

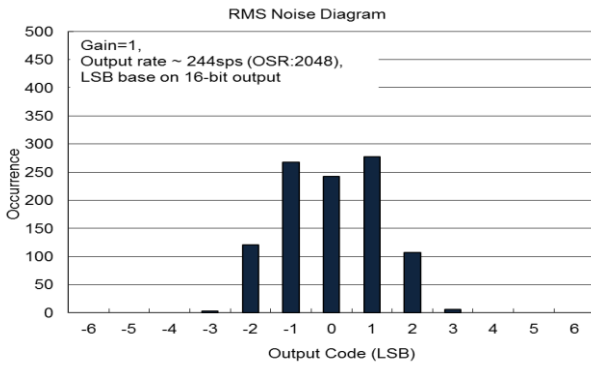


Figure 6.9-1 RMS Noise Diagram

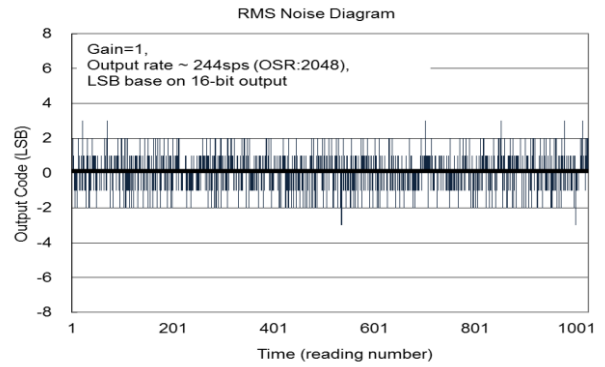


Figure 6.9-2 Output Code Diagram

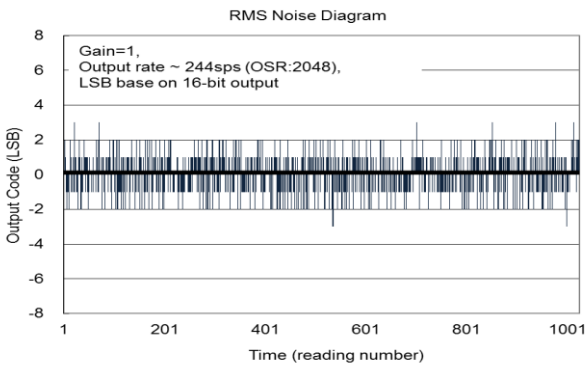


Figure 6.9-3 RMS Noise Diagram

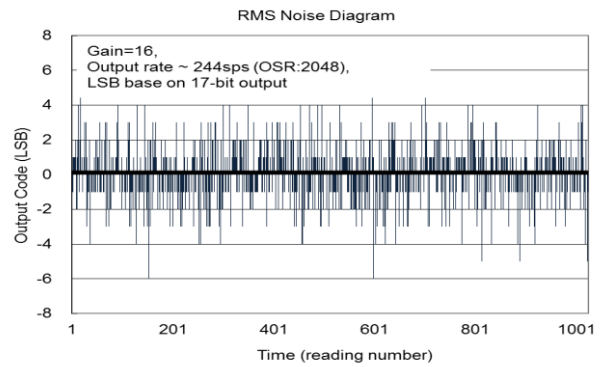


Figure 6.9-4 Output Code Diagram

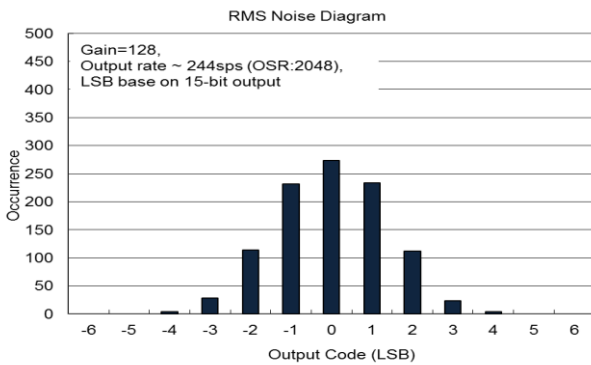


Figure 6.9-5 RMS Noise Diagram

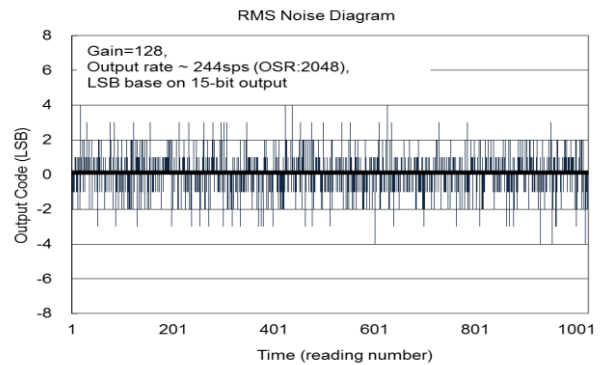


Figure 6.9-6 Output Code Diagram



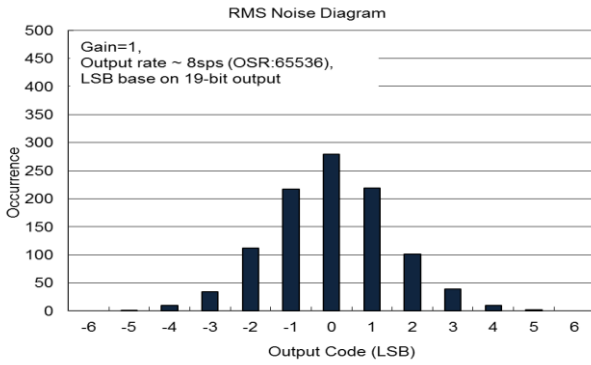


Figure 6.9-7 RMS Noise Diagram

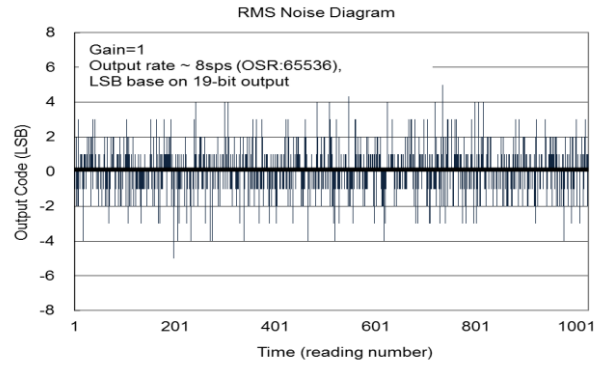


Figure 6.9-8 Output Code Diagram

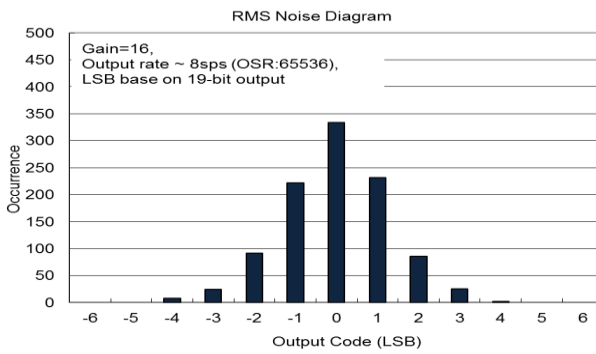


Figure 6.9-9 RMS Noise Diagram

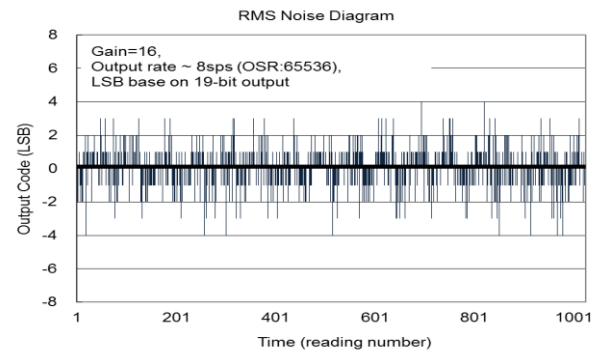


Figure 6.9-10 Output Code Diagram

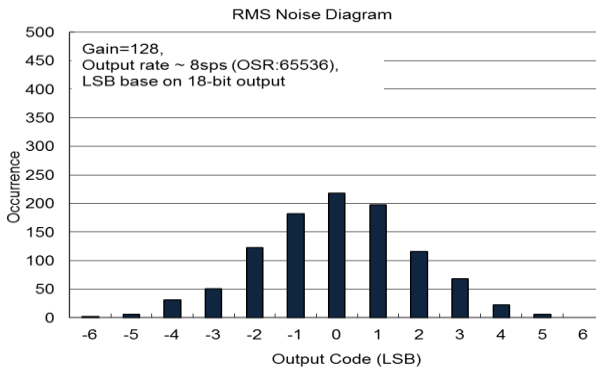


Figure 6.9-11 RMS Noise Diagram

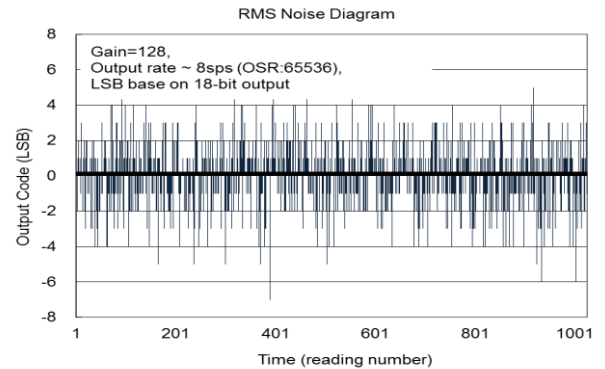


Figure 6.9-12 Output Code Diagram

## 6.9.4. SD18 ,Temperature Sensor

$T_A = 25^{\circ}\text{C}$ ,  $V_{DD} = 3.0\text{V}$ ,  $V_{DDA} = 2.4\text{V}$ , unless otherwise noted

Sym.	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$TC_S$	Sensor temperature drift			173		$\mu\text{V}/^{\circ}\text{C}$
KT	Absolute Temperature Scale $0^{\circ}\text{K}$			-284		$^{\circ}\text{C}$
$TC_{ERR}$	One point calibrate error temperature	Calibration at $25^{\circ}\text{C}$ of $-40^{\circ}\text{C} \sim 85^{\circ}\text{C}$		$\pm 1$		$^{\circ}\text{C}$

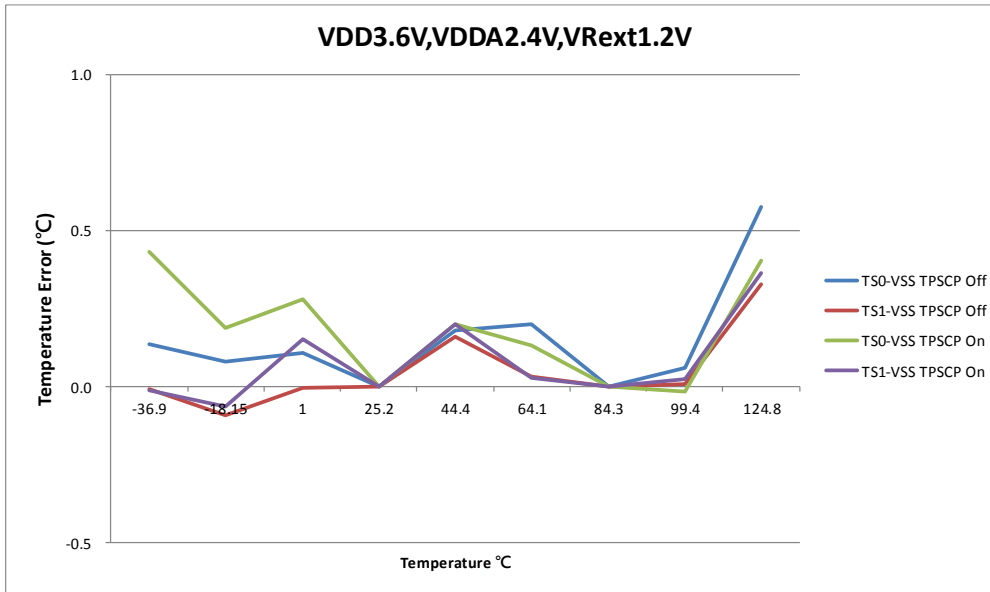


Figure 6.9-13 ADC Temperature Error

## 6.10. Build-In EPROM(BIE)

TA = 25°C, VDD = 3.0V, unless otherwise noted

Sym.	Parameter	Test Conditions	Min.	Typ.	Max.	unit
V <sub>BIE</sub>	Supply Voltage at VPP PIN			8.5	8.75	V
I <sub>BIE</sub>	Operation supply current			3		mA
V <sub>SS</sub>	Supply Voltage			0		V

When connecting to the external VBIE power source to program the BIE block, users can use the instruction to program the words one by one into the BIE block.

## 6.11. Build-In EPROM(BIE) Low voltage control circuit

TA = 25°C, VDD = 3.05V, unless otherwise noted

Sym.	Parameter	Test Conditions	Min.	Typ.	Max.	unit
T <sub>O</sub>	Operation temperature range		0	25	40	°C
V <sub>DD</sub>	Operation supply Voltage		2.75		5.5	V
V <sub>SS</sub>	Supply Voltage			0		V

When the 2.75V low voltage programming control circuit is activated, users can program the BIE block without connecting to the external VBIE power source.

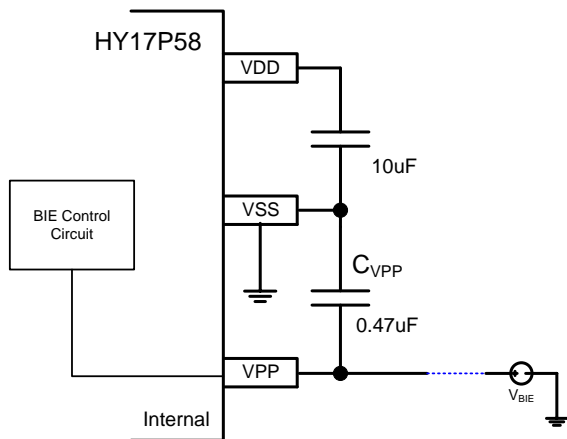


Figure 6.11-1 BIE typical application circuit

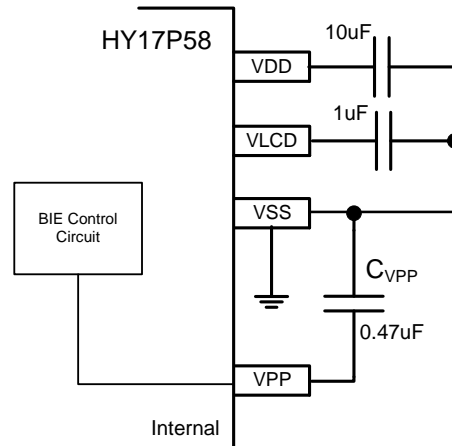


Figure 6.11-2 Use low voltage control circuit

## 6.12. LED Backlight driver

$T_A = 25^\circ\text{C}, V_{DD} = 2.4\text{V} \sim \text{BLOUT}+0.2\text{V}, \text{ENLEDP}[0]=1\text{b}, -40^\circ\text{C} < T_A < 85^\circ\text{C}$ , unless otherwise noted

Sym.	Parameter	Test Conditions	Min.	Typ.	Max.	Unit	
$V_{IN}$	$V_{DD}$ Supply Voltage		2.4		$V_{BL} + 0.2$	V	
$V_{GG}$	Pump voltage	$V_{DD}=2.2\text{V}$		4		V	
$V_{BL}$	backlight voltage(BLOUT)	$V_{DD}=2.2\text{V},$ $V_{GG}=4\text{V}, C_{HL}=1\mu\text{F},$ $I_{LED} \leq 15\text{mA}$ $T_A=25^\circ\text{C}$	LEDS[2:0]=000b		2.0		V
			LEDS[2:0]=001b		2.2		
			LEDS[2:0]=010b		2.4		
			LEDS[2:0]=011b		3.0		
			LEDS[2:0]=100b		3.2		
			LEDS[2:0]=101b		3.4		
			LEDS[2:0]=110b		3.6		
			LEDS[2:0]=111b		3.8		
$I_{LED}$	drive current				15	mA	

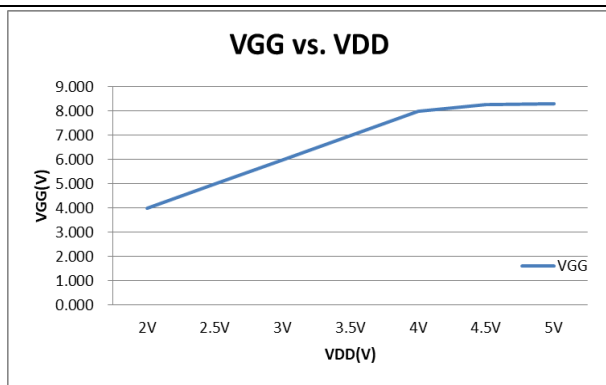


Figure 6.12-1 VGG vs. VDD

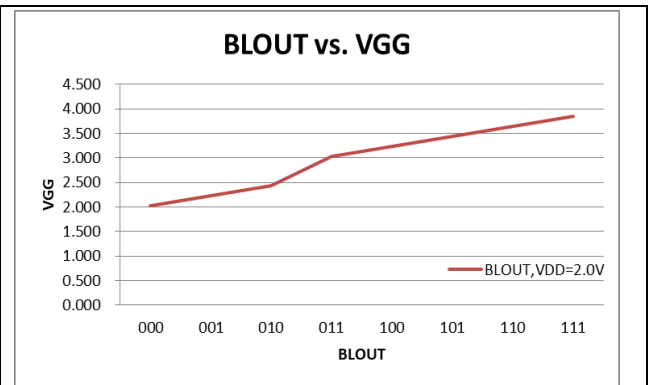


Figure 6.12-2 BLOUT vs. VGG

## 7. 訂貨資訊

下單品名 1	封裝型式	引腳數	封裝型式		程式碼	出貨包裝 形式	個裝 數量	材料 組成	MSL3
			描述方式		編號 2				
HY17P58-D000	Die	-	D	000	000	-		Green4	-
HY17P58-L100	LQFP	100	L	100	000	Tray	90	Green4	MSL-3

### <sup>1</sup> 產品名稱 – 封裝型式描述方式 – 程式碼編號 (空白片 / 標準品 / 代客燒錄碼)

例如：您的 HY17P58 代客燒錄服務申請的程式碼編號為 008，且需要的產品是裸片出貨。則下單品名為 HY17P58-D000-008

例如：您的需求是 HY17P58 不帶程式碼的空白片且需要的產品是裸片出貨。則下單品名為 HY17P58-D000

例如：您的需求是 HY17P58 不帶程式碼的空白片且需要的產品是封裝片 LQFP100 出貨，則下單品名為 HY17P58-L100，且需以 Tray 出貨，則除下單品名外，請特別註明出貨包裝形式為 Tray

例如：您的 HY17P58 代客燒錄服務申請的程式碼編號為 009，而需求的產品是封裝片 LQFP100 出貨，則下單品名為 HY17P58-L100-009，且需以 Tray 出貨，則除下單品名外，請特別註明出貨包裝形式為 Tray

### <sup>2</sup> 程式碼編號

“001”~“999” 為標準品或代客燒錄申請的程式碼編號，而空白晶片不帶此碼。

### <sup>3</sup> MSL:

濕度敏感性等級係依據 IPC/JEDEC J-STD-020 的規範加以試驗分級，並參考 IPC/JEDEC J-STD-033 的標準處理、包裝、運輸與使用。

### <sup>4</sup> Green (RoHS & no Cl/Br):

HYCON 產品皆為 Green Product，符合 RoHS 指令，REACH 高關注物質(SVHC)以及無鹵素規定 (Br<900ppm or Cl<900ppm or (Br+Cl)<1500ppm)。

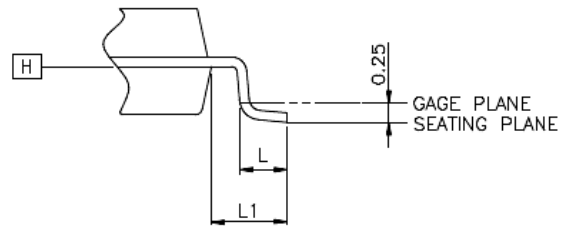
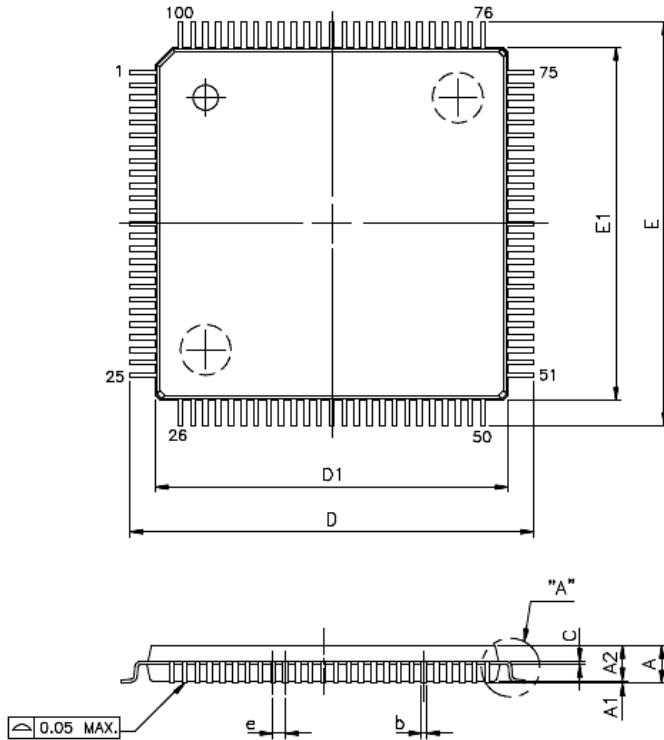
# HY17P58

Embedded 18-Bit  $\Sigma\Delta$ ADC  
8-Bit RISC-like Mixed Signal Microcontroller

## 8. 封裝型式資訊

### 8.1. LQFP100(14x14)

#### 8.1.1. Package Dimensions



VARIATIONS (ALL DIMENSIONS SHOWN IN MM)

SYMBOLS	MIN.	NOM.	MAX.
A	--	--	1.60
A1	0.05	--	0.15
A2	1.35	1.40	1.45
b	0.17	0.20	0.27
c	0.09	0.127	0.20
D	16.00 BSC		
D1	14.00 BSC		
E	16.00 BSC		
E1	14.00 BSC		
e	0.50 BSC		
L	0.45	0.60	0.75
L1	1.00 REF		

Note: JEDEC MS-026 compliant

## 9. 修訂記錄

以下描述本文件差異較大的地方，而標點符號與字形的改變不在此描述範圍。

文件版次	頁次	日期	摘要
V01	All	2018/10/22	初版發行
V02	31~32	2019/03/15	修改 OPA 網路架構
V03	31	2019/10/29	新增 DAC 網路方塊圖
	41	2020/1/7	新增外振 32768 功耗
V04	39	2020/4/30	修正 HAO 規格
	43		修正 I/O 規格
	45		修正 BOR2 規格
V05	30	2020/6/2	修正 SPI 暫存器名稱
	28、38		修正 LCD 暫存器名稱
	47	2020/7/15	增加 VDDA 上下限規格
V06	36	2021/1/4	修改暫存器列表，增加 INIS1、VRIN、INIS
	45~46		修正 BOR2 規格 增加 BOR、Reset 時序圖
	31~33		修改 DAC、OPA 網路架構說明
	28、37	2021/4/20	增加 LCDTYPE 控制 Bit
	47		修改 REFO 電氣規格
	26、27	2021/4/28	修正圖 4-16、圖 4-17、圖 4-18
V07	21	2021/9/11	修改 Reset 架構圖