



HY17P51

Datasheet

8-Bit RISC-like Mixed Signal Microcontroller
Embedded 4x14 LCD Driver
Embedded High Resolution $\Sigma\Delta$ ADC

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- 8、本規格書中內容，未經本公司許可，嚴禁用於其他目的之轉載或複製。

1. 特點

- 8 位元加強型精簡指令集，共有 71 個指令包含硬體乘法指令及查表指令 H08D
- 2.0V to 5.5V 工作電壓範圍，-40°C~85°C 工作溫度範圍。
- 內建高精度 RC 震盪器，多種 CPU 工作時脈切換選擇，可讓使用者達到最佳省電規劃
 - 運行模式
 - 待機模式 1.1uA
 - 休眠模式 0.4uA
- 4KWord OTP Type 程式記憶體，256Byte 資料記憶體
- Brownout detector 及 Watch dog Timer，可防止 CPU 進入死機模式。
- 4x14 LCD 液晶驅動器
 - 1/4 Duty、1/3 Bias
 - 內建 Charge Pump 穩壓線路，可提供多種 LCD 偏壓
 - 2 個 LCD 埠可設定數位輸出埠
- LVD 低電壓檢測功能具 14 段檢測電壓設置與外部輸入電壓檢測功能
- 類比電壓源 VDDA 具 10mA 穩壓電壓源輸出，快速啟動功能，可提供傳感器驅動電壓
- 24-Bit $\Sigma\Delta$ ADC 類比數位轉換器
 - 梳狀濾波器採二階/三階設計，轉換頻率達 7.2Ksps
 - 取樣頻率 921KHz
 - 超取樣頻率設置 64 ~ 65536
 - 全差動輸入信號、測量範圍零點調整
 - 內置 PGA(Programmable Gain Amplifier) 有 1/4 ~ 128 倍輸入信號放大倍率選擇
 - 內置絕對溫度感測器
- 8-bit Timer A1
- 串列通訊 EUART 模組、蜂鳴器輸出功能
- Built-In EPROM (BIE) · 內建 2.75V 低壓燒錄控制電路
- Support 8 stack Level.

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2. 引腳定義

2.1. QFN32 引腳圖

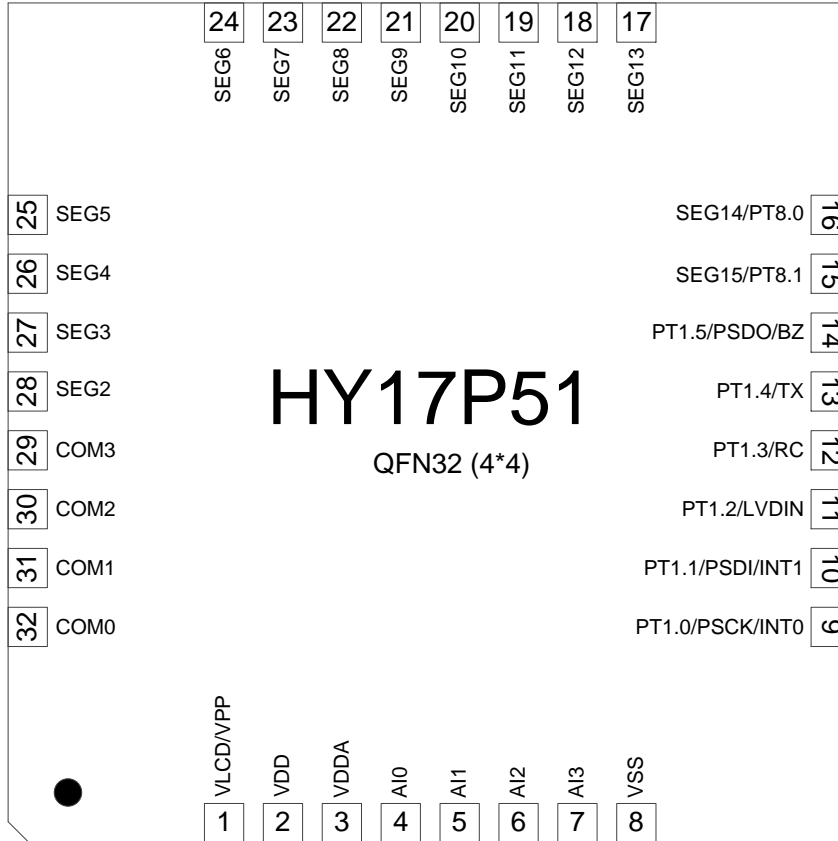


圖 2-1 HY17P51 QFN32 引腳圖

註：VPP 與 VLCD 復用同一接口，非燒錄 OTP 時禁止輸入高電壓

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2.2. QFN16 引腳圖

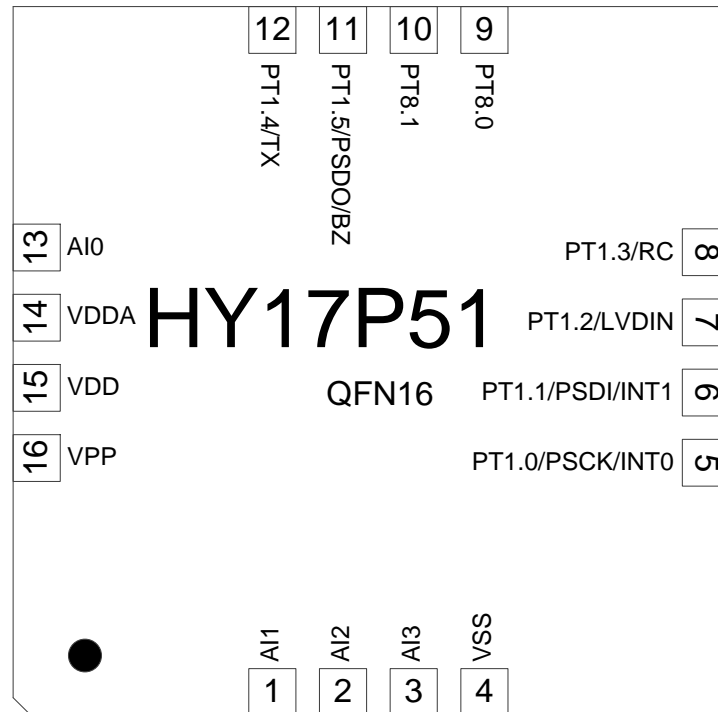


圖 2-2 HY17P51 QFN16 引腳圖

註：VPP 與 VLCD 復用同一接口，非燒錄 OTP 時禁止輸入高電壓

2.3. I/O 定義與說明

“I/O”輸入/輸出,“I”輸入,“O”輸出,“S”史密斯觸發,“C”CMOS 特性兼容輸出與輸入,“P”電壓源,“A”類比通道

引腳編號		引腳名稱	引腳特性		功能說明
QFN32 (4x4)	QFN16 (3x3)		格式	緩衝	
1	16	VLCD/VPP	P	P	LCD 的電壓源 OTP 讀/寫時的電壓源
		VLCD VPP	P	P	
2	15	VDD	P	P	晶片工作電壓源接正端引腳, 需外接 10uF 電容至 VSS.
3	14	VDDA	P	P	LDO 線性穩壓電源輸出引腳·類比電 路電壓源·啟動輸出時需外接 1uF 電 容至 VSS.
4	13	AI0	A	A	類比輸入通道
5	1	AI1	A	A	類比輸入通道
6	2	AI2	A	A	類比輸入通道
7	3	AI3	A	A	類比輸入通道
8	4	VSS	P	P	晶片工作電壓源接地端引腳
9	5	PT1.0/INT1.0/PSCK	I/O	S/C	數位輸入/輸出引腳 中斷源 E0IF OTP 讀/寫介面接口
		PT1.0	I	S	
		INT1.0 PSCK	I	S	
10	6	PT1.1/INT1.1/PSDI	I/O	S/C	數位輸入/輸出引腳 中斷源 E1IF OTP 讀/寫介面接口
		PT1.1	I	S	
		INT1.1 PSDI	I	S	
11	7	PT1.2/LVDIN	I/O	S/C	數位輸入/輸出引腳 LVD 外部信號輸入接口
		PT1.2 LVDIN	A	A	
12	8	PT1.3/RC	I/O	S/C	數位輸入/輸出引腳 EUART 通訊接收信號
		PT1.3 RC	I	S	
13	12	PT1.4/TX	I/O	S/C	數位輸入/輸出引腳 EUART 通訊傳送信號
		PT1.4 TX	O	C	

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引腳編號		引腳名稱	引腳特性		功能說明
QFN32 (4x4)	QFN16 (3x3)		格式	緩衝	
14	11	PT1.5/PSDO/BZ			數位輸入/輸出引腳 OTP 讀/寫介面接口 蜂鳴器輸出端
		PT1.5	I/O	S/C	
		PSDO	O	C	
		BZ	O	C	
15	10	PT8.1/SEG15			數位輸入/輸出引腳 LCD Segment 輸出
		PT8.1	I/O	S/C	
		SEG15	O	A	
16	9	PT8.0/SEG14			數位輸入/輸出引腳 LCD Segment 輸出
		PT8.0	I/O	S/C	
		SEG14	O	A	
17	-	SEG13			LCD Segment 輸出
		SEG13	O	A	
18	-	SEG12			LCD Segment 輸出
		SEG12	O	A	
19	-	SEG11			LCD Segment 輸出
		SEG11	O	A	
20	-	SEG10			LCD Segment 輸出
		SEG10	O	A	
21	-	SEG9			LCD Segment 輸出
		SEG9	O	A	
22	-	SEG8			LCD Segment 輸出
		SEG8	O	A	
23	-	SEG7			LCD Segment 輸出
		SEG7	O	A	
24	-	SEG6			LCD Segment 輸出
		SEG6	O	A	
25	-	SEG5			LCD Segment 輸出
		SEG5	O	A	
26	-	SEG4			LCD Segment 輸出
		SEG4	O	A	
27	-	SEG3			LCD Segment 輸出
		SEG3	O	A	
28	-	SEG2			LCD Segment 輸出
		SEG2	O	A	

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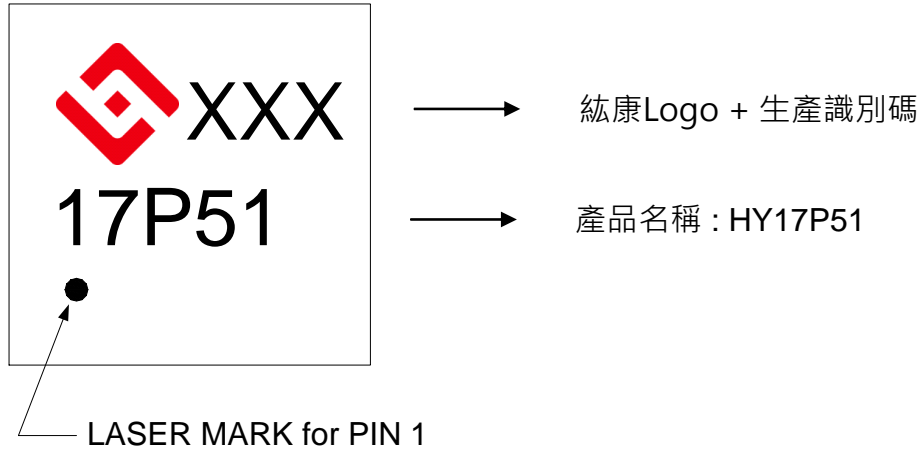
引腳編號		引腳名稱	引腳特性		功能說明
QFN32 (4x4)	QFN16 (3x3)		格式	緩衝	
29	-	COM3 COM3	O	A	LCD COM 輸出
30	-	COM2 COM2	O	A	LCD COM 輸出
31	-	COM1 COM1	O	A	LCD COM 輸出
32	-	COM0 COM0	O	A	LCD COM 輸出

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2.4. 封裝片標記信息

2.4.1. QFN 封裝片標記信息



3. 應用電路

3.1. 橋式感測器 LCD 顯示

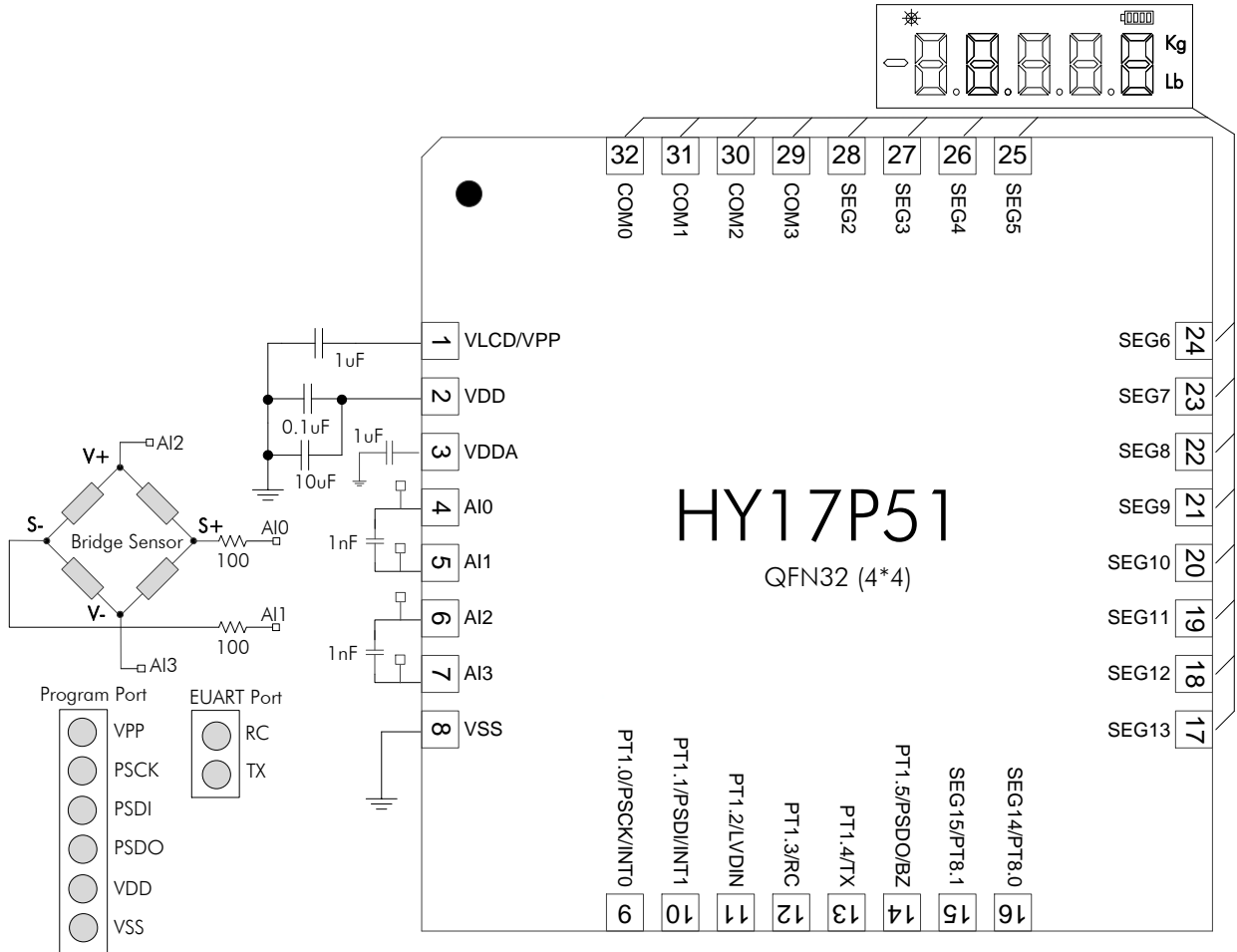


圖 3-1 橋式感測器 LCD 顯示應用電路-增強 RS 抗干擾能力

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3.2. 快速電子體溫計應用

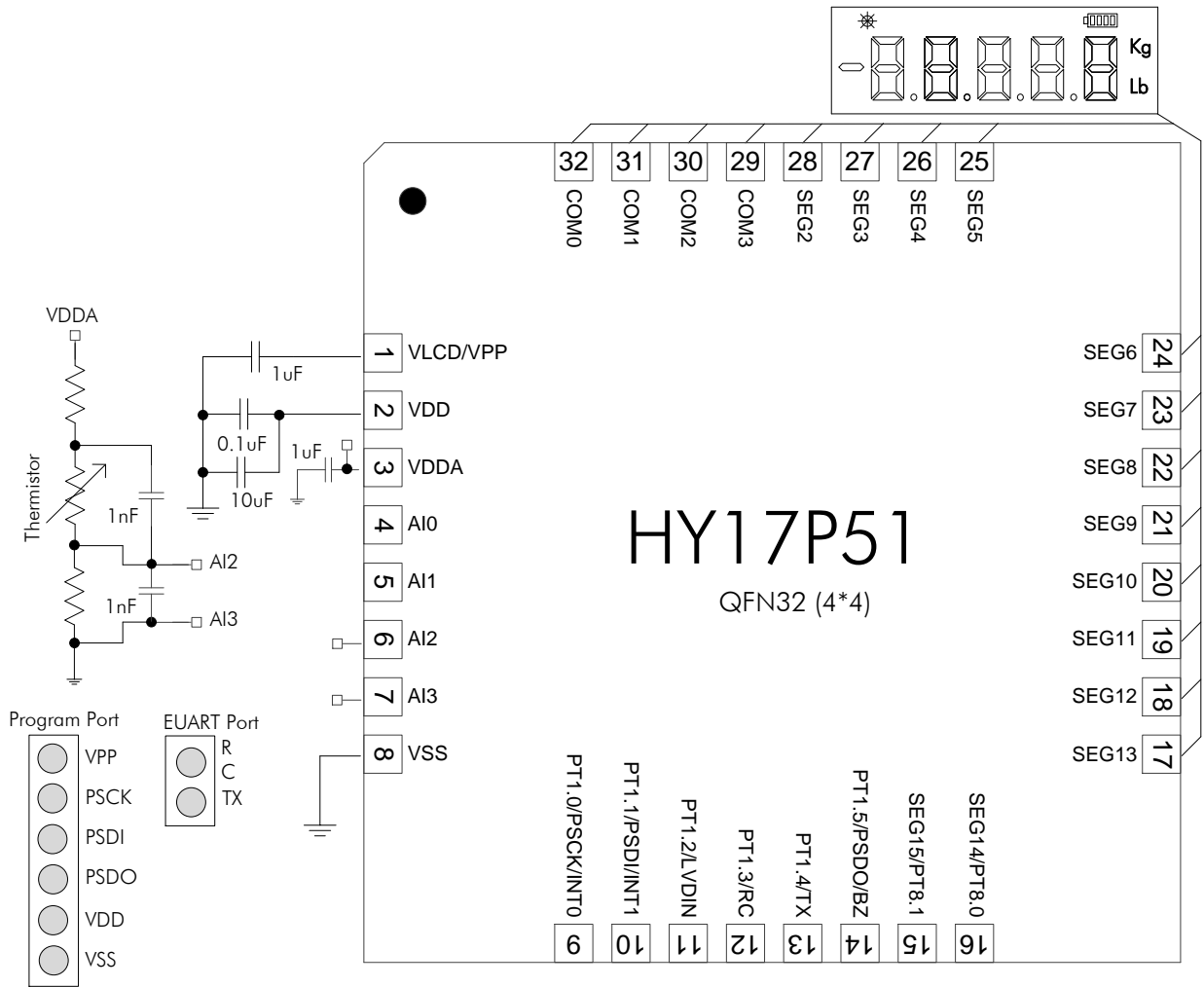


圖 3-2 快速電子體溫計應用應用電路

4. 功能概述

4.1. 內部方塊圖

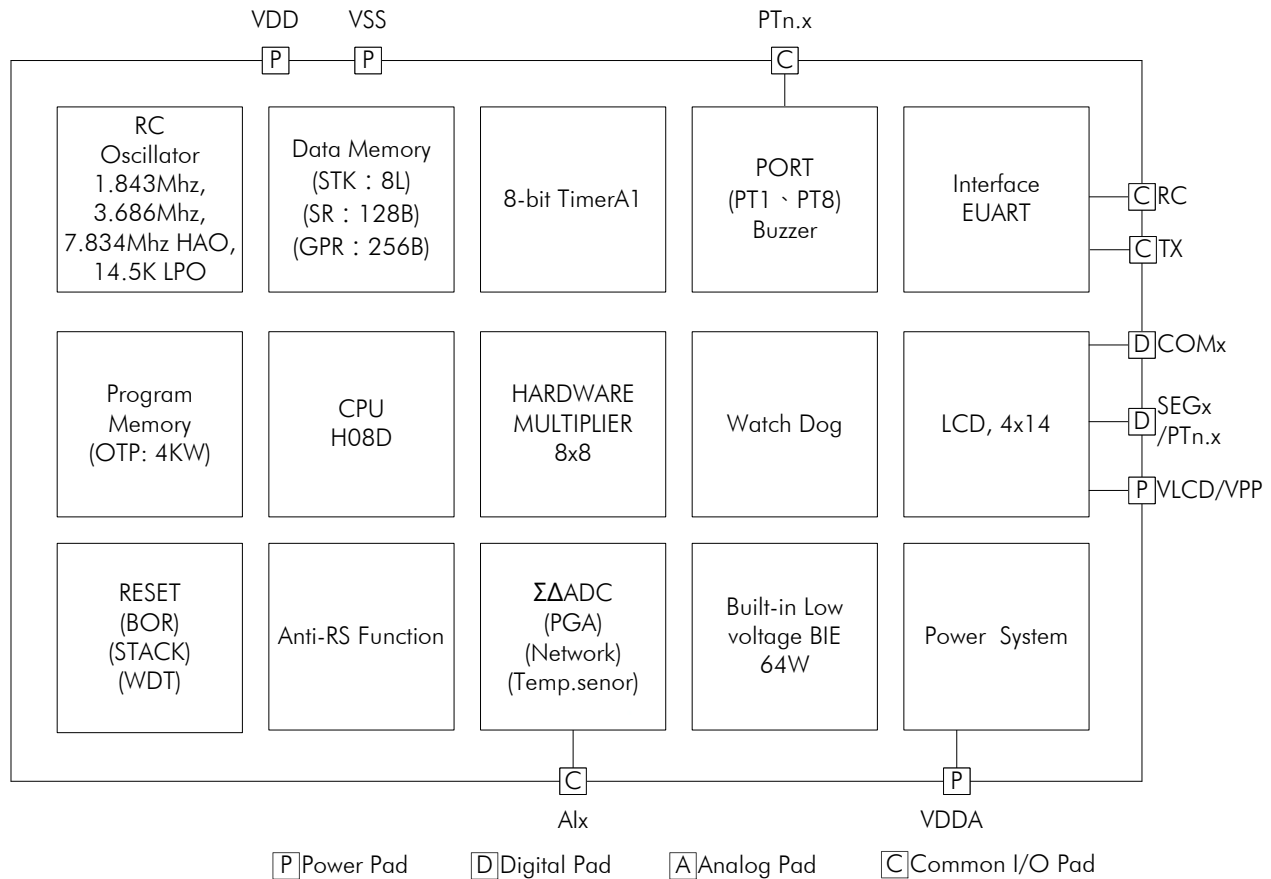


圖 4-1 HY17P51 內部方塊圖

4.2. 相關說明與支援文件

晶片功能相關使用說明書

DS-HY17P51

HY17P51 說明書

UG-HY17S58

HY17S58 使用說明書

APD-CORE002

H08D 指令集說明書

開發工具相關使用說明書

APD-HY17PIDE001

HY17P 系列 Assembly 語言開發工具軟體使用說明書

APD-HYIDE016

H08 系列 C 語言開發工具軟體使用說明書

APD-HY17PIDE002

HY17P 系列開發工具硬體使用說明書

產品生產相關使用說明書

APD-HY17PIDE004

HY17P 系列生產線專用燒錄器說明書

4.3. Clock System

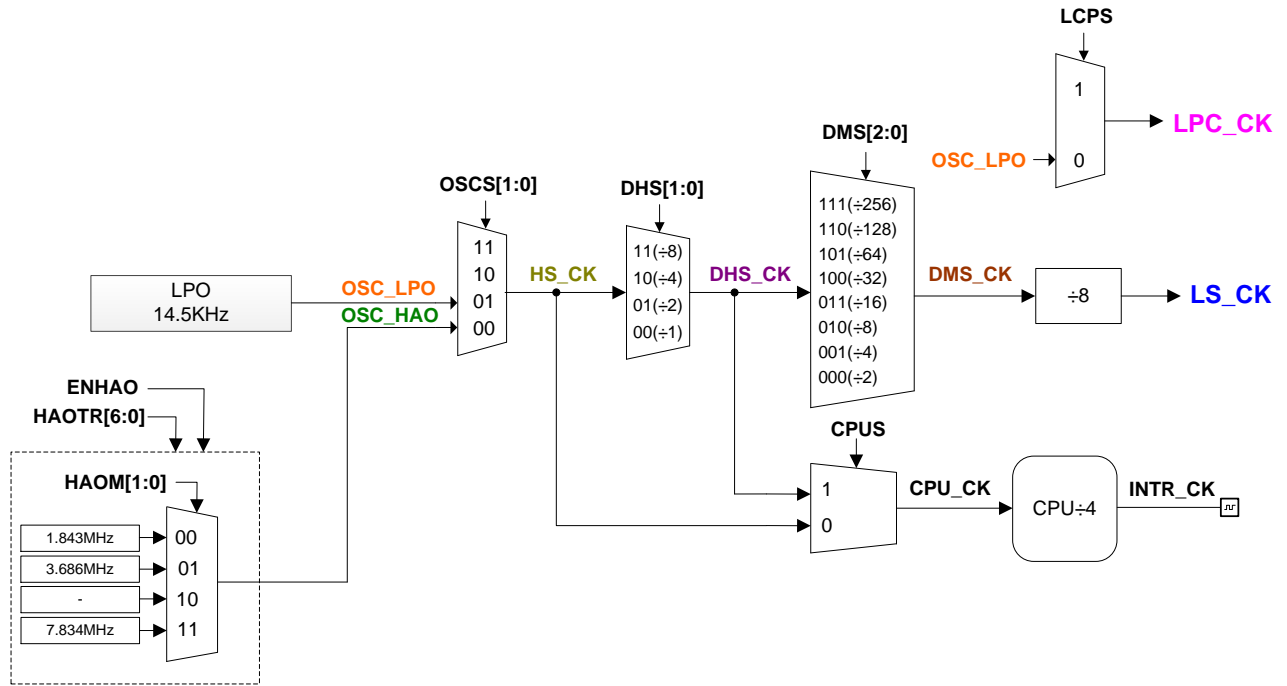


圖 4-2 Clock System 方塊圖(一)

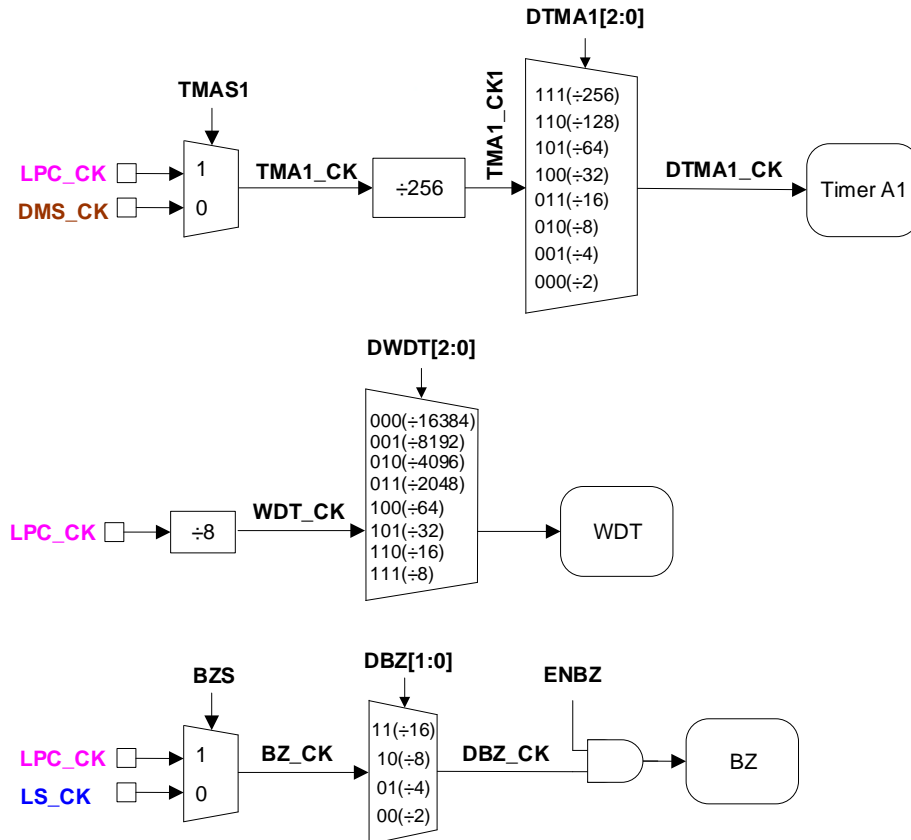


圖 4-3 Clock System 方塊圖(二)

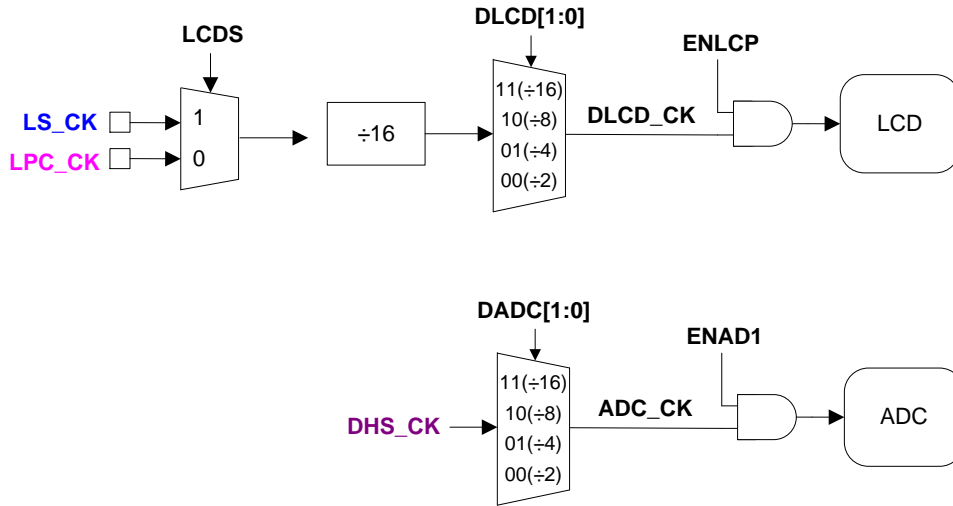


圖 4-4 Clock System 方塊圖(三)

4.4. Low Voltage Detect(LVD)

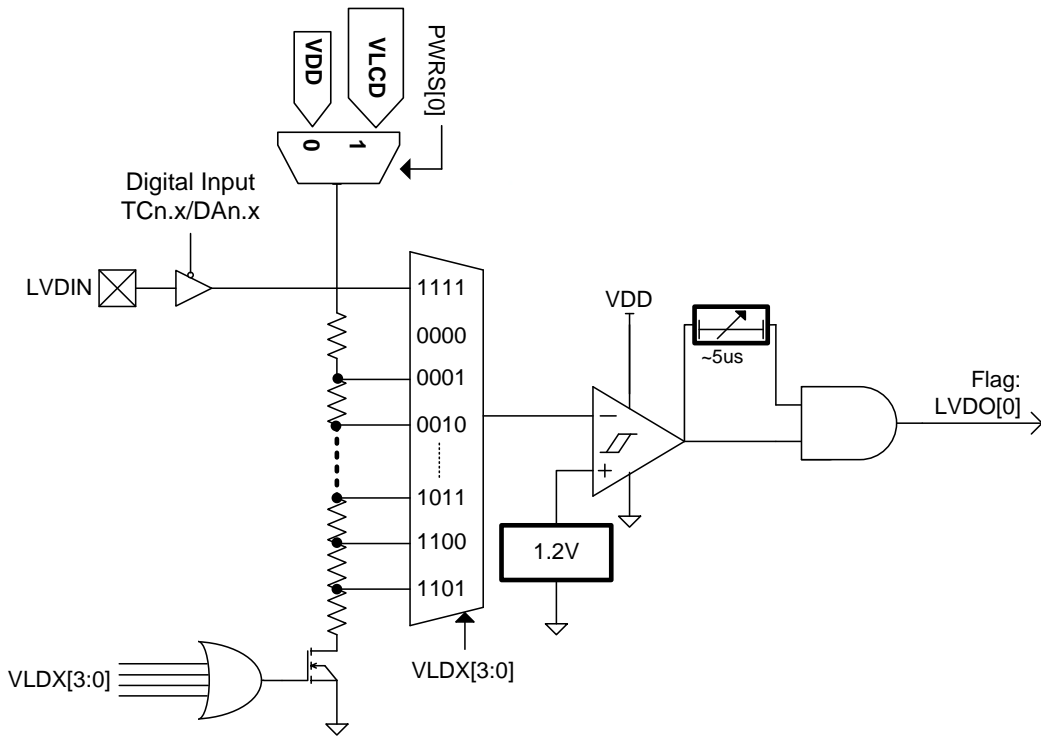


圖 4-5 Low Voltage Detect 方塊圖

4.5. Reset

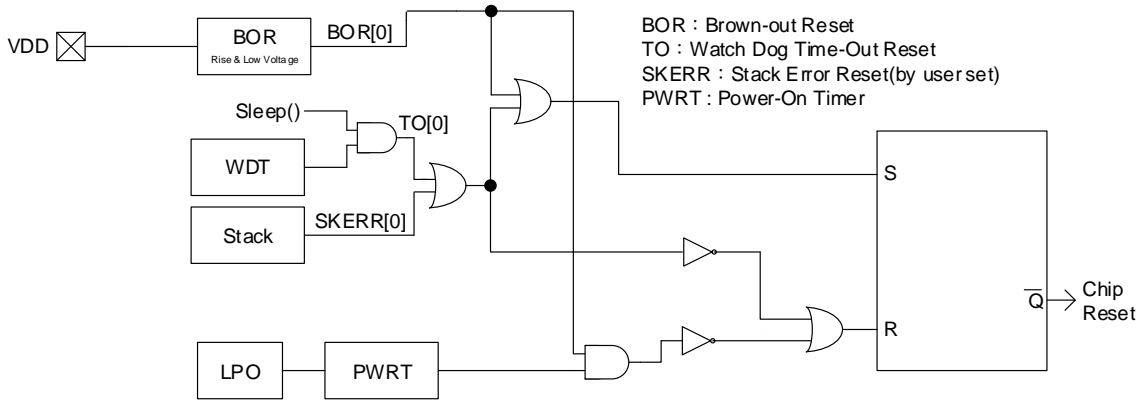


圖 4-6 Reset 方塊圖

4.6. Power System

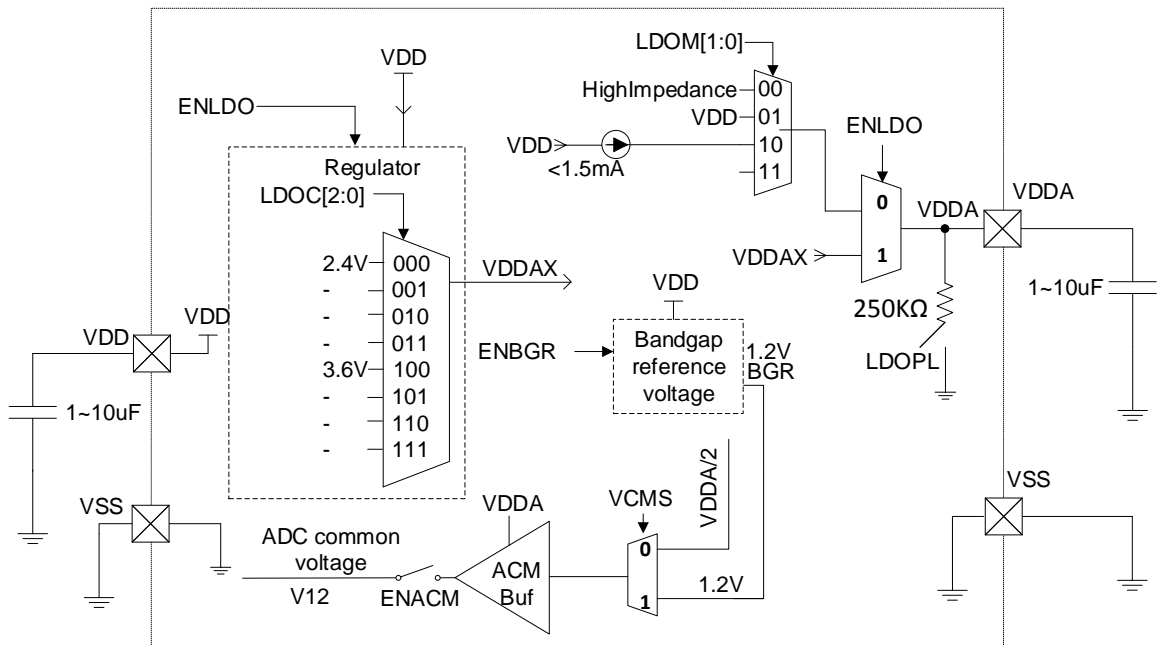


圖 4-7 Power System 方塊圖

4.7. $\Sigma\Delta$ ADC Network

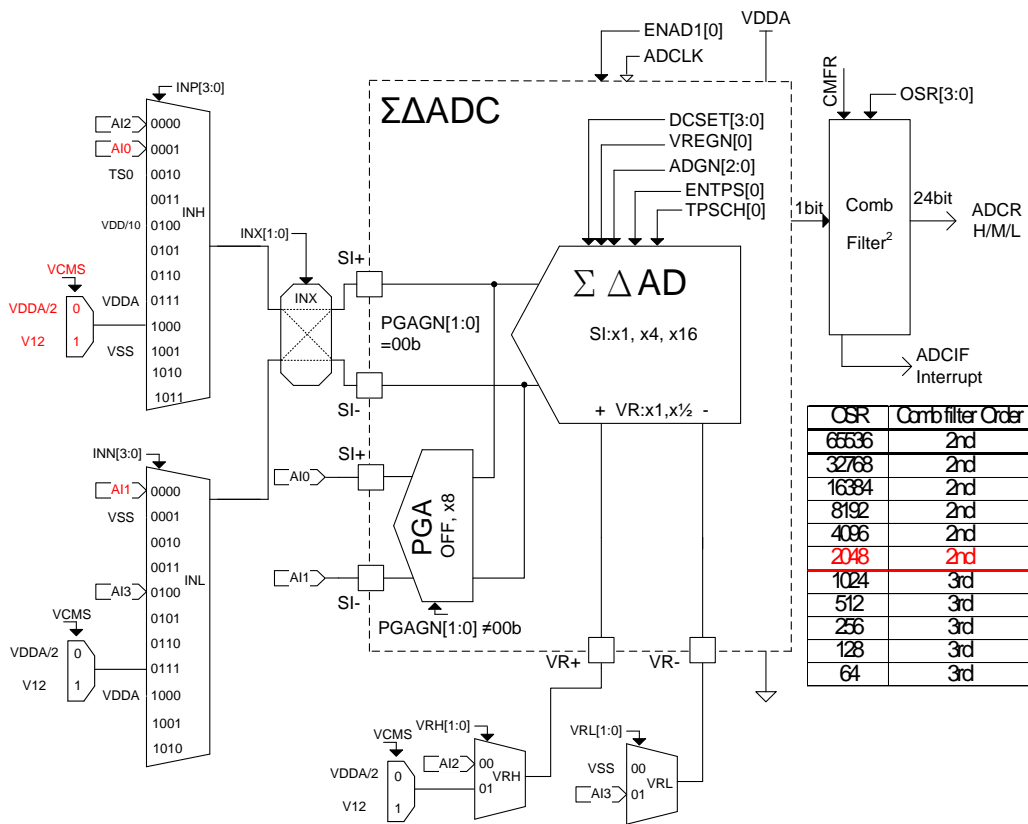


圖 4-8 $\Sigma\Delta$ ADC Network 方塊圖

4.8. GPIO PT1

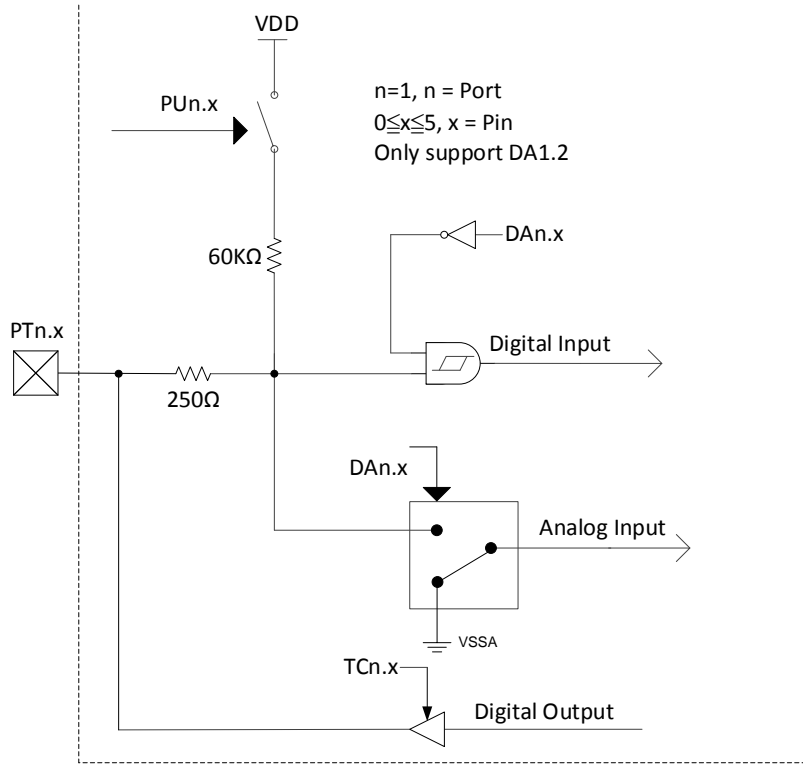


圖 4-9 GPIO PT1 方塊圖

4.9. GPIO PT8/SEG14~SEG15

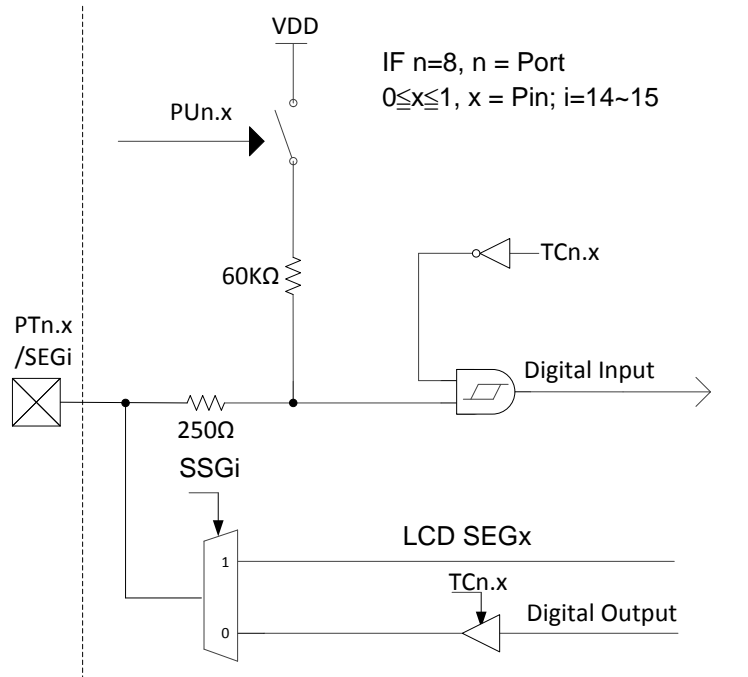


圖 4-10 GPIO PT8/SEG14~SEG15 方塊圖

4.10. Watch Dog

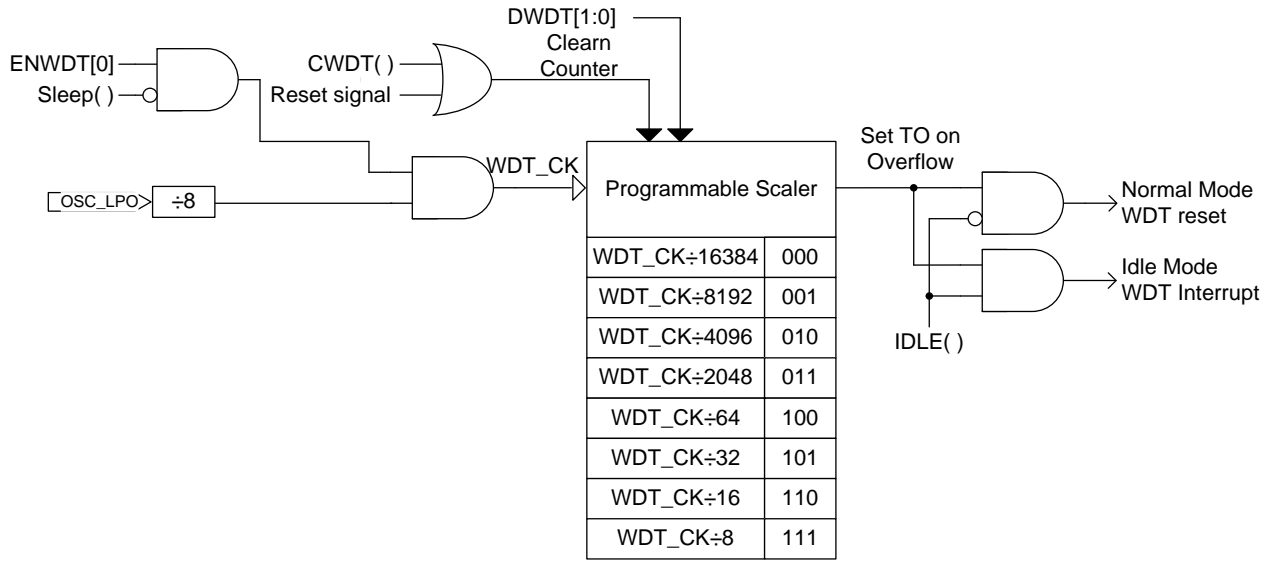


圖 4-11 Watch Dog 方塊圖

4.11. 8-bit Timer A1

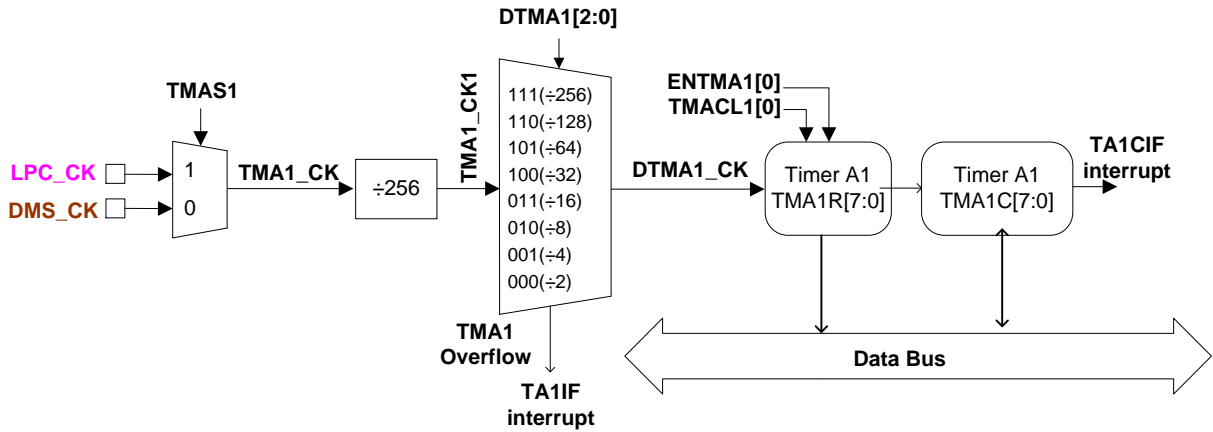


圖 4-12 8-bit Timer A1 方塊圖

4.12. LCD

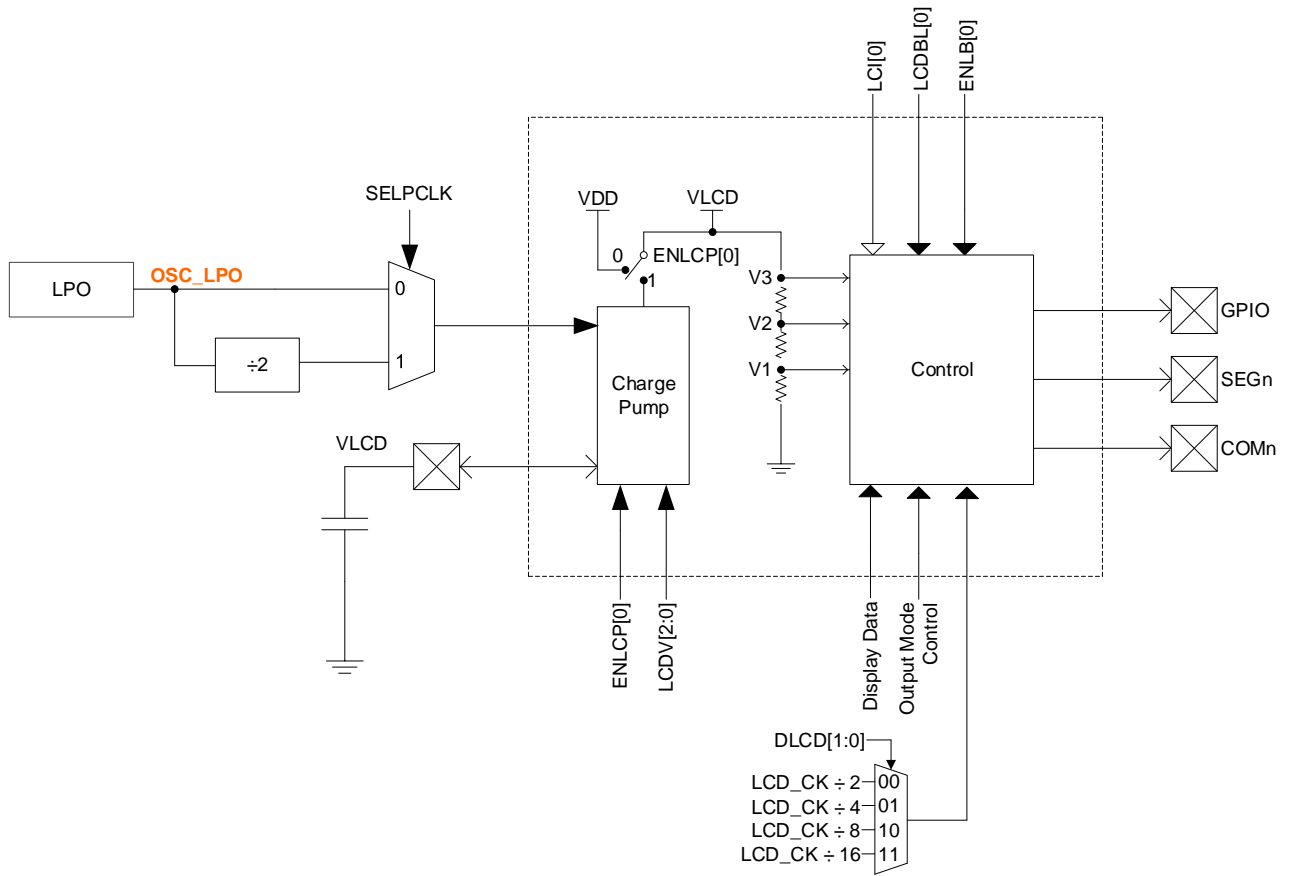


圖 4-13 LCD 方塊圖

4.13. EUART

EUART TRANSMIT BLOCK DIAGRAM

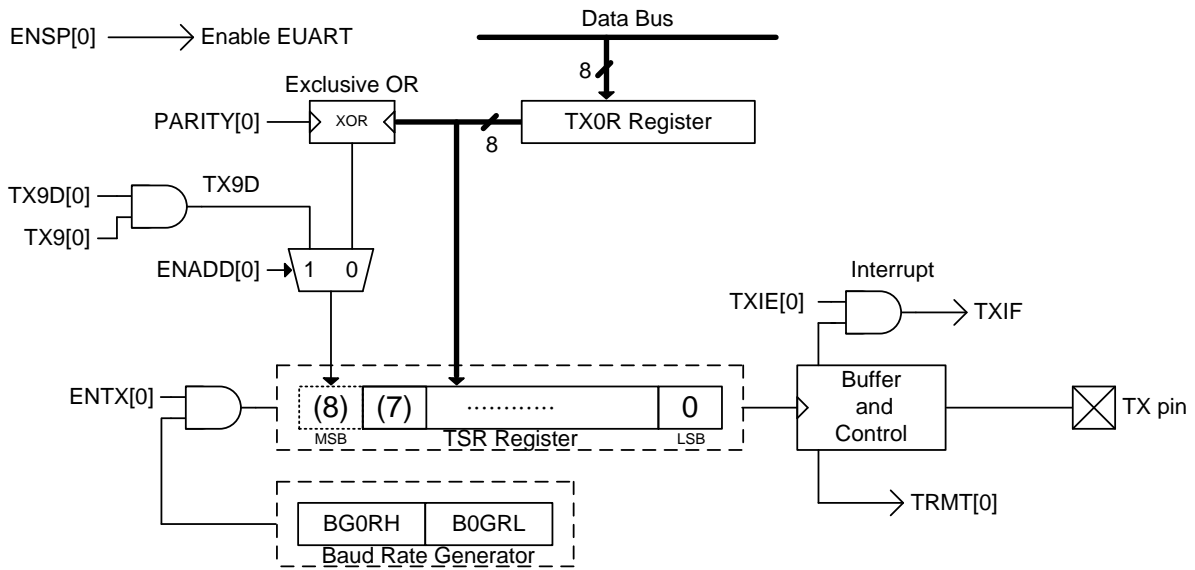
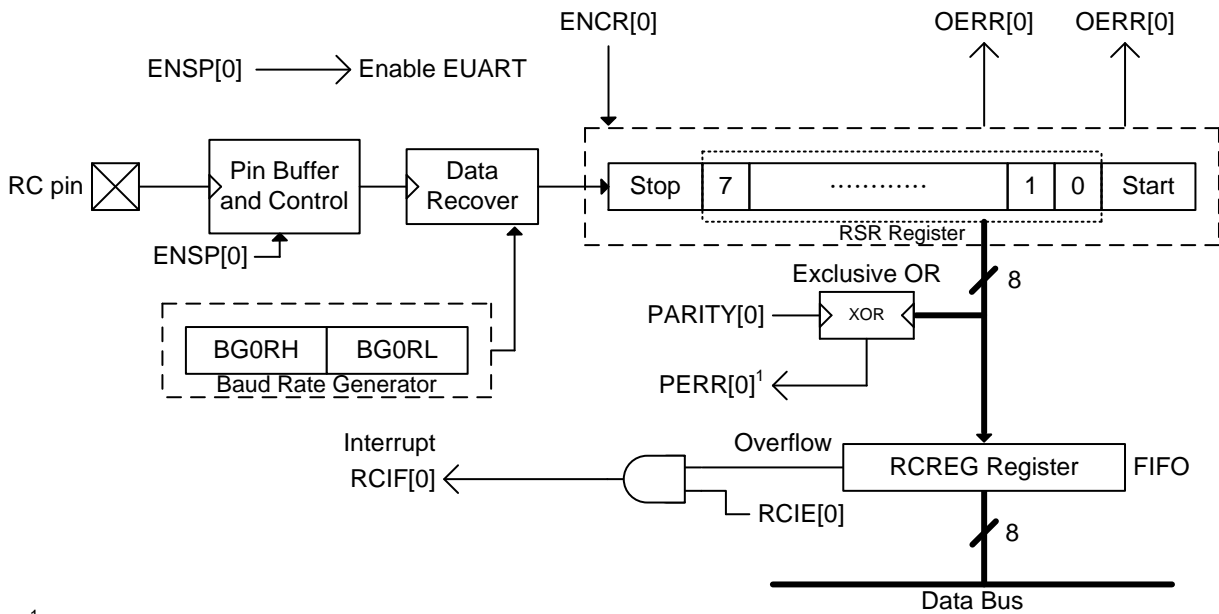


圖 4-14 EUART 傳送方塊圖

EUART 8-BITS RECEIVE BLOCK DIAGRAM



¹Don't care PERR[0] state of 8-bits receive mode

圖 4-15 EUART 8-bits 接收方塊圖

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5. 暫存器列表

“.”no use,“r”read/write,“w”write,“r”read,“r0”only read 0,“r1”only read 1,“w0”only write 0,“w1”only write 1
“\$”for event status,“.”unimplemented bit,“x”unknown,“u”unchanged,“d”depends on condition

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	ARST	IRST	R/W
000h	INDF0	Contents of FSR0 to address data memoryvalue of FSR0 not changed								xxxx xxxx	uuuu uuuu	***** 1 1 1 1 1 1
001h	POINC0	Contents of FSR0 to address data memoryvalue of FSR0 post-incremented								xxxx xxxx	uuuu uuuu	***** 1 1 1 1 1 1
002h	PODEC0	Contents of FSR0 to address data memoryvalue of FSR0 post-decremented								xxxx xxxx	uuuu uuuu	***** 1 1 1 1 1 1
003h	PRINC0	Contents of FSR0 to address data memoryvalue of FSR0 pre-incremented								xxxx xxxx	uuuu uuuu	***** 1 1 1 1 1 1
004h	PLUSW0	Contents of FSR0 to address data memoryvalue of FSR0 offset by W								xxxx xxxx	uuuu uuuu	***** 1 1 1 1 1 1
005h	INDF1	Contents of FSR1 to address data memoryvalue of FSR1 not changed								xxxx xxxx	uuuu uuuu	***** 1 1 1 1 1 1
006h	POINC1	Contents of FSR1 to address data memoryvalue of FSR1 post-incremented								xxxx xxxx	uuuu uuuu	***** 1 1 1 1 1 1
007h	PODEC1	Contents of FSR1 to address data memoryvalue of FSR1 post-decremented								xxxx xxxx	uuuu uuuu	***** 1 1 1 1 1 1
008h	PRINC1	Contents of FSR1 to address data memoryvalue of FSR1 pre-incremented								xxxx xxxx	uuuu uuuu	***** 1 1 1 1 1 1
009h	PLUSW1	Contents of FSR1 to address data memoryvalue of FSR1 offset by W								xxxx xxxx	uuuu uuuu	***** 1 1 1 1 1 1
00Ah	INDF2	Contents of FSR2 to address data memoryvalue of FSR2 not changed								xxxx xxxx	uuuu uuuu	***** 1 1 1 1 1 1
00Bh	POINC2	Contents of FSR2 to address data memoryvalue of FSR2 post-incremented								xxxx xxxx	uuuu uuuu	***** 1 1 1 1 1 1
00Ch	PODEC2	Contents of FSR2 to address data memoryvalue of FSR2 post-decremented								xxxx xxxx	uuuu uuuu	***** 1 1 1 1 1 1
00Dh	PRINC2	Contents of FSR2 to address data memoryvalue of FSR2 pre-incremented								xxxx xxxx	uuuu uuuu	***** 1 1 1 1 1 1
00Eh	PLUSW2	Contents of FSR2 to address data memoryvalue of FSR2 offset by W								xxxx xxxx	uuuu uuuu	***** 1 1 1 1 1 1
00Fh	FSROH	-	-	-	-	-	-	-	FSR0[8]XU	~.~.~.~.~.~.* 1 1 1 1 1 1
010h	FSROL	Indirect Data Memory Address Pointer 0 Low Byte,FSR0[7:0]								xxxx xxxx	uuuu uuuu	***** 1 1 1 1 1 1
011h	FSR1H	-	-	-	-	-	-	-	FSR1[8]XU	~.~.~.~.~.~.* 1 1 1 1 1 1
012h	FSR1L	Indirect Data Memory Address Pointer 0 Low Byte,FSR1[7:0]								xxxx xxxx	uuuu uuuu	***** 1 1 1 1 1 1
016h	TOSH	-	-	-	-	TOS[11:8]		 xxxx uuuu	~.~.~.~.~.~.* 1 1 1 1 1 1	
017h	TOSL	Top-of-Stack Low Byte (TOS<7:0>)								xxxx xxxx	uuuu uuuu	***** 1 1 1 1 1 1
018h	SKCN	SKFL	SKUN	SKOV	-	SKPRT[3:0]			000. 0000	u\$. \$\$\$	rw0,rw0,rw0,~.~.~.* 1 1 1 1 1 1	
01Ah	PCLATH	-	-	-	-	PC[11:8]		 0000 0000	~.~.~.~.~.~.* 1 1 1 1 1 1	
01Bh	PCLATL	PC Low Byte for PC<7:0>								0000 0000	0000 0000	***** 1 1 1 1 1 1
01Dh	TBLPTRH	-	-	-	-	TBLPTR11:8]		 xxxx uuuu	~.~.~.~.~.~.* 1 1 1 1 1 1	
01Eh	TBLPTRL	Program Memory Table Pointer Low Byte (TBLPTR<7:0>)								xxxx xxxx	uuuu uuuu	***** 1 1 1 1 1 1
01Fh	TBLDH	Program Memory Table Latch High Byte								xxxx xxxx	uuuu uuuu	***** 1 1 1 1 1 1
020h	TBLDL	Program Memory Table Latch Low Byte								xxxx xxxx	uuuu uuuu	***** 1 1 1 1 1 1
021h	PRODH	Product Register of Multiply High Byte								xxxx xxxx	uuuu uuuu	***** 1 1 1 1 1 1
022h	PRODL	Product Register of Multiply Low Byte								xxxx xxxx	uuuu uuuu	***** 1 1 1 1 1 1
023h	INTE0	GIE	TA1GIE	ADIE	WDTIE	-	-	E1IE	EOIE	0000 0000	0uuu uuuu	***** 1 1 1 1 1 1
024h	INTE1	TA1IE	-	TXIE	RCIE	-	-	-	-	0000 0000	uuuu uuuu	***** 1 1 1 1 1 1
026h	INTF0	-	TA1CIF	ADIF	WDTIF	-	-	E1IF	E0IF	.000 0000	.uuu uuuu	***** 1 1 1 1 1 1
027h	INTF1	TA1IF	-	TXIF	RCIF	-	-	-	-	0000 0000	uuuu uuuu	***** 1 1 1 1 1 1
029h	WREG	Working Register								xxxx xxxx	uuuu uuuu	***** 1 1 1 1 1 1
02Ah	BSRCN	-	-	-	-	-	-	-	BSR[0]XU	~.~.~.~.~.~.* 1 1 1 1 1 1
02Bh	MSTAT	-	-	-	C	DC	N	OV	Z	...X xxxx	...U uuuu	~.~.~.~.~.~.* 1 1 1 1 1 1
02Ch	PSTAT	BOR	PD	TO	IDL	RST	SKERR	-	-	\$000 \$0..	uu\$u u\$.	rw0,rw0,rw0,rw0,rw0,~.~.* 1 1 1 1 1 1
02Eh	BIECN	1	-	-	ENBVD	VPPHV	ENBCP	BIEWR	BIERD	1.00 \$000	1.00 \$uuu	r1,~.~.* r1,~.~.* 1 1 1 1 1 1
02Fh	BIEARH	-	-	1	1	1	1	1	1	0.xx xxxx	u.uu uuuu	***** 1 1 1 1 1 1
030h	BIEARL	BIE Address Register as BIEAL[5:0]								xxxx xxxx	uuuu uuuu	***** 1 1 1 1 1 1
031h	BIEDRH	BIE High Byte Data Register								xxxx xxxx	uuuu uuuu	***** 1 1 1 1 1 1
032h	BIEDRL	BIE Low Byte Data Register								xxxx xxxx	uuuu uuuu	***** 1 1 1 1 1 1
033h	PWRCN	ENBGR	LDOC[2:0]		LDOM[1:0]		ENLDO	CSFON		1000 0000	uuuu uu0u	***** 1 1 1 1 1 1
034h	OSCCN0	-	OSCS[0]	DHS[1:0]		DMS[2:0]		CUPS		0000 0000	uuuu uuuu	***** 1 1 1 1 1 1
035h	OSCCN1	CCOPT	-	DADC[1:0]		-	-	-	LCDS	0000 0000	uuuu uuuu	***** 1 1 1 1 1 1
036h	OSCCN2	DLCD[1:0]		-	-	-	HAOM[1:0]		ENHAO	0000 0011	uuuu uu11	***** 1 1 1 1 1 1
037h	CSFCN0	SKRST	HAOTR[6:0]								.1..	~.~.~.~.~.~.* 1 1 1 1 1 1
038h	CSFCN1	ENSDRV	-	-	-	-	-	-	-	uuuu uuuu	***** 1 1 1 1 1 1
039h	WDTCN	ENBZ	BZS	BZ[1:0]		ENWDT	DWDWT[2:0]			0000 0000	uuuu \$000	~.~.~.* rw1,~.~.* 1 1 1 1 1 1
03Ah	AD1H	ADC1 conversion high byte data register								..00 0000	..uu uuuu	~.~.~.~.~.~.* 1 1 1 1 1 1
03Bh	AD1M	ADC1 conversion middle byte data register								0000 0000	uuuu uuuu	***** 1 1 1 1 1 1
03Ch	AD1L	ADC1 conversion low byte data register								0000 0000	uuuu uuuu	***** 1 1 1 1 1 1

表 5-1 資料記憶體列表

HY17P51

Embedded High Resolution ΣΔADC 8-Bit RISC-like Mixed Signal Microcontroller



“-”no use,“*”read/write,“w”write,“r”read,“r0”only read 0,“r1”only read 1,“w0”only write 0,“w1”only write 1
“\$”for event status,“u”unimplemented bit,“x”unknown,“u”unchanged,“d”depends on condition

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	ARST	IRST	R/W	
03Dh	AD1CN0	ENAD1	-	OSR[3:0]			CMFR	0000 0000	uuuu uuuu	***** 1 1 1 1 1 1 1			
03Eh	AD1CN1	INIS1	-	VREGN	PGAGN[1:0]		ADGN[2:0]		xxxx xxxx	uuuu uuuu	***** 1 1 1 1 1 1 1		
03Fh	AD1CN2	-	-	-	-	DCSET[3:0]			xxxx xxxx	uuuu uuuu	***** 1 1 1 1 1 1 1		
040h	AD1CN3	INP[3:0]			INN[3:0]			xxxx xxxx	uuuu uuuu	***** 1 1 1 1 1 1 1			
041h	AD1CN4	VRH[1:0]		VRL[1:0]		INX[1:0]		VRIS	INIS	0000 0000	uuuu uuuu	***** 1 1 1 1 1 1 1	
042h	AD1CN5	ENACM	-	VCMS	LDOPL	-	-	ENTPS	TPSCH	0000 0000	uuuu uuuu	***** 1 1 1 1 1 1 1	
043h	LVDCN	-	-	PWRS	LVDS[3:0]			LVDO	0000 0000	uuuu uuuu	***** 1 1 1 1 1 1 1		
044h	TMA1CN	ENTMA1	TMACL1	TMAS1	DTMA1[2:0]		-	0000 0000	u0uu uuuu	*r,w 1,1,1,1,1,1,1			
045h	TMA1R	TMA1 counter Register									0000 0000	uuuu uuuu	rw0, rw0, rw0, rw0, rw0, rw0, rw0
046h	TMA1C	TMA1C counter Register									0000 0000	uuuu uuuu	rw0, rw0, rw0, rw0, rw0, rw0, rw0
047h	PT1	-	-	PT1.5	PT1.4	PT1.3	PT1.2	PT1.1	PT1.0	xxxx xxxx	xxxx xxxx	***** 1 1 1 1 1 1 1	
048h	TRISC1	-	-	TC1.5	TC1.4	TC1.3	TC1.2	TC1.1	TC1.0	xx00 0000	uuuu uuuu	***** 1 1 1 1 1 1 1	
049h	PT1DA	-	-	-	-	-	DA1.2	-	-	xxxx x0xx	uuuu uuuu	***** 1 1 1 1 1 1 1	
04Ah	PT1PU	-	-	PU1.5	PU1.4	PU1.3	PU1.2	PU1.1	PU1.0	xx11 1111	uuuu uuuu	***** 1 1 1 1 1 1 1	
04Bh	PT1M1	-	-	-	-	INTEG1[1:0]		INTEG0[1:0]		0000 0000	uuuu uuuu	***** 1 1 1 1 1 1 1	
04Ch	PT8	-	-	-	-	-	-	PT8.1	PT8.0	xxxx xxxx	uuuu uuuu	***** 1 1 1 1 1 1 1	
04Dh	TRISC8	-	-	-	-	-	-	TC8.1	TC8.0	xxxx xx00	uuuu uuuu	***** 1 1 1 1 1 1 1	
04Eh	PT8DA	-	-	-	-	-	-	DA8.1	DA8.0	xxxx xx00	uuuu uuuu	***** 1 1 1 1 1 1 1	
04Fh	PT8PU	-	-	-	-	-	-	PUB.1	PUB.0	xxxx xx11	uuuu uuuu	***** 1 1 1 1 1 1 1	
050h	UR0CN	ENSP	ENTX	TX9	TX9D	PARITY	-	-	WUE	0000 0.0	uuuu u..u	***** 1 1 1 1 1 1 1	
051h	UR0STA	-	RC9D	PERR	FERR	OERR	RCIDL	TRMT	ABDOVF	.000 0010	.uuu uuuu	-r,r,r,r r,r,r,rw 0	
052h	BA0CN	-	-	-	-	ENCR	RC9	ENADD	ENABD 0000 uuuu	-,-,-,-,***** 1 1 1 1 1 1 1	
053h	BG0RH	-	-	-	Baud Rate Generator Register High Byte				...x xxxx	...u uuuu	-,-,-,-,***** 1 1 1 1 1 1 1		
054h	BG0RL	Baud Rate Generator Register Low Byte								xxxx xxxx	uuuu uuuu	***** 1 1 1 1 1 1 1	
055h	TX0R	UART Transmit Register									xxxx xxxx	uuuu uuuu	***** 1 1 1 1 1 1 1
056h	RC0REG	UART Receive Register									xxxx xxxx	uuuu uuuu	r,r,r,r,r r,r,r,r,r
057h	LCDCN1	ENLCP	LCDV[2:0]			ENLB	SELPCLK	-	-	0000 0000	uuuu uuuu	***** 1 1 1 1 1 1 1	
058h	LCDCN2	-	-	-	-	-	-	LCDBL	LCI00uu	***** 1 1 1 1 1 1 1	
059h	LCDCN3	SCM3[1:0]		SCM2[1:0]		SCM1[1:0]		SCM0[1:0]		1111 1111	uuuu uuuu	***** 1 1 1 1 1 1 1	
05Ah	LCDCN4	-	-	-	-	-	-	SSG15	SSG14	0000 0000	uuuu uuuu	***** 1 1 1 1 1 1 1	
05Bh	LCD0	LCD SEG3[4:7] data				LCD SEG2[3:0] data				xxxx xxxx	uuuu uuuu	***** 1 1 1 1 1 1 1	
05Ch	LCD1	LCD SEG5[4:7] data				LCD SEG4[3:0] data				xxxx xxxx	uuuu uuuu	***** 1 1 1 1 1 1 1	
05Dh	LCD2	LCD SEG7[4:7] data				LCD SEG6[3:0] data				xxxx xxxx	uuuu uuuu	***** 1 1 1 1 1 1 1	
05Eh	LCD3	LCD SEG9[4:7] data				LCD SEG8[3:0] data				xxxx xxxx	uuuu uuuu	***** 1 1 1 1 1 1 1	
05Fh	LCD4	LCD SEG11[4:7] data				LCD SEG10[3:0] data				xxxx xxxx	uuuu uuuu	***** 1 1 1 1 1 1 1	
060h	LCD5	LCD SEG13[4:7] data				LCD SEG12[3:0] data				xxxx xxxx	uuuu uuuu	***** 1 1 1 1 1 1 1	
061h	LCD6	LCD SEG15[4:7] data				LCD SEG14[3:0] data				xxxx xxxx	uuuu uuuu	***** 1 1 1 1 1 1 1	
080h ~ 17Fh	SRAM as 256Byte									uuuu uuuu	uuuu uuuu	***** 1 1 1 1 1 1 1	

表 5-2 資料記憶體列表(續)

6. 電氣特性

Absolute Maximum Ratings :

Absolute maximum ratings over operating free-air temperature (unless otherwise noted)

Voltage applied at VDD to VSS	-0.2 V to 6.0 V
Voltage applied to any pin	-0.2 V to VDD + 0.3 V
Voltage applied to RST/VPP pin	-0.2 V to 8.0 V
Diode current at any device terminal	±2 mA
Storage temperature, Tstg: (unprogrammed device)	-55°C to 125°C
(programmed device)	-40°C to 85°C
Total power dissipation.	0.5w
Maximum output current sink by any I/O pin.	10mA

6.1. Recommended operating conditions

TA = -40°C ~ 85°C, unless otherwise noted

Sym.	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
VDD	Supply Voltage	All digital peripherals and CPU	2.0		5.5	V
VDDA	Supply Voltage	Analog peripherals	2.4		5.0	
VSS	Supply Voltage		0		0	

6.2. Internal RC Oscillator

TA = 25°C, VDD = 3.0V, unless otherwise noted

Sym.	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
HAO	High Speed Oscillator frequency	ENHAO[0]=1, HAOM[1:0]=00	-20%	1.843	+20%	MHz
		ENHAO[0]=1, HAOM[1:0]=01	-20%	3.686	+20%	MHz
		ENHAO[0]=1, HAOM[1:0]=11	-20%	7.834	+20%	MHz
		After Frequency Trim by Writer	-2%		+2%	MHz
LPO	Low Power Oscillator frequency	VDD supply voltage be enable LPO	-20%	14.5	+20%	KHz

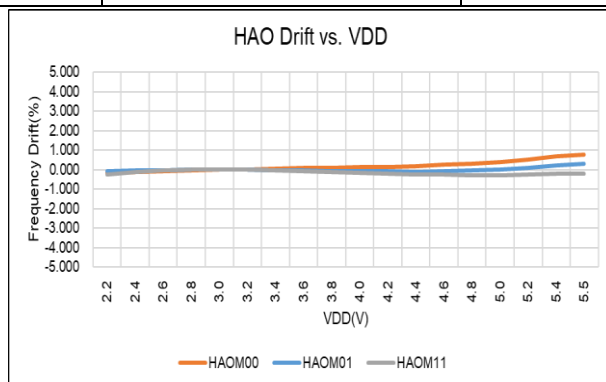


Figure 6.2-1 HAO vs. VDD

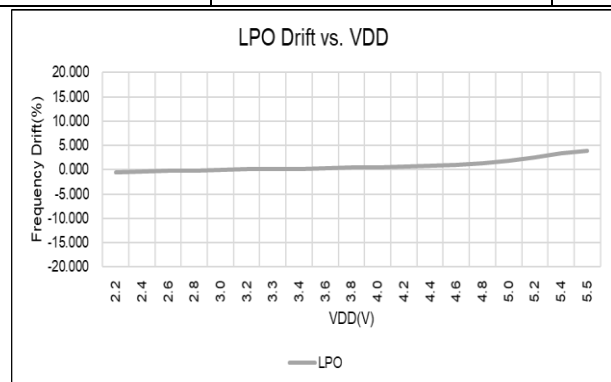


Figure 6.2-2 LPO vs. VDD

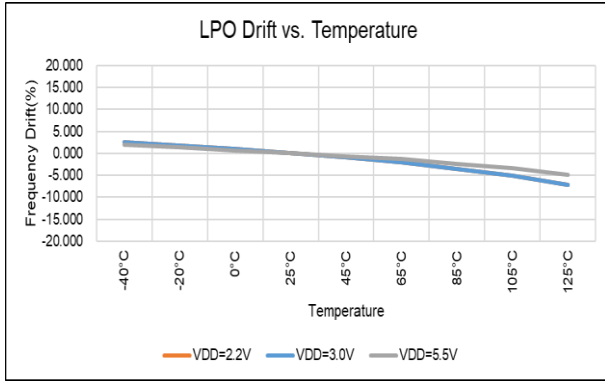


Figure 6.2-3 LPO vs. Temperature

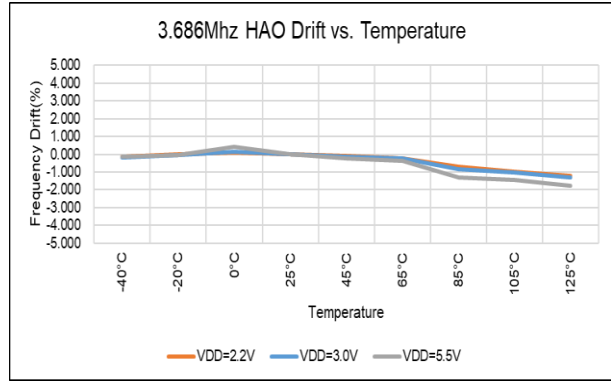


Figure 6.2-4 HAO(3.686MHz) vs. Temperature

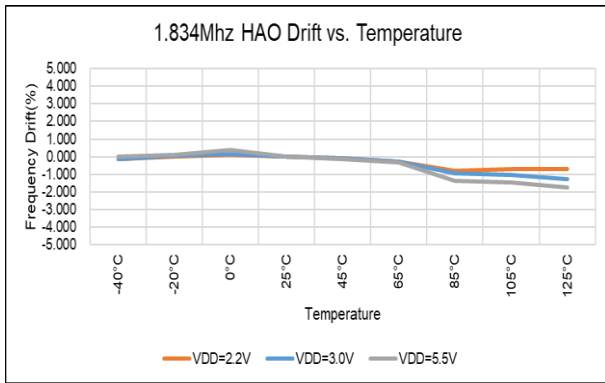


Figure 6.2-4 HAO(1.843MHz) vs. Temperature

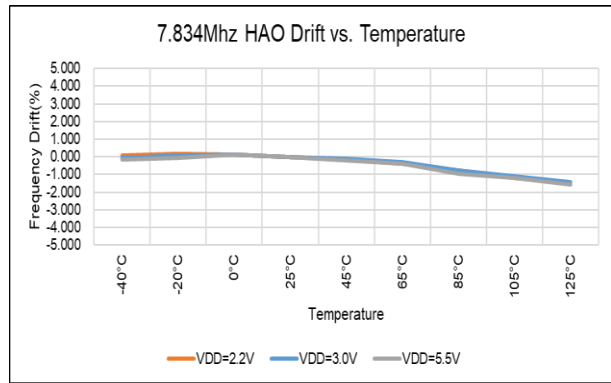


Figure 6.2-6 HAO(7.834MHz) vs. Temperature

6.3. Supply current into VDD excluding peripherals current

TA = 25°C, VDD = 3.0V, OSC_LPO = 14.5KHz, , unless otherwise noted

Sym.	Parameter	Test Conditions	Min.	Typ.	Max.	unit
I _{AM2}	Active mode 2	OSC_CY = off, OSC_HAO = 3.686MHz, CPU_CK = 3.686MHz		320	650	uA
I _{AM5}	Active mode 5	OSC_CY = off, OSC_HAO = 3.686MHz, CPU_CK = 3.686MHz/2		250	500	uA
I _{LP1}	Low Power 1	OSC_CY = off, OSC_HAO=off, CPU_CK = LPO		2	5	uA
I _{LP2}	Low Power 2	OSC_CY = off, OSC_HAO=off, CPU_CK = LPO, Idle state		1.1	2.5	uA
I _{LP3}	Low Power 3	OSC_CY = off, OSC_HAO=off, CPU_CK = off, Sleep state		0.4	1.0	uA

OSC_HAO : Internal High Accuracy Oscillator frequency.
CPU_CK : CPU core work frequency.

TA = 25°C, VDD = 5.5V, OSC_LPO = 14.5KHz, , unless otherwise noted

Sym.	Parameter	Test Conditions	Min.	Typ.	Max.	unit
I _{AM2}	Active mode 2	OSC_CY = off, OSC_HAO = 3.686MHz, CPU_CK = 3.686MHz		720	1200	uA
I _{AM5}	Active mode 5	OSC_CY = off, OSC_HAO = 3.686MHz, CPU_CK = 3.686MHz/2		600	900	uA
I _{LP1}	Low Power 1	OSC_CY = off, OSC_HAO=off, CPU_CK = LPO		4	10	uA
I _{LP2}	Low Power 2	OSC_CY = off, OSC_HAO=off, CPU_CK = LPO, Idle state		2.5	5	uA
I _{LP3}	Low Power 3	OSC_CY = off, OSC_HAO=off, CPU_CK = off, Sleep state		0.4	2	uA

OSC_HAO : Internal High Accuracy Oscillator frequency.
CPU_CK : CPU core work frequency.

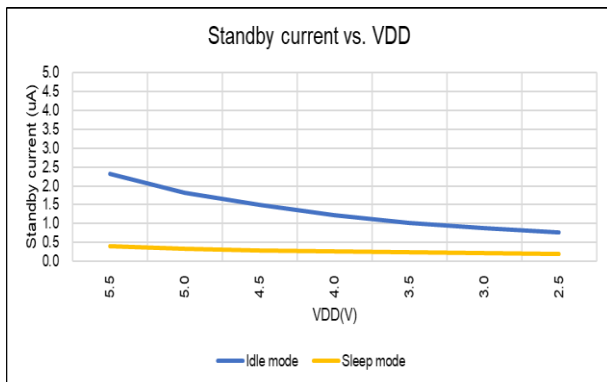


Figure 6.3-1 Standby current vs. VDD

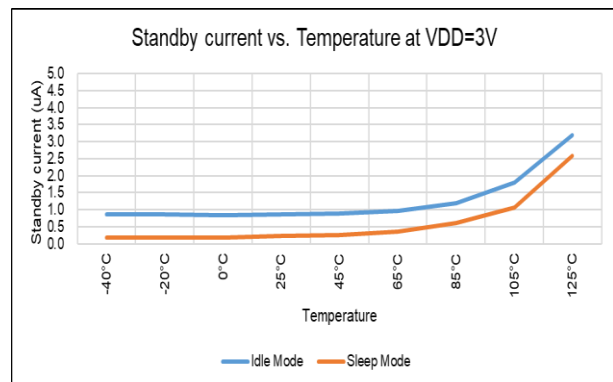


Figure 6.3-2 Standby current vs. Temperature VDD=3V

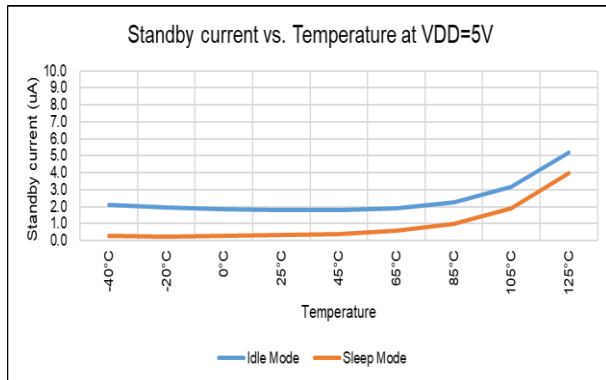


Figure 6.3-3 Standby current vs. Temperature at VDD=5V

6.4. Port 1 & 8

TA = 25°C, VDD = 3.0V, unless otherwise noted

Sym.	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
Input voltage and Schmitt trigger and leakage current and timing						
V _{IH}	High-Level input voltage				0.7*VDD	V
V _{IL}	Low-Level input voltage		0.3*VDD			
V _{hys}	Input Voltage hysteresis(V _{IH} - V _{IL})			0.3*VDD		V
I _{LKG}	Leakage Current				0.1	uA
R _{PU}	Port pull high resistance(PT1 ~ PT2)			60		kΩ
	Port pull high resistance(PT8)			60		kΩ
Output voltage and current and frequency						
V _{OH}	High-level output voltage	VDD<4V, I _{OH} =3mA,	VDD -0.3			V
		VDD>=4V, I _{OH} =5mA,	VDD -0.3			
V _{OL}	Low-level output voltage	VDD<4V, I _{OL} =-3mA	VSS +0.3			V
		VDD>=4V, I _{OL} =-5mA	VSS +0.3			

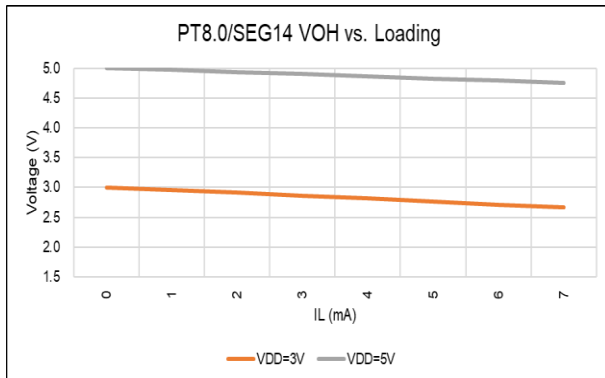


Figure 6.4-1 PT8.0/SEG14 VOH vs. Loading

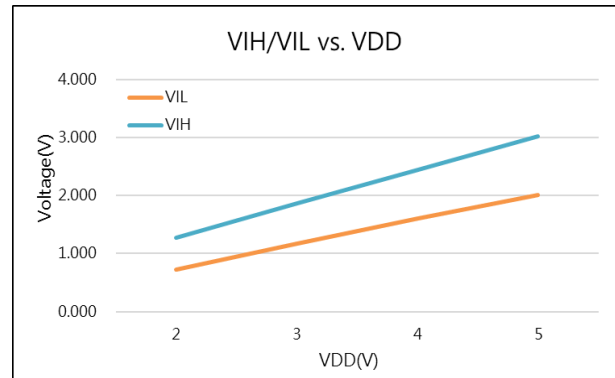


Figure 6.4-2 V_{IH}/V_{IL} vs. VDD

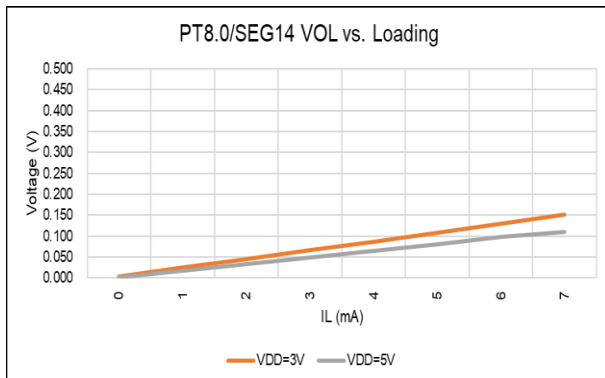


Figure 6.4-3 PT8.0/SEG14 VOL vs. Loading

HY17P51

Embedded High Resolution $\Sigma\Delta$ ADC
8-Bit RISC-like Mixed Signal Microcontroller



6.5. Port 1.4~1.5

TA = 25°C, VDD = 3.0V, unless otherwise noted

Sym.	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
Input voltage and Schmitt trigger and leakage current and timing						
V _{IH}	High-Level input voltage				0.7*VDD	V
V _{IL}	Low-Level input voltage		0.3*VDD			
V _{hys}	Input Voltage hysteresis(V _{IH} - V _{IL})			0.3*VDD		V
I _{LKG}	Leakage Current				0.1	uA
R _{PU}	Port pull high resistance			60		kΩ
Output voltage and current and frequency						
V _{OH}	High-level output voltage	VDD=3V, I _{OH} =10mA,	VDD -0.4			V
		VDD=5V, I _{OH} =15mA,	VDD -0.4			
V _{OL}	Low-level output voltage	VDD=3V, I _{OL} =-10mA			VSS +0.4	
		VDD=5V, I _{OL} =-15mA			VSS +0.4	

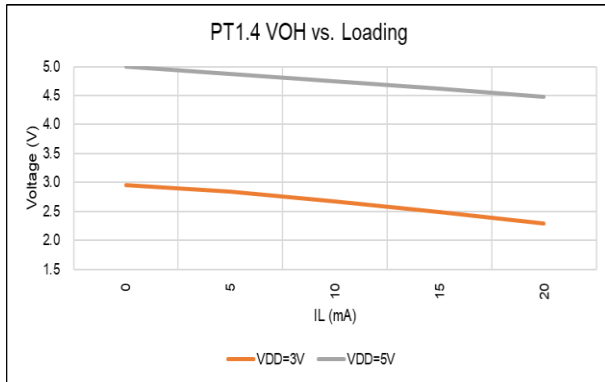


Figure 6.5-1 PT1.4 VOH vs. Loading

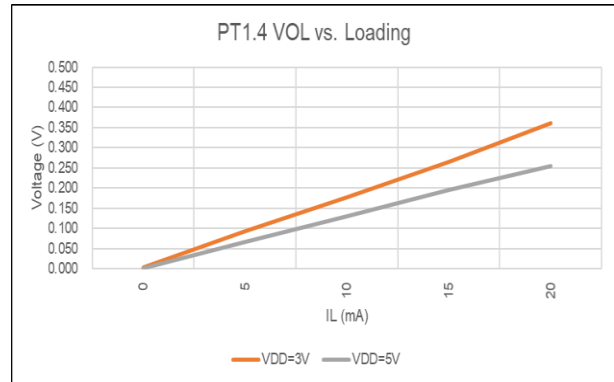


Figure 6.5-2 PT1.4 VOL vs. Loading

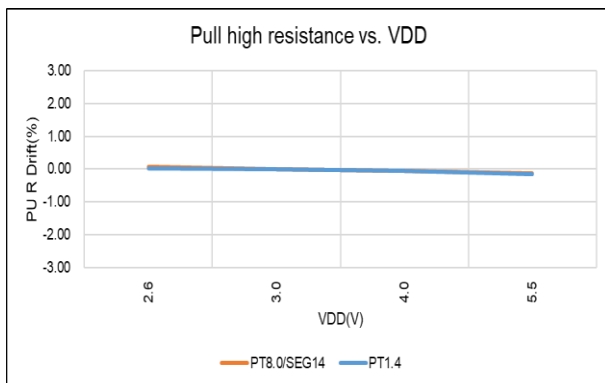


Figure 6.5-3 Pull high resistance vs. VDD

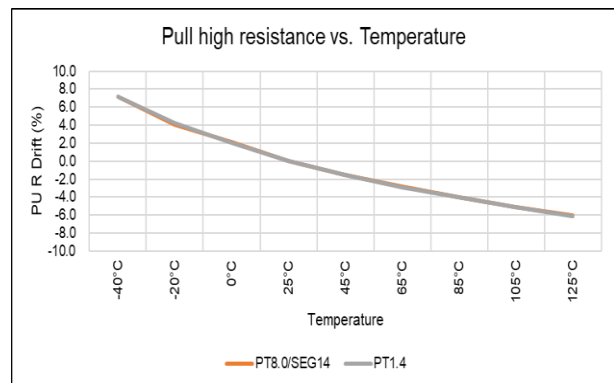


Figure 6.5-4 Pull high resistance vs. Temperature

6.6. Reset(Brownout, Low Voltage Detect)

TA = 25°C, VDD = 3.0V, unless otherwise noted

Sym.	Parameter	Test Conditions	Min.	Typ.	Max.	unit
BOR1	Pulse length needed to accepted reset internally, t_{d-LVR1}		2			uS
	VDD Start Voltage to accepted reset internally (L→H), V_{HYS1}		1.6	1.8	2.0	V
	BOR1 current, I_{BOR1}			0.4		uA
	Temperature Drift			5		%
LVD	Operation current, I_{LVD}			10		uA
	External input voltage to compare reference voltage		1.15	1.2	1.25	V
	Compare reference voltage temperature drift	TA = -40°C ~ 85 °C		50		ppm/°C
	Detect VDD voltage rang by user option, VSVS VLDS[3:0]=1110b		-0.1	4.0	+0.1	V
	Detect VDD voltage rang by user option, VSVS VLDS[3:0]=1101b			3.6		
	Detect VDD voltage rang by user option, VSVS VLDS[3:0]=1100b			3.3		
	Detect VDD voltage rang by user option, VSVS VLDS[3:0]=1011b			3.0		
	Detect VDD voltage rang by user option, VSVS VLDS[3:0]=1010b			2.9		
	Detect VDD voltage rang by user option, VSVS VLDS[3:0]=1001b			2.8		
	Detect VDD voltage rang by user option, VSVS VLDS[3:0]=1000b			2.7		
	Detect VDD voltage rang by user option, VSVS VLDS[3:0]=0111b			2.6		
	Detect VDD voltage rang by user option, VSVS VLDS[3:0]=0110b			2.5		
	Detect VDD voltage rang by user option, VSVS VLDS[3:0]=0101b			2.4		
	Detect VDD voltage rang by user option, VSVS VLDS[3:0]=0100b			2.3		
	Detect VDD voltage rang by user option, VSVS VLDS[3:0]=0011b			2.2		
	Detect VDD voltage rang by user option, VSVS VLDS[3:0]=0010b			2.1		
Detect VDD voltage rang by user option, VSVS VLDS[3:0]=0001b		2.0				

BOR1 : Brownout Reset 1
LVD : Low Voltage Detect

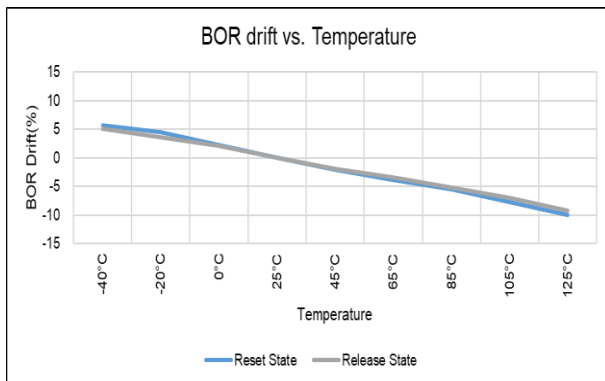


Figure 6.6-1 BOR vs. Temperature

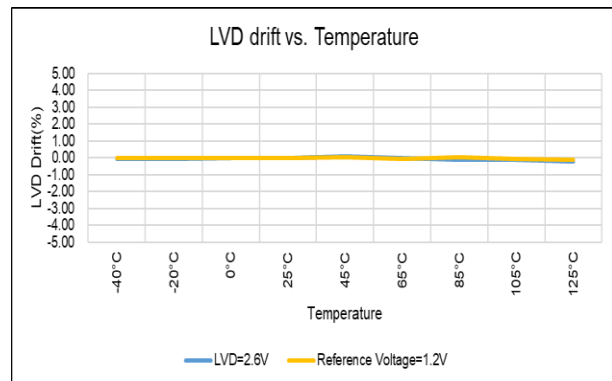


Figure 6.6-2 LVD drift vs. Temperature

6.7. Power System

TA = 25°C, VDD = 3.0V, unless otherwise noted

Sym.	Parameter	Test Conditions		Min.	Typ.	Max.	Unit
VDDA	VDDA operation current, I_{VDDA}	$I_L = 0\text{mA}$	LDOC[2:0]=000b	20			μA
	Select VDDA output voltage	$I_L = 0.1\text{mA}$, $VDD \geq VDDA + 0.25\text{V}$	LDOC [2:0]=000b	-5%	2.4	+5%	V
			LDOC [2:0]=100b		3.6		V
	Dropout voltage	$I_L = 10\text{mA}$	LDOC [2:0]=000b		500		mV
	Temperature drift	LDOC [2:0]=000b $I_L = 0.1\text{mA}$	TA=-40°C~85°C	50			PPM/°C
VDD Voltage drift	LDOC [2:0]=000b	VDD=2.2V~5.5V	±0.2			%/V	
VDDA/2	operation current, I_{ACM}	ENADC[0]=1b,	ENACM [0]=1b	50			μA
	Internal Analog Common Mode Voltage, $V_{ACM}=VDDA/2$		$I_L = 0\mu\text{A}$	VDDA/2			V
	Temperature drift	ENADC[0]=1b,	TA=-40°C~85°C, ENACM [0]=1b	50			PPM/°C
V12	operation current, I_{V12}	ENADC[0]=1b,	ENV12 [0]=1b	50			μA
	Internal Analog Common Mode Voltage, $V_{ACM}=V12$		$I_L = 0\mu\text{A}$	1.1	1.2	1.3	V
	Temperature drift	ENADC[0]=1b,	TA=-40°C~85°C, ENV12 [0]=1b	50			PPM/°C

VDDA : Adjust Voltage Regulator,
ACM : Internal Analog Common Mode Voltage VDDA/2 (No voltage output)

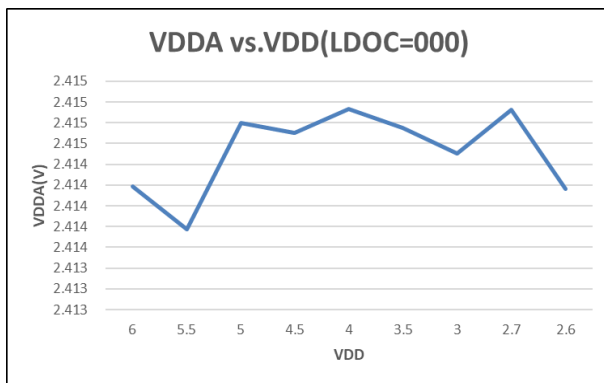


Figure 6.7-1 VDDA Drift vs. VDD

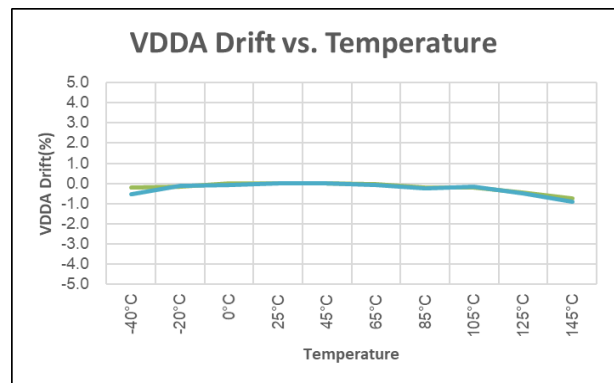


Figure 6.7-2 VDDA Drift vs. Temperature

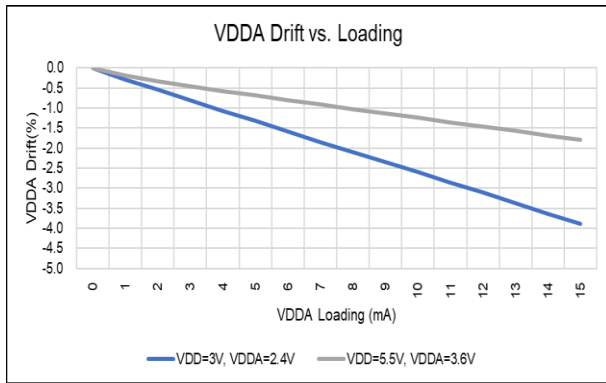


Figure 6.7-3 VDDA Drift vs. Loading

6.8. LCD

TA = 25°C, VDD = 3.3V, CVLCD = 4.7uF, unless otherwise noted.

Sym.	Parameter	Test Conditions	Min.	Typ.	Max.	unit	
I _{LCD}	Operation supply current with output buffer.(all segment turn on, No load)	ENLCP[0]=1 VDD = 3.0V		5		uA	
VLCD	Supply Voltage at VLCD pin	ENLCP [0]=0	2.4		5	V	
	Embedded Charge Pump output voltage at VLCD pin	VDD = 3.3V, ENLCP [0]=1 CVLCD =4.7uF	LCDV[2:0]=111b	-10%	2.45	+10%	V
			LCDV[2:0]=110b	-10%	2.70	+10%	
			LCDV[2:0]=101b	-10%	2.85	+10%	
			LCDV[2:0]=100b	-10%	3.10	+10%	
			LCDV[2:0]=011b	-10%	3.30	+10%	
			LCDV[2:0]=010b	-10%	4.10	+10%	
			LCDV[2:0]=001b (VDD>2.4V mode)	-10%	4.55	+10%	
LCDV[2:0]=000b (VDD>2.75V)	-10%	5.1	+10%				
VDD Voltage drift	ENLCP [0]=1, CVLCD =4.7uF, LCDV[2:0]>010b, VDD=2.2V~ 5.5V; LCDV[2:0]=001b, VDD>2.4V; LCDV[2:0]=000b, VDD>2.75V;			4		%/V	
Z _{LCD}	Output impedance with LCD buffer	f _{LCD} =128Hz, VLCD=3.05V		10		kΩ	

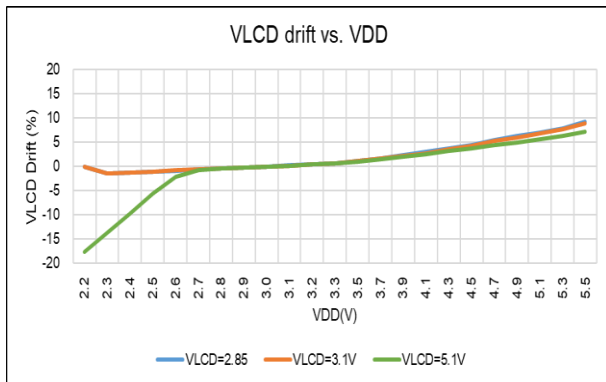


Figure6.8-1 VLCD drift vs. VDD

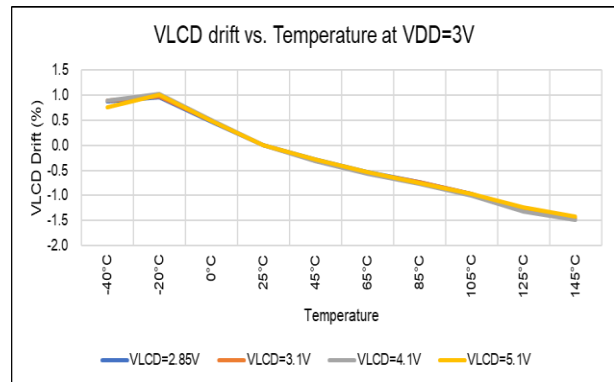


Figure6.8-2 VLCD drift vs. Temperature at VDD=3V

6.9. $\Sigma\Delta$ ADC, Power Supply and recommended operating conditions

TA = 25°C, VDD = 3.0V, VDDA=2.4V, unless otherwise noted

Sym.	Parameter	Test Conditions		Min.	Typ.	Max.	Unit
V _{SD18}	Supply Voltage at VDDA	ENLDO[0]=0		2.4		5.5	V
f _{SD18}	Modulator sample frequency, ADC_CK			230	921		KHz
	Over Sample Ratio, OSR			64		65536	
I _{SD18}	Operation supply current without PGA	ENAD1 [0]=1	GAIN =16, ADC_CK=921KHz		300		uA

6.9.1. PGA, Power Supply and recommended operating conditions

TA = 25°C, VDD = 3.0V, VDDA=2.4V, unless otherwise noted

Sym.	Parameter	Test Conditions		Min	Typ.	Max.	Unit
V _{PGA}	Supply Voltage at VDDA	ENLDO [0]=0		2.4		5.5	V
I _{PGA}	Operation supply current	PGAGN[1:0]=<11>			450		uA
G _{PGA}	Gain temperature drift	TA = -40°C~ 85°C	GAIN=128		14		ppm/°C

6.9.2. $\Sigma\Delta$ ADC, performance

TA = 25°C, VDD = 3.6V, VDDA=2.4V, V_{VR}= AI2(short to VDDA)/2

GAIN=16 with PGA=8, f_{SD18}=921KHz, unless otherwise noted

Sym.	Parameter	Test Conditions		Min.	Typ.	Max.	Unit
INL	Integral Nonlinearity(INL)	VDDA=2.4V, VVR= AI2/2, Δ SI=±450mV			±0.003	±0.01	%FSR
	No Missing Codes ³	ADC_CK=921KHz, OSR[3:0]=0000b		23			Bits
G _{SD18}	Temperature drift Gain x16	TA = -40°C~ 85°C			10		ppm/°C
E _{OS}	Offset error of Full Scale Rang input voltage range with Chopper without PGA	Δ AI=0V Δ V _R =1.2V DCSET[3:0]=<0000> * Δ AI is external short	Gain=2			1	%FSR
	Offset temperature drift with chopper without PGA		GAIN=1		2		uV/°C
			GAIN=2		1		
			GAIN=4		0.5		
Offset temperature drift with chopper		GAIN=16		0.15			
CM _{SD18}	Common-mode rejection	V _{CM} =0.7V to 1.7V, V _{VR} = 1.0V, without PGA	V _{SI} =0V, GAIN=1		90		dB
			V _{SI} =0V,		75		dB

			GAIN=16		
PSRR	DC power supply rejection	VDDA=3.0V $\Delta V_{DDA}=\pm 100\text{mV}$, $V_{VR}=1.0\text{V}$, $V_{SI}=1.2\text{V}, V_{SI}=-1.2\text{V}$,	GAIN=1	75	dB
			PGA=off		GAIN=16
			PGA=8		

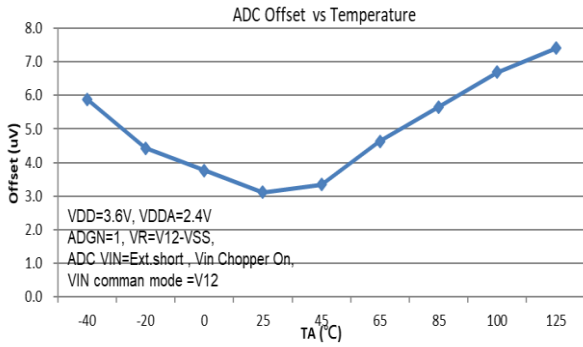


Figure 6.9-1 ADC Offset drift with Temperature (Gain=1)

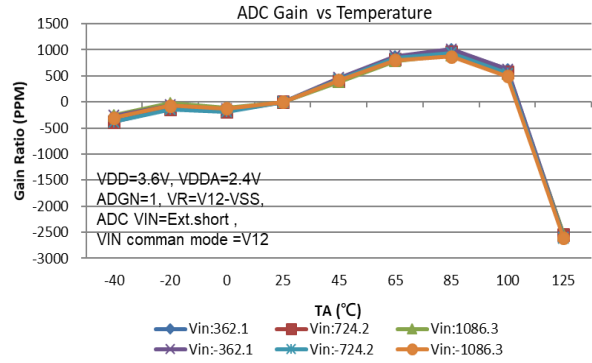


Figure 6.9-2 ADC Gain drift with Temperature (Gain=1)

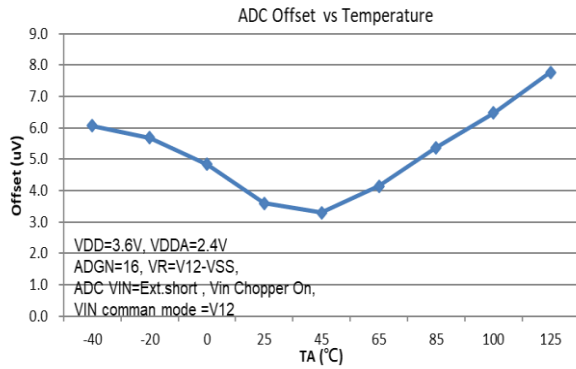


Figure 6.9-3 ADC Offset drift with Temperature (Gain=16)

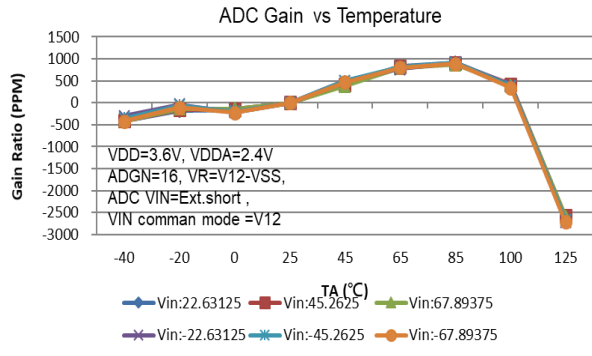


Figure 6.9-4 ADC Gain drift with Temperature (Gain=16)

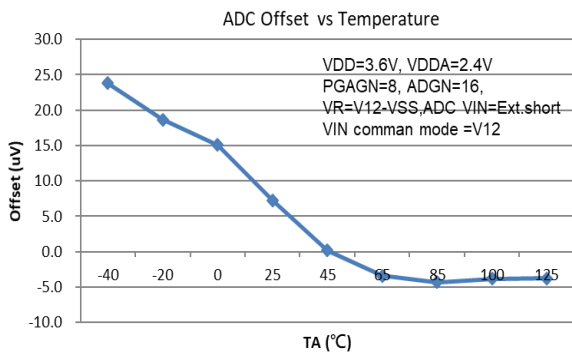


Figure 6.9-5 Offset drift with Temperature (Gain=128)

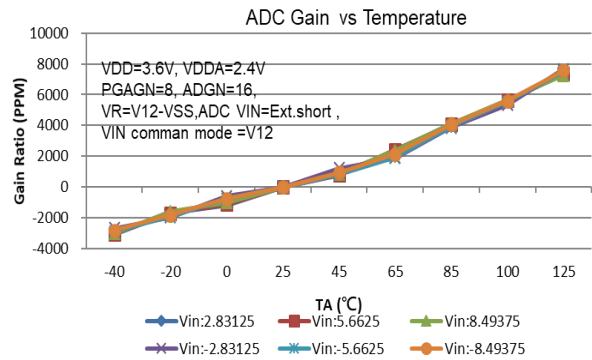


Figure 6.9-5 ADC Gain drift with Temperature (Gain=128)

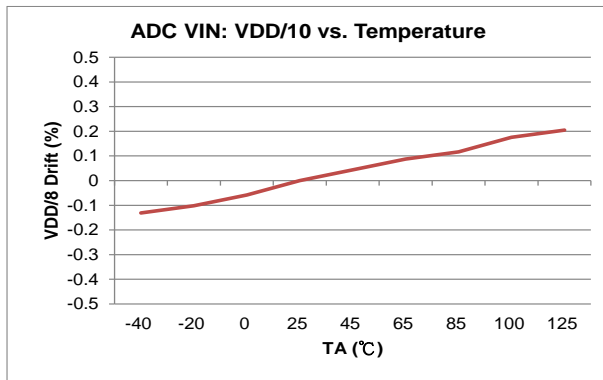


Figure 6.9-6 VDD/10 drift with Temperature

6.9.3. $\Sigma\Delta$ ADC Noise Performance

HY17P51 針對 $\Sigma\Delta$ ADC 提供了重要的輸入雜訊規格。下表列出典型的雜訊規格表與 Gain, Output rate, 及差動最大輸入電壓等關係。測試條件設定在外部輸入訊號短路到 VDDA/2 電位下，取樣 1024 筆資料。

ENOB(RMS) with OSR/GAIN at A/D Clock=921KHz, VDD=3.6V, VDDA=2.4V, VREF=1.2V																
Max. Vin(mV) =0.9VREF ⁽¹⁾	OSR				64	128	256	512	1024	2048	4096	8196	16384	32768	65536	
	Output rate(Hz)				15625	7813	3906	1953	977	488	244	122	61	28	14	
	Gain	=	PGAGN	x												ADGN
±1080	1	=	off	x	1	14.05	15.24	15.8	16.24	16.65	17.03	17.52	18.09	18.56	18.98	19.52
±270	4	=	off	x	4	14.09	15.14	15.59	16.02	16.6	16.87	17.31	17.82	18.29	18.74	19.1
±68	16	=	off	x	16	11.95	14.88	15.39	15.94	16.47	16.81	17.21	17.73	18.13	18.6	19.02
±135	8	=	8	x	1	13.67	15.14	15.6	16.04	16.47	16.88	17.35	17.87	18.42	18.87	19.34
±8.5	128	=	8	x	16	11.61	12.63	13.13	13.55	14.11	14.47	14.92	15.36	15.96	16.46	16.92

(1) Max. Vin(mV) is the max. input voltage single end to ground(VSS)

RMS(uV) with OSR/GAIN at A/D Clock=921KHz, VDD=3.6V, VDDA=2.4V, VREF=1.2V																
Max. Vin(mV) =0.9VREF ⁽¹⁾	OSR				64	128	256	512	1024	2048	4096	8196	16384	32768	65536	
	Output rate(Hz)				15625	7813	3906	1953	977	488	244	122	61	28	14	
	Gain	=	PGAGN	x												ADGN
±1080	1	=	off	x	1	142.74	62.37	42.43	31.17	23.40	18.04	12.83	8.65	6.22	4.65	3.20
±270	4	=	off	x	4	34.62	16.74	12.22	9.06	6.06	5.03	3.71	2.61	1.88	1.38	1.08
±68	16	=	off	x	16	38.02	4.99	3.52	2.41	1.66	1.32	0.99	0.69	0.53	0.38	0.28
±135	8	=	8	x	1	23.17	8.36	6.06	4.47	3.33	2.50	1.80	1.26	0.86	0.63	0.46
±8.5	128	=	8	x	16	6.05	2.97	2.11	1.58	1.07	0.83	0.61	0.45	0.30	0.21	0.15

Table6.9-4(a) D18 ENOB and RMS Noise Table at VDDA=2.4V

ENOB(RMS) with OSR/GAIN at A/D Clock=1MHz, VDD=3.6V, VDDA=2.4V, VREF=1.2V at High Accuracy Mode																
Max. Vin(mV) =0.9VREF ⁽¹⁾	OSR				64	128	256	512	1024	2048	4096	8196	16384	32768	65536	
	Output rate(Hz)				7813	3906	1953	977	488	244	122	61	31	14	7	
	Gain	=	PGAGN	x												ADGN
±1080	1	=	off	x	1	14.95	15.76	16.25	16.8	17.13	17.51	17.99	18.51	19	19.61	20.04
±270	4	=	off	x	4	14.94	15.64	16.07	16.52	17.02	17.34	17.83	18.43	18.92	19.39	19.82
±68	16	=	off	x	16	14.75	15.44	15.89	16.46	16.96	17.32	17.79	18.3	18.81	19.22	19.62
±135	8	=	8	x	1	14.94	15.59	16.1	16.59	17.06	17.37	17.89	18.31	18.92	19.37	19.81
±8.5	128	=	8	x	16	12.57	12.89	13.53	13.94	14.48	14.68	15.25	15.85	16.38	16.98	17.49

(1) Max. Vin(mV) is the max. input voltage single end to ground(VSS)

RMS Noise(uV) with OSR/GAIN at A/D Clock=1MHz, VDD=3.6V, VDDA=2.4V, VREF=1.2V at High Accuracy Mode																
Max. Vin(mV) =0.9VREF ⁽¹⁾	OSR				64	128	256	512	1024	2048	4096	8196	16384	32768	65536	
	Output rate(Hz)				7813	3906	1953	977	488	244	122	61	31	14	7	
	Gain	=	PGAGN	x												ADGN
±1080	1	=	off	x	1	76.21	43.47	30.92	21.16	16.80	12.95	9.29	6.45	4.61	3.01	2.24
±270	4	=	off	x	4	19.21	11.84	8.76	6.40	4.53	3.63	2.59	1.71	1.22	0.88	0.65
±68	16	=	off	x	16	5.46	3.39	2.48	1.68	1.18	0.92	0.67	0.47	0.33	0.25	0.19
±135	8	=	8	x	1	9.62	6.11	4.30	3.06	2.20	1.78	1.24	0.93	0.61	0.44	0.33
±8.5	128	=	8	x	16	3.11	2.49	1.59	1.20	0.83	0.72	0.48	0.32	0.22	0.15	0.10

Table6.9-4(b) High Accuracy Mode, $\Sigma\Delta$ ADC ENOB and RMS Noise Table at VDDA=2.4V

The RMS Noise are referred to the input. The Effective Number of Bits (ENOB(RMS Bit)) is defined as:

$$ENOB(RMS) = \frac{\ln\left(\frac{FSR}{RMS\ Noise}\right)}{\ln(2)}$$

$$RMS\ Noise = \frac{\left(2 \times VREF \times \sqrt{\sum_{k=1}^{1024} (ADO[k] - Average)^2}\right)}{2^{23}}$$

Where FSR (Full - Scale Range) = $2 \times VREF / Gain$.

$$Average = \frac{\sum_{k=1}^{1024} (ADO[k])}{1024}$$

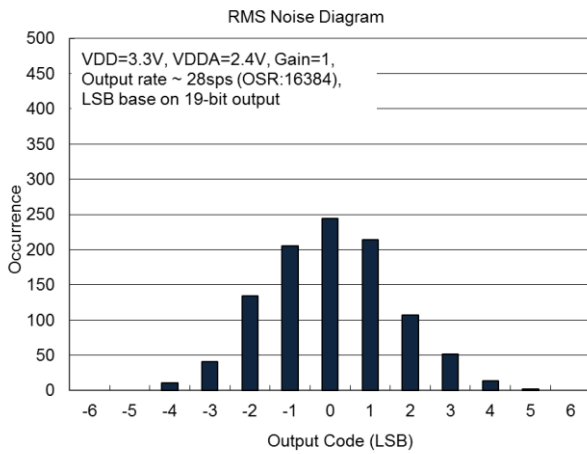


Figure 6.9-6 RMS Noise Diagram

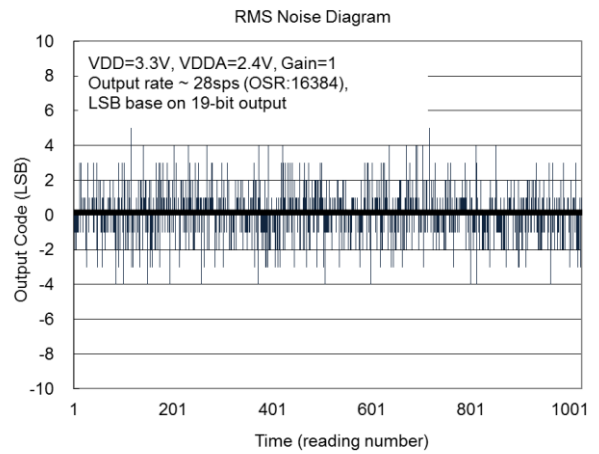


Figure 6.9-7 Output Code Diagram

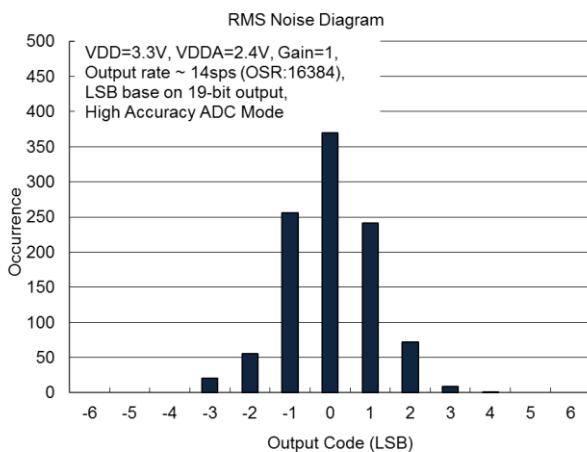


Figure 6.9-8 RMS Noise Diagram

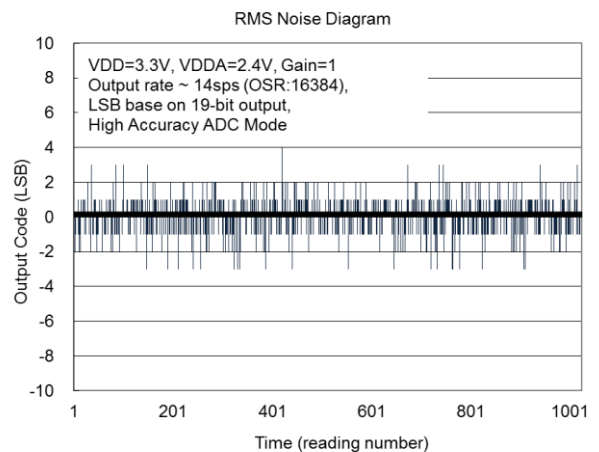


Figure 6.9-9 Output Code Diagram

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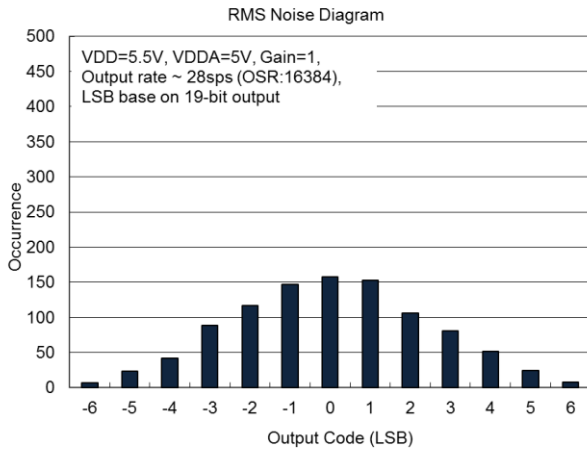


Figure 6.9-10 RMS Noise Diagram

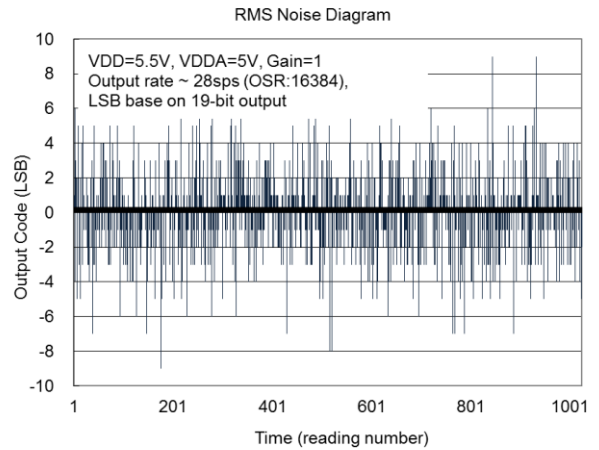


Figure 6.9-11 Output Code Diagram

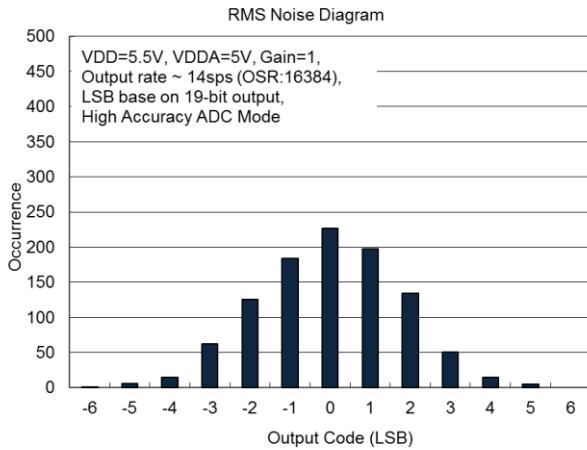


Figure 6.9-12 RMS Noise Diagram

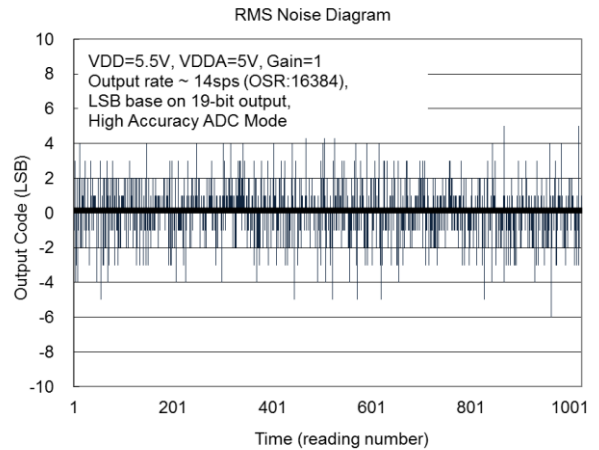


Figure 6.9-13 Output Code Diagram

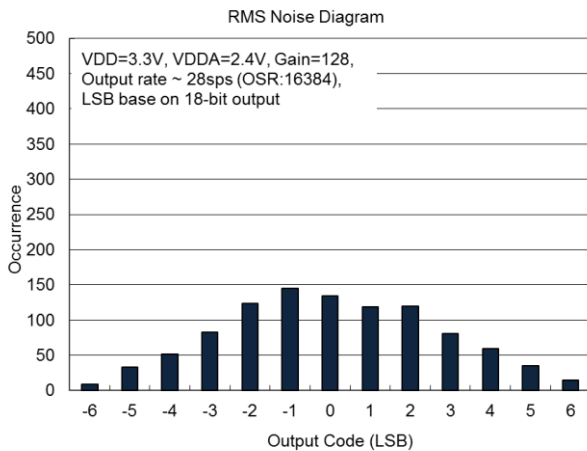


Figure 6.9-14 RMS Noise Diagram

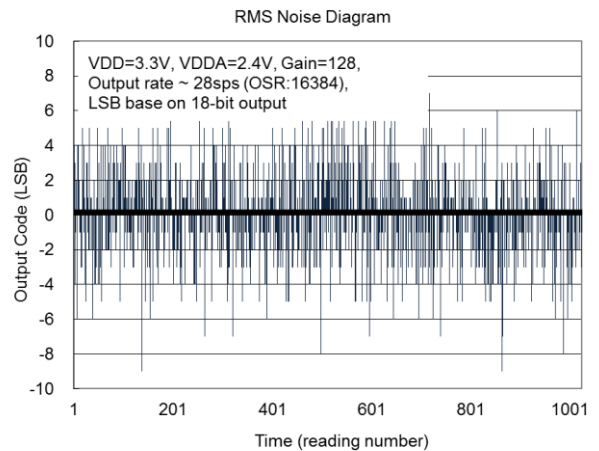


Figure 6.9-15 Output Code Diagram

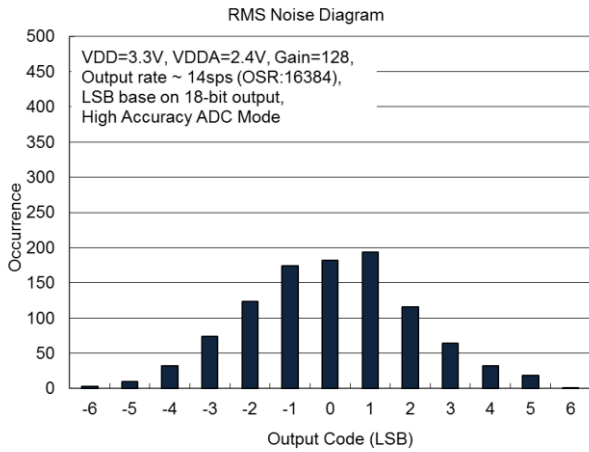


Figure 6.9-16 RMS Noise Diagram

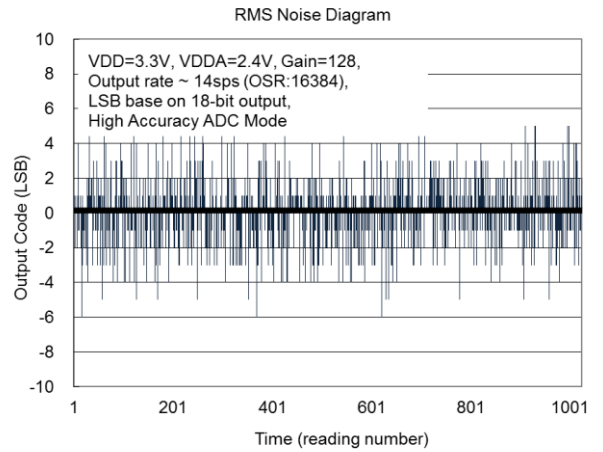


Figure 6.9-17 Output Code Diagram

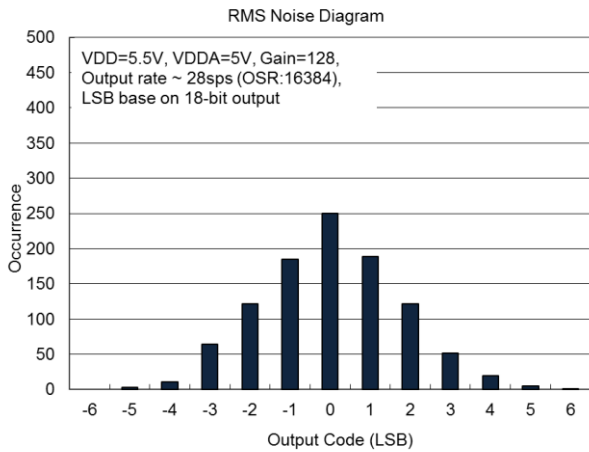


Figure 6.9-18 RMS Noise Diagram

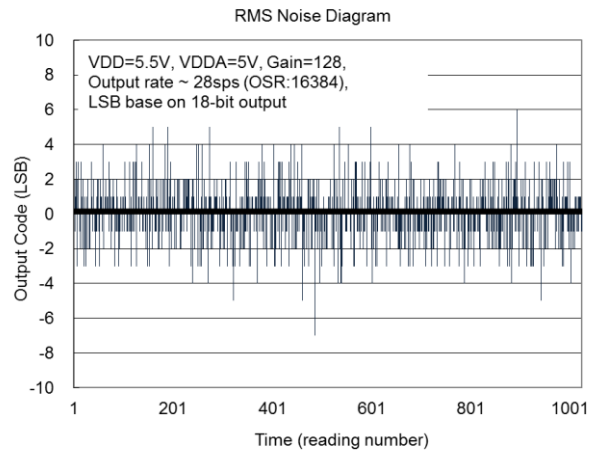


Figure 6.9-19 Output Code Diagram

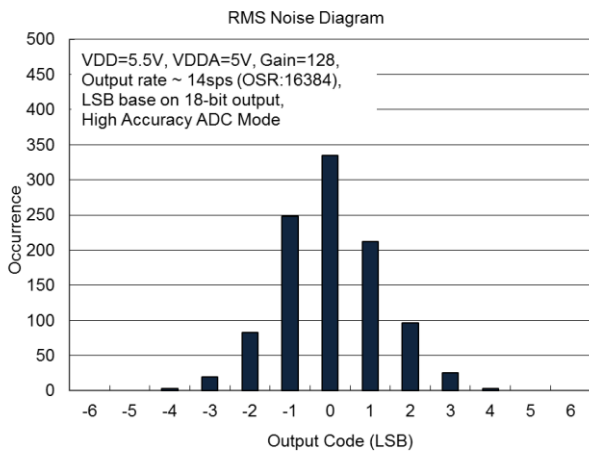


Figure 6.9-20 RMS Noise Diagram

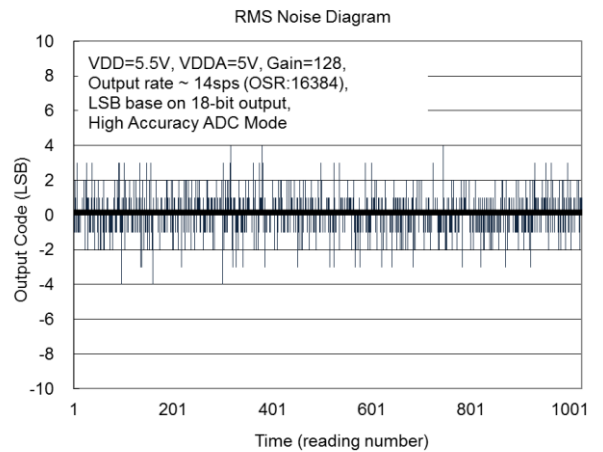


Figure 6.9-21 Output Code Diagram

6.9.4. $\Sigma\Delta$ ADC ,Temperature Sensor

TA = 25°C, VDD = 3.0V, VDDA=2.4V, unless otherwise noted

Sym.	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
TC _S	Sensor temperature drift			1.7		mV/°C
TC _{ERR}	One point calibrate error temperature	Calibration at 25°C of -40°C~85°C		±2		°C

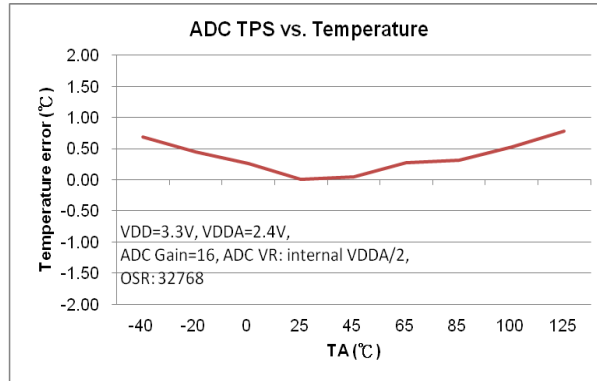


Figure 6.9-22 ADC Temperature Error

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6.10. Build-In EPROM(BIE)

TA = 25°C, VDD = 3.0V, unless otherwise noted

Sym.	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V _{BIE}	Supply Voltage at VPP PIN		7.5	7.75	8.0	V
I _{BIE}	Operation supply current				6.3	mA
V _{SS}	Supply Voltage			0		V

When connecting to the external VBIE power source to program the BIE block, users can use the instruction to program the words one by one into the BIE block.

6.11. Build-In EPROM(BIE) Low voltage control circuit

TA = 25°C, VDD = 3.05V, unless otherwise noted

Sym.	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
T _O	Operation temperature range		0	25	40	°C
V _{DD}	Operation supply Voltage		2.75		5.5	V
V _{SS}	Supply Voltage			0		V

When the 2.75V low voltage programming control circuit is activated, users can program the BIE block without connecting to the external VBIE power source.

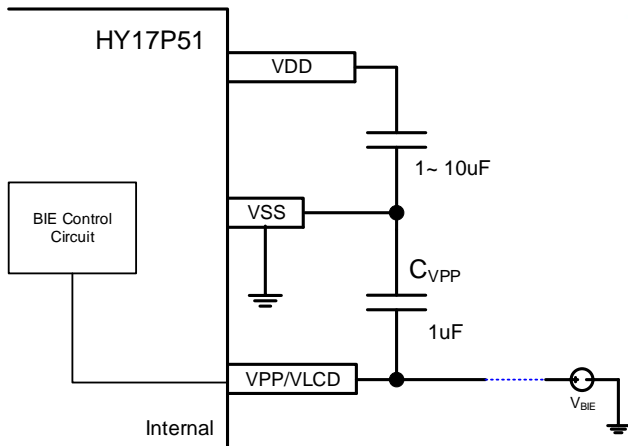


Figure 6.11-1 BIE typical application circuit

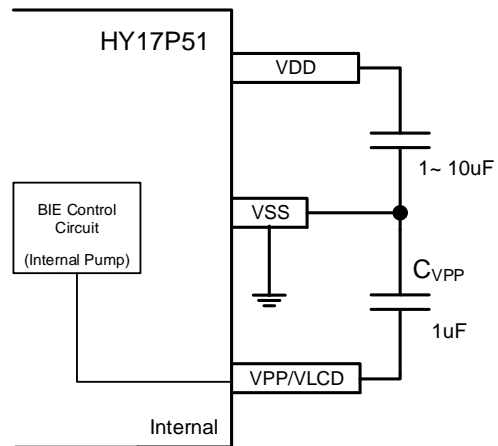


Figure 6.11-2 Use low voltage control circuit

7. 訂貨資訊

下單品名 1	封裝型式	引腳數	封裝型式		程式碼	出貨包裝 形式	個裝 數量	材料 組成	MSL3
			描述方式	編號 2					
HY17P51-NS32	QFN	32	N	S32	000	Tape & Reel	5000	Green4	MSL-3
HY17P51-N016	QFN	16	N	016	000	Tape & Reel	5000	Green4	MSL-3

¹ 產品名稱 – 封裝型式描述方式 – 程式碼編號 (空白片 / 標準品 / 代客燒錄碼)

例如：您的需求是 HY17P51 不帶程式碼的空白片且需要的產品是封裝片 QFN32 出貨，則下單品名為 HY17P51-NS32，且需以 Reel 出貨，則除下單品名外，請特別註明出貨包裝形式為 Reel

例如：您的 HY17P51 代客燒錄服務申請的程式碼編號為 008，而需求的產品是封裝片 QFN32 出貨，則下單品名為 HY17P51-NS32-008，且需以 Reel 出貨，則除下單品名外，請特別註明出貨包裝形式為 Reel

例如：您的需求是 HY17P51 不帶程式碼的空白片且需要的產品是封裝片 QFN16 出貨，則下單品名為 HY17P51-N016，且需以 Reel 出貨，則除下單品名外，請特別註明出貨包裝形式為 Reel

例如：您的 HY17P51 代客燒錄服務申請的程式碼編號為 009，而需求的產品是封裝片 QFN16 出貨，則下單品名為 HY17P51-N016-009，且需以 Reel 出貨，則除下單品名外，請特別註明出貨包裝形式為 Reel

² 程式碼編號

“001”~“999” 為標準品或代客燒錄申請的程式碼編號，而空白晶片不帶此碼。

³ MSL:

濕度敏感性等級係依據 IPC/JEDEC J-STD-020 的規範加以試驗分級，並參考 IPC/JEDEC J-STD-033 的標準處理、包裝、運輸與使用。

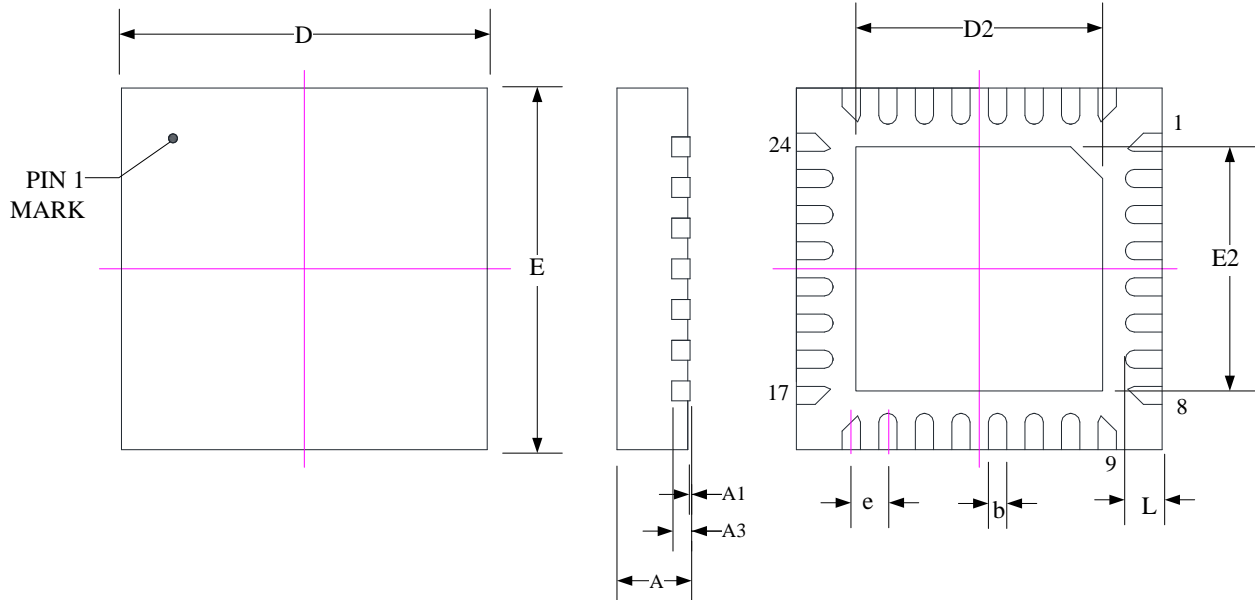
⁴ Green (RoHS & no Cl/Br):

HYCON 產品皆為 Green Product，符合 RoHS 指令，REACH 高關注物質(SVHC)以及無鹵素相關規定。

8. 封裝型式資訊

8.1. QFN32(NS32)

8.1.1. Package Dimensions QFN32(4x4x0.55)

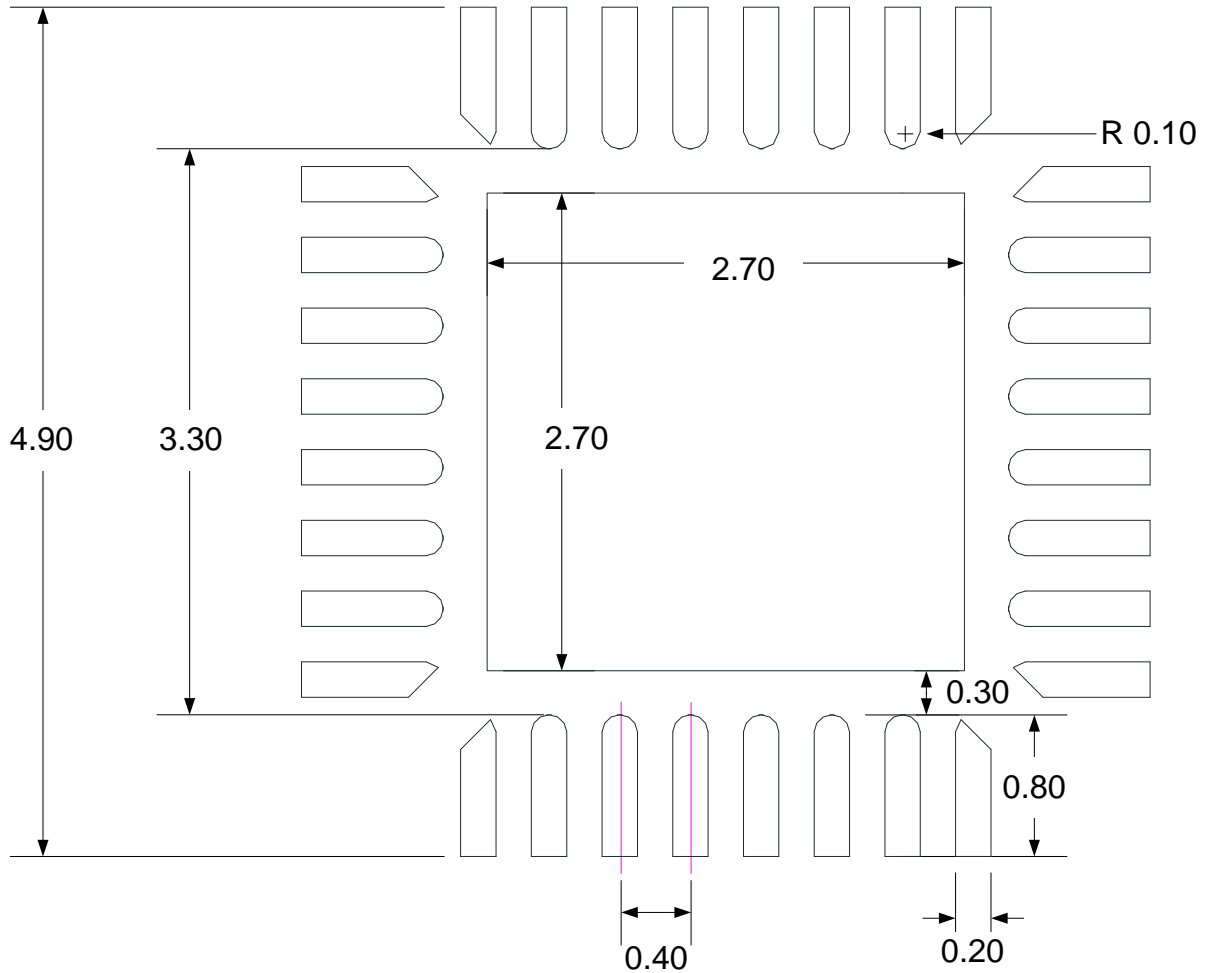


SYMBOLS	MIN	NOM	MAX
A	0.50	0.55	0.60
A1	0.00	0.02	0.05
A3	0.15 REF.		
b	0.15	0.20	0.25
D	3.90	4.00	4.10
E	3.90	4.00	4.10
D2	2.65	2.70	2.75
E2	2.65	2.70	2.75
L	0.25	0.30	0.35
e	0.40 BASIC		

Note:

1. All dimensions refer to JEDEC OUTLINE MO-220.
2. Do not include Mold Flash or Protrusions.
3. Unit: mm.
4. https://www.hycontek.com/hy_mcu/QFN_DFN_PCB.pdf

8.1.2. Land Pattern Design Recommendations



Note:

1. Publication IPC-7351 is recommended for alternate designs.
2. https://www.hycontek.com/wp-content/uploads/QFN_DFN_PCB.pdf
3. Unit: mm.

HY17P51

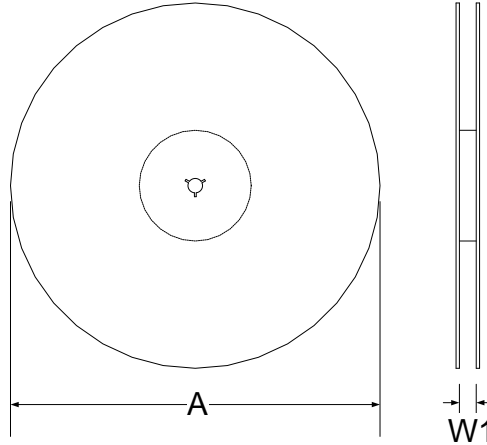
Embedded High Resolution $\Sigma\Delta$ ADC
8-Bit RISC-like Mixed Signal Microcontroller



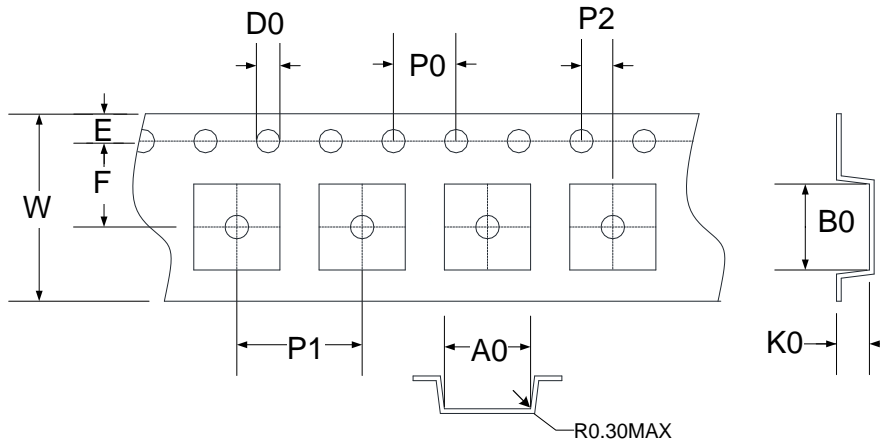
8.1.3. Tape & Reel Information

8.1.3.1. Reel Dimensions

Unit: mm



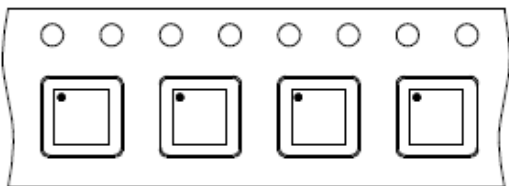
8.1.3.2. Carrier Tape Dimensions



SYMBOLS	Reel Dimensions		Carrier Tape Dimensions										
	A	W1	A0	B0	K0	P0	P1	P2	E	F	D0	W	
Spec.	330	12.5	4.35	4.35	1.10	4.00	8.00	2.00	1.75	5.50	1.50	12.00	
Tolerance	+6/-3	+1.5/-0	± 0.10	± 0.10	± 0.10	± 0.10	± 0.10	± 0.10	± 0.05	± 0.10	± 0.05	+0.1/-0	± 0.30

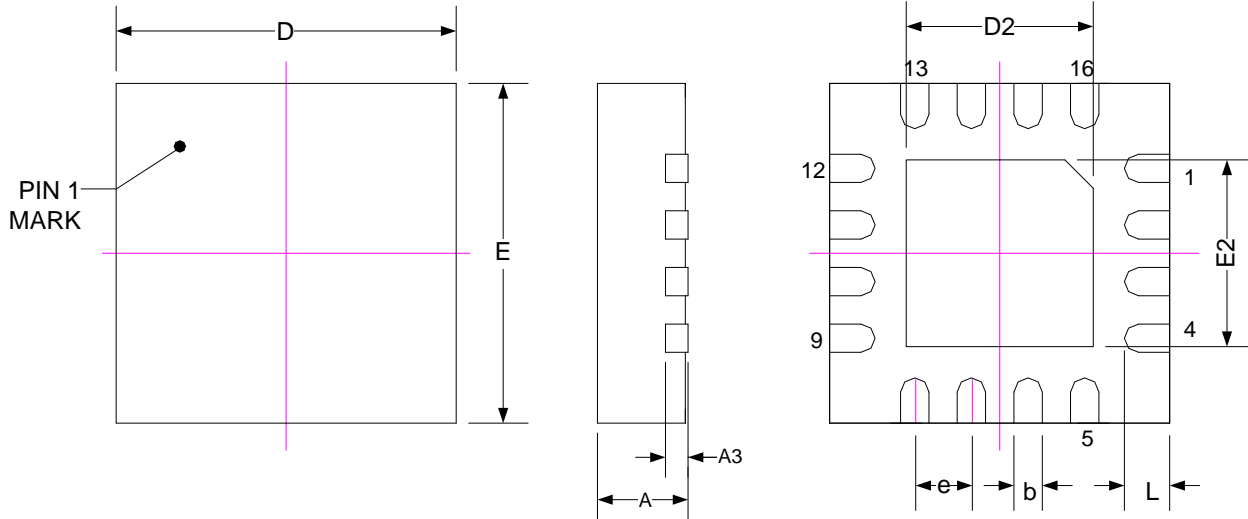
Note: 10 Sprocket hole pitch cumulative tolerance is $\pm 0.20mm$.

8.1.3.3. Pin1 direction



8.2. QFN16(N016)

8.2.1. Package Dimensions QFN16(3x3x0.75)

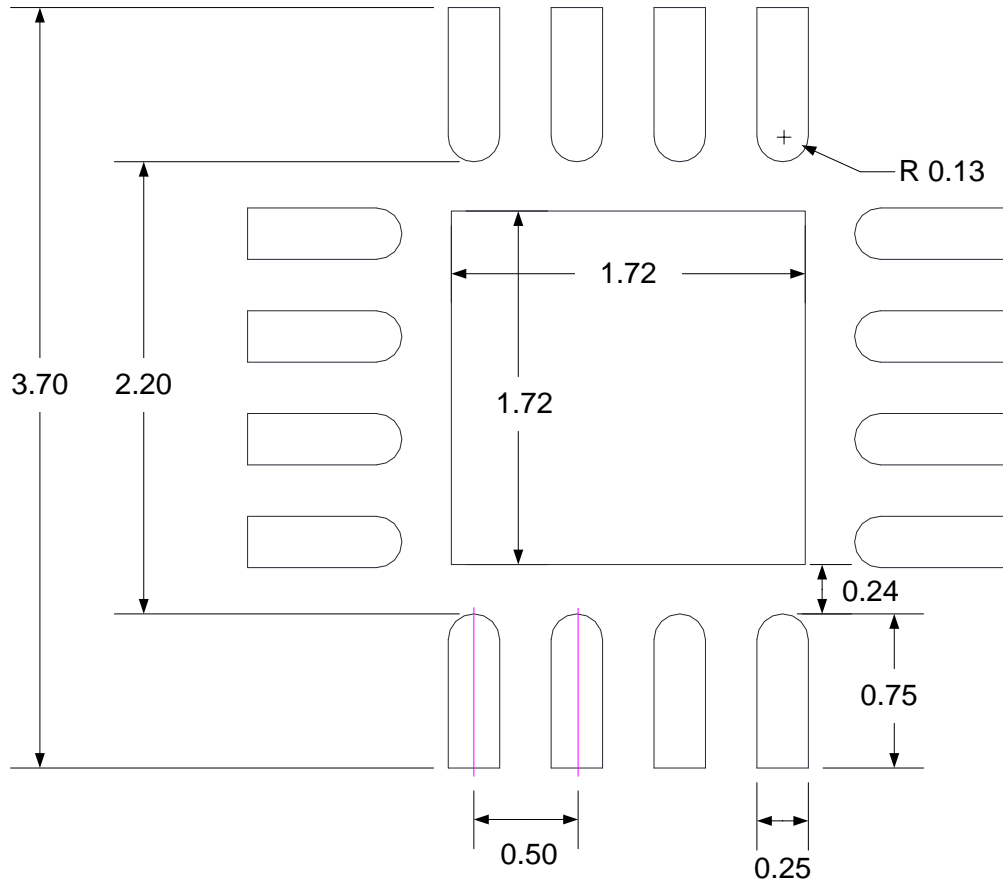


SYMBOLS	MIN	NOM	MAX
A	0.70	0.75	0.80
A3	0.203 REF.		
b	0.20	0.25	0.30
D	2.925	3.000	3.075
E	2.925	3.000	3.075
D2	1.625	1.725	1.825
E2	1.625	1.725	1.825
L	0.30	0.35	0.40
e	0.50 BASIC		

Note:

1. All dimensions refer to JEDEC OUTLINE MO-220.
2. Do not include Mold Flash or Protrusions.
3. Unit: mm.
4. https://www.hycontek.com/hy_mcu/QFN_DFN_PCB.pdf

8.2.2. Land Pattern Design Recommendations



Note:

1. Publication IPC-7351 is recommended for alternate designs.
2. https://www.hycontek.com/wp-content/uploads/QFN_DFN_PCB.pdf
3. Unit: mm.

HY17P51

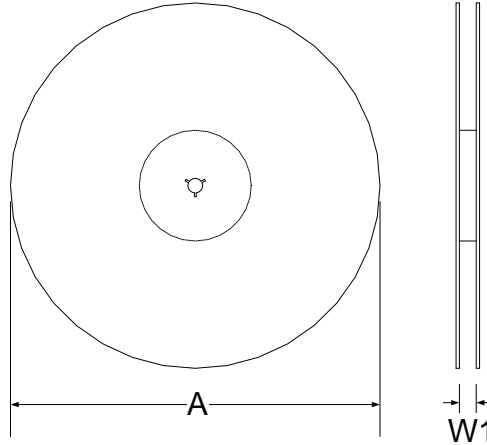
Embedded High Resolution $\Sigma\Delta$ ADC
8-Bit RISC-like Mixed Signal Microcontroller



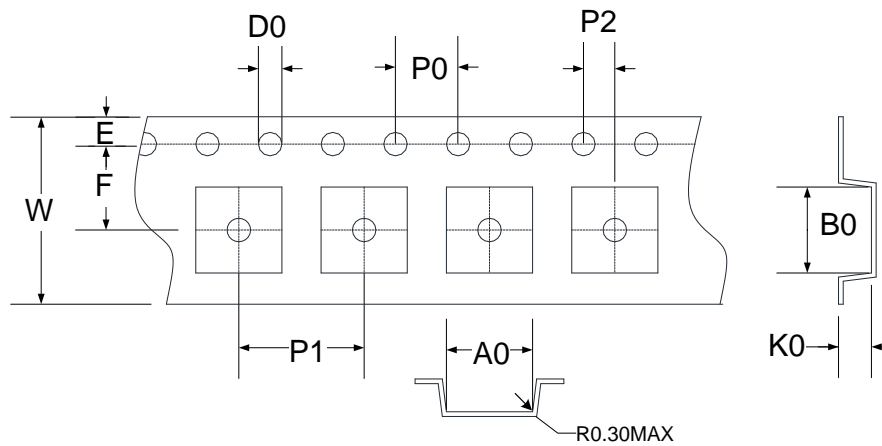
8.2.3. Tape & Reel Information

8.2.3.1. Reel Dimensions

Unit: mm



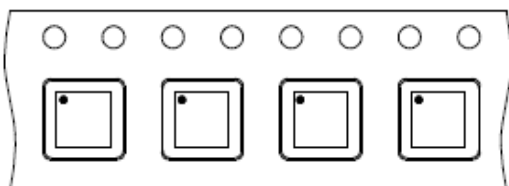
8.2.3.2. Carrier Tape Dimensions



SYMBOLS	Reel Dimensions		Carrier Tape Dimensions										
	A	W1	A0	B0	K0	P0	P1	P2	E	F	D0	W	
Spec.	330	12.5	3.30	3.30	1.10	4.00	8.00	2.00	1.75	5.50	1.50	12.00	
Tolerance	+6/-3	+1.5/-0	± 0.10	± 0.10	± 0.10	± 0.10	± 0.10	± 0.10	± 0.05	± 0.10	± 0.05	+0.1/-0	± 0.30

Note: 10 Sprocket hole pitch cumulative tolerance is $\pm 0.20mm$.

8.2.3.3. Pin1 direction



9. 修訂記錄

以下描述本文件差異較大的地方，而標點符號與字形的改變不在此描述範圍。

文件版次	頁次	日期	摘要
V01	All	2021/06/21	初版發行
V02	24~25	2021/08/30	修改暫存器列表，以符合實際情況
	45~51	2021/09/24	修改 QFN32 的包裝數量及封裝型式資訊
	26	2021/09/29	修正 RST Pin 電氣規格