HY17M28
Datasheet

8-Bit RISC-like Mixed Signal Microcontroller
Embedded 24-Bit ΣΔADC
Low Noise Amplifier
LED Driver

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注意：

1、 本說明書中的內容，隨著產品的改進，有可能不經過預告而更改。請客戶及時到本公司網站下載更新 http://www.hycontek.com。

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8、 本規格書中內容，未經本公司許可，嚴禁用於其他目的之轉載或複製。

1. 特點

- **8-Bit RISC-like 微控制器**
  - 具有 71 條高性能指令集 H08D
  - 硬體查表器
  - Power On/ Brown Out 1/ Brown Out 2
  - WDT/MCLR Reset
- **工作電壓與操作溫度範圍**
  - VDD = 1.9V ~ 5.5V 數位電路
  - VDDA = 2.4V ~ 5.5V 類比電路
  - - 40°C ~ 85°C 工作溫度
- **記憶體**
  - 8KW MTP 程式記憶體(燒錄次數 100 次)
  - 32 bytes EEPROM 資料記憶體(1.5K 次) Or 64 bytes EEPROM 資料記憶體(700 次)
  - 512bytes SRAM + 32/64bytes EEPROM
  - 8L Stack Level
- **24-Bit ΣΔADC 類比數位轉換器**
  - 最高取樣頻率達 1MHz
  - 超取樣頻率設置 64～65536
  - 支援輸入端緩衝器設計
  - 二/三階梳狀濾波器，轉換頻率 15.6Ksps
  - 信號放大 x1/4, x1/2, x1,x2,x4,x8,x16
  - 全差動輸入信號與測量範圍的零點調整
  - 低溫飄係數與內置絕對溫度傳感器
- **低功耗與低溫飄係數電源系統**
  - VDDA 線性穩壓電源
    - 供應類比電路或外部傳感器電壓源
    - 採可外灌輸入電壓設計
    - 可設置穩壓輸出 2.4V/2.6V/2.9V/3.3V /3.6V /4.0V/4.5V/5.0V
  - REFO 參考電壓源
    - 可設置輸出 1.2V
- **Low Noise PGA Amplifier**
  - 內建單端放大電路，信號放大 x10, x20, x40
- **通訊介面**
  - I^2C、EUART、2 線式 ICE 與燒錄引腳
- **計時器**
  - Watch Dog
  - 8-bit Timer A (TMA1)
  - 16-bit Timer B (TMB)
    - 16-Bit PWM or 8-bit+8-bit PWM
- **8 個 GPIO 支援定電流控制線路**
  - Source current 2~15mA 定電流驅動
  - Sink current 80mA
- **2 Touch Key support**
- **低功耗特性**
  - 休眠模式 0.1uA@3.0V
  - 待機模式 0.5uA@3.0V
  - 待機模式下喚醒,可支援 HAO 快速啟動功能,滿足 30us 內完成頻率由低速切成高速需求
- **Bootloader 更新功能**
  - 支援 Bootloader 線上更新(ISP)功能
- **工作頻率**
  - 內置±2%高精度 HAO 震盪器(燒錄器校正後)
  - 內置低功耗 LPO 震盪器 14.5KHz
  - 外接石英震盪器 32768Hz ~ 16MHz
- **封裝**
  - SSOP20、SSOP28、QFN32
- **應用領域**
  - 溫度感測、紅外線測溫

功能列表

Model No.	VDD (V)	Internal Clock (Hz)	System Clock (Hz)	Program Memory (word)	SRAM (byte)	Built-In EEPROM (byte)	ADC ENOB (bit x ch)	Sample Rate (sps)	I/O	Timer (bit x ch)	PWM (bit x ch)	Serial Interface (I/F x ch)	Package
HY17M28	1.9~5.5	14.5K 1.843M 4.147M 8.755M 15.667M	14.5K~16M	8K	512	32/64	20-bit x7	8~15.6K	15xIO	8-bit x 1 16-bit x 1	8-bit x 2 16-bit x 1	EUART x 1 I^2C x 1	SSOP20
							20-bit x11		19xIO				SSOP28
							20-bit x14		23xIO				QFN32

2. 引腳與定義

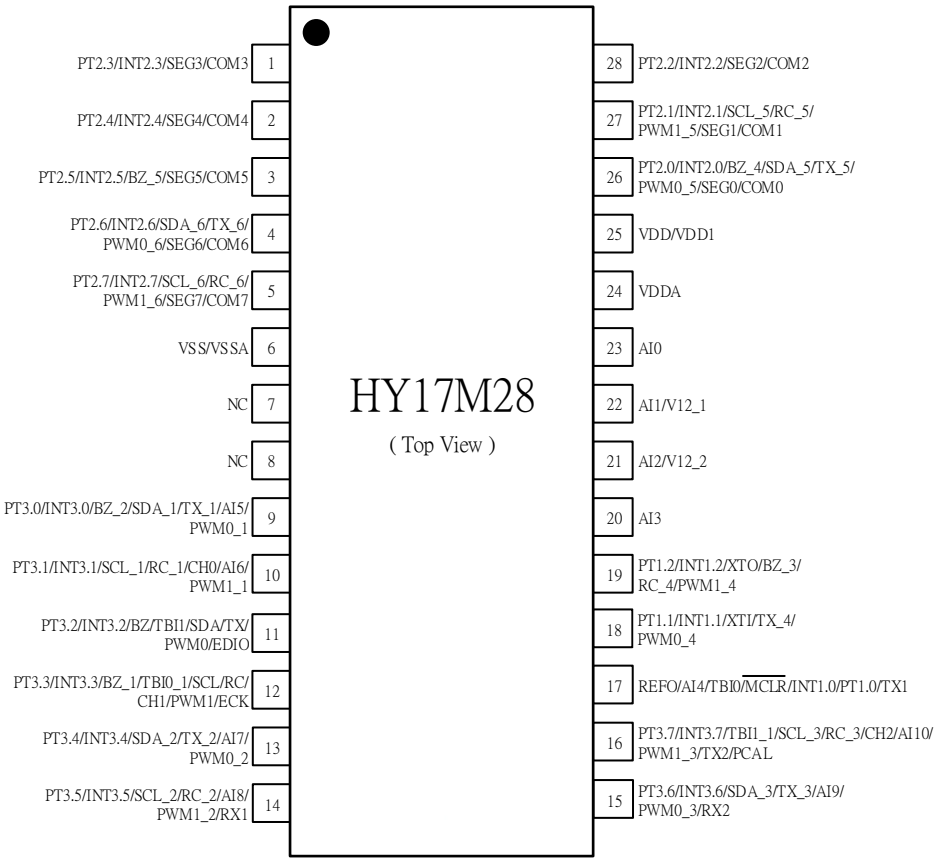


圖 2-1 引腳圖 SSOP28 (209mil)

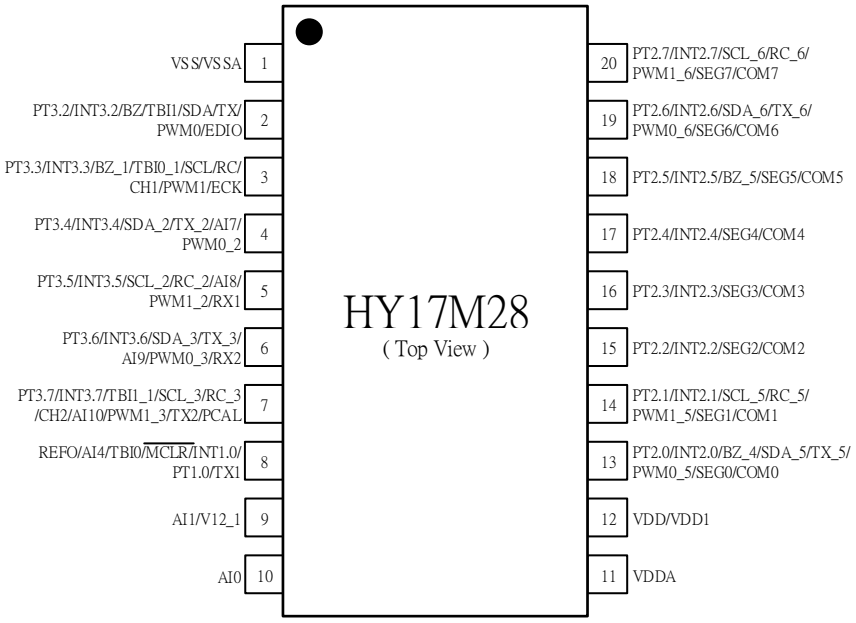


圖 2-2 引腳圖 SSOP20 (150mil)

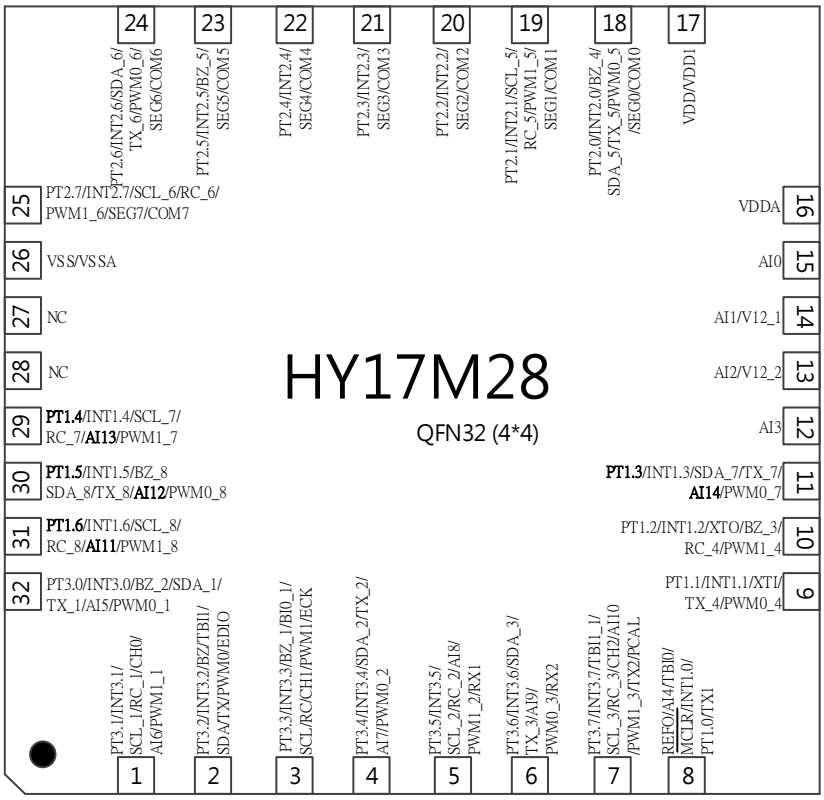


圖 2-3 引腳圖 QFN32 (4*4)

2.1. HY17M28 引腳定義說明

封裝 / 腳位			設計			描述
SSOP20	SSOP28	QFN32		型式	緩衝	
12	25	17	VDD	P	P	晶片工作電壓源接正端引腳, 需外接 10uF 電容至 VSS.
			VDD1	P	P	PT2 PORT 電壓源(short to VDD).
11	24	16	VDDA	P	P	LDO 線性穩壓電源輸出引腳,若啟動輸出時需外接 1uF 電容至 VSS.
1	6	26	VSS	P	P	晶片工作電壓源接地端引腳
			VSSA	P	P	晶片類比電壓源接地端引腳
10	23	15	AI0	A	A	類比輸入通道
9	22	14	AI1/V12_1*2			
			AI1	A	A	類比輸入通道
			V12_1*2	P	P	1.2V 參考電壓
-	21	13	AI2/V12_2*2			
			AI2	A	A	類比輸入通道
			V12_2*2	P	P	1.2V 參考電壓
-	20	12	AI3	A	A	類比輸入通道
8	17	8	PT1.0/INT1.0/MCLR/TBI0/REFO/TX1			
			PT1.0	I/O	S/C	數位輸入/輸出引腳
			INT1.0	I	S	外部中斷源
			MCLR	I	S	低電位有效，帶內部上拉電阻
			TBI0	I	S	TimerB CPI 輸入選擇源
			REFO	P	P	參考電壓引腳
			TX1	O	A	Touch Key TX1 引腳
-	18	9	PT1.1/INT1.1/XTI/TX_4*2/PWM0_4*2			
			PT1.1	I/O	S/C	數位輸入/輸出引腳
			INT1.1	I	S	外部中斷源
			XTI	A	A	外接震盪器輸入端
			TX_4*2	O	C	UART 通訊傳送信號
			PWM0_4*2	O	C	PWM0 輸出
-	19	10	PT1.2/INT1.2/XTO/BZ_3/RC_4*2/PWM1_4*2			
			PT1.2	I/O	S/C	數位輸入/輸出引腳
			INT1.2	I	S	外部中斷源
			XTO	A	A	外接震盪器輸出端
			RC_4*2	I	S	UART 通訊接收信號
			PWM1_4*2	O	C	PWM1 輸出

封裝 / 腳位			設計			描述
SSOP20	SSOP28	QFN32		型式	緩衝	
-	-	11	PT1.3/INT1.3/SDA_7*2/TX_7*2/AI14/PWM0_7*2			
			PT1.3	I/O	S/C	數位輸入/輸出引腳
			INT1.3	I	S	外部中斷源
			SDA_7*2	I/O	S/C	I²C 通訊數據信號
			TX_7*2	O	C	UART 通訊傳送信號
			AI14	A	A	類比輸入通道
			PWM0_7*2	O	C	PWM0 輸出
-	-	29	PT1.4/INT1.4/SCL_7*2/RC_7*2/AI13/PWM1_7*2			
			PT1.4	I/O	S/C	數位輸入/輸出引腳
			INT1.4	I	S	外部中斷源
			SCL_7*2	I/O	S/C	I²C 通訊時鐘信號
			RC_7*2	I	S	UART 通訊接收信號
			AI13	A	A	類比輸入通道
			PWM1_7*2	O	C	PWM1 輸出
-	-	30	PT1.5/INT1.5/BZ_8/SDA_8*2/TX_8*2/AI12/PWM0_8*2			
			PT1.5	I/O	S/C	數位輸入/輸出引腳
			INT1.5	I	S	外部中斷源
			BZ_8*2	O	C	蜂鳴器輸出端
			SDA_8*2	I/O	S/C	I²C 通訊數據信號
			TX_8*2	O	C	UART 通訊傳送信號
			AI12	A	A	類比輸入通道
			PWM0_8*2	O	C	PWM0 輸出
-	-	31	PT1.6/INT1.6/SCL_8*2/RC_8*2/AI11/PWM1_8*2			
			PT1.6	I/O	S/C	數位輸入/輸出引腳
			INT1.6	I	S	外部中斷源
			SCL_8*2	I/O	S/C	I²C 通訊時鐘信號
			RC_8*2	I	S	UART 通訊接收信號
			AI11	A	A	類比輸入通道
			PWM1_8*2	O	C	PWM1 輸出
-	9	32	PT3.0/INT3.0/BZ_2*2/SDA_1*2/TX_1*2/AI5/PWM0_1*2			
			PT3.0	I/O	S/C	數位輸入 / 輸出引腳
			INT3.0	I	S	外部中斷源
			BZ_2*2	O	C	蜂鳴器輸出端
			SDA_1*2	I/O	S/C	I²C 通訊數據信號

封裝 / 腳位			設計			描述
SSOP20	SSOP28	QFN32		型式	緩衝	
			TX_1*2	O	C	UART 通訊傳送信號
			AI5	A	A	類比輸入通道
			PWM0_1*2	O	C	PWM0 輸出
-	10	1	PT3.1/INT3.1/SCL_1*2/RC_1*2/CH0/AI6/PWM1_1*2			
			PT3.1	I/O	S/C	數位輸入 / 輸出引腳
			INT3.1	I	S	外部中斷源
			SCL_1*2	I/O	S/C	I²C 通訊時鐘信號
			RC_1*2	I	S	UART 通訊接收信號
			CH0	A	A	比較器輸入通道
			AI6	A	A	類比輸入通道
			PWM1_1*2	O	C	PWM1 輸出
2	11	2	PT3.2/INT3.2/BZ/TBI1/SDA/TX/PWM0/EDIO*1			
			PT3.2	I/O	S/C	數位輸入 / 輸出引腳
			INT3.2	I	S	外部中斷源
			BZ	O	C	蜂鳴器輸出端
			TBI1	I	S	TimerB CPI 輸入選擇源
			SDA	I/O	S/C	I²C 通訊數據信號
			TX	O	C	UART 通訊傳送信號
			PWM0	O	C	PWM0 輸出
			EDIO*1	I/O	S/C	仿真及燒錄之通訊數據 EDIO
3	12	3	PT3.3/INT3.3/BZ_1*2/TBI0_1*2/SCL/RC/CH1/PWM1/ECK*1			
			PT3.3	I/O	S/C	數位輸入 / 輸出引腳
			INT3.3	I	S	外部中斷源
			BZ_1*2	O	C	蜂鳴器輸出端
			TBI0_1*2	I	S	TimerB CPI 輸入選擇源
			SCL	I/O	S/C	I²C 通訊時鐘信號
			RC	I	S	UART 通訊接收信號
			CH1	A	A	比較器輸入通道
			PWM1	O	C	PWM1 輸出
			ECK*1	I	S	仿真及燒錄之通訊時鐘腳 ECK
4	13	4	PT3.4/INT3.4/SDA_2*2/TX_2*2/AI7/PWM0_2*2			
			PT3.4	I/O	S/C	數位輸入 / 輸出引腳
			INT3.4	I	S	外部中斷源
			SDA_2*2	I/O	S/C	I²C 通訊數據信號

封裝 / 腳位			設計			描述
SSOP20	SSOP28	QFN32		型式	緩衝	
			TX_2*2	O	C	UART 通訊傳送信號
			AI7	A	A	類比輸入通道
			PWM0_2*2	O	C	PWM0 輸出
5	14	5	PT3.5/INT3.5/SCL_2*2/RC_2*2/AI8/PWM1_2*2/RX1			
			PT3.5	I/O	S/C	數位輸入 / 輸出引腳
			INT3.5	I	S	外部中斷源
			SCL_2*2	I/O	S/C	I²C 通訊時鐘信號
			RC_2*2	I	S	UART 通訊接收信號
			AI8	A	A	類比輸入通道
			PWM1_2*2	O	C	PWM1 輸出
			RX1	A	A	Touch Key RX1
6	15	6	PT3.6/INT3.6/SDA_3*2/TX_3*2/AI9/PWM0_3*2/RX2			
			PT3.6	I/O	S/C	數位輸入 / 輸出引腳
			INT3.6	I	S	外部中斷源
			SDA_3*2	I/O	S/C	I²C 通訊數據信號
			TX_3*2	O	C	UART 通訊傳送信號
			AI9	A	A	類比輸入通道
			PWM0_3*2	O	C	PWM0 輸出
			RX2	A	A	Touch Key RX2
7	16	7	PT3.7/INT3.7/TBI1_1*2/SCL_3*2/RC_3*2/CH2/AI10/PWM1_3*2/TX2/PCAL			
			PT3.7	I/O	S/C	數位輸入 / 輸出引腳
			INT3.7	I	S	外部中斷源
			TBI1_1*2	I	S	TimerB CPI 輸入選擇源
			SCL_3*2	I/O	S/C	I²C 通訊時鐘信號
			RC_3*2	I	S	UART 通訊接收信號
			CH2	A	A	比較器輸入通道
			AI10	A	A	類比輸入通道
			PWM1_3*2	O	C	PWM1 輸出
			TX2	O	A	Touch Key TX2
			PCAL*1	O	C	燒錄用之頻率校正輸出引腳
13	26	18	PT2.0/INT2.0/BZ_4*2/SDA_5*2/TX_5*2/PWM0_5*2/SEG0/COM0			
			PT2.0	I/O	S/C	數位輸入 / 輸出引腳
			INT2.0	I	S	外部中斷源
			BZ_4*2	O	C	蜂鳴器輸出端

封裝 / 腳位			設計			描述
SSOP20	SSOP28	QFN32		型式	緩衝	
			SDA_5*2	I/O	S/C	I²C 通訊數據信號
			TX_5*2	O	C	UART 通訊傳送信號
			PWM0_5*2	O	C	PWM0 輸出
			SEG0	O	C	Constant current source port, SEG0
			COM0	O	C	Sink current port, COM0
14	27	19	PT2.1/INT2.1/SCL_5*2/RC_5*2/PWM1_5*2/SEG1/COM1			
			PT2.1	I/O	S/C	數位輸入/輸出引腳
			INT2.1	I	S	外部中斷源
			SCL_5*2	I/O	S/C	I²C 通訊時鐘信號
			RC_5*2	I	S	UART 通訊接收信號
			PWM1_5*2	O	C	PWM1 輸出
			SEG1	O	C	Constant current source port, SEG1
			COM1	O	C	Sink current port, COM1
15	28	20	PT2.2/INT2.2/SEG2/COM2			
			PT2.2	I/O	S/C	數位輸入/輸出引腳
			INT2.2	I	S	外部中斷源
			SEG2	O	C	Constant current source port, SEG2
			COM2	O	C	Sink current port, COM2
16	1	21	PT2.3/INT2.3/SEG3/COM3			
			PT2.3	I/O	S/C	數位輸入/輸出引腳
			INT2.3	I	S	外部中斷源
			SEG3	O	C	Constant current source port, SEG3
			COM3	O	C	Sink current port, COM3
17	2	22	PT2.4/INT2.4/SEG4/COM4			
			PT2.4	I/O	S/C	數位輸入/輸出引腳
			INT2.4	I	S	外部中斷源
			SEG4	O	C	Constant current source port, SEG4
			COM4	O	C	Sink current port, COM4
18	3	23	PT2.5/INT2.5/BZ_5*2/SEG5/COM5			
			PT2.5	I/O	S/C	數位輸入 / 輸出引腳
			INT2.5	I	S	外部中斷源
			BZ_5*2	O	C	蜂鳴器輸出端
			SEG5	O	C	Constant current source port, SEG5
			COM5	O	C	Sink current port, COM5
19	4	24	PT2.6/INT2.6/SDA_6*2/TX_6*2/PWM0_6*2/SEG6/COM6			

封裝 / 腳位			設計			描述
SSOP20	SSOP28	QFN32		型式	緩衝	
			PT2.6	I/O	S/C	數位輸入 / 輸出引腳
			INT2.6	I	S	外部中斷源
			SDA_6*2	I/O	S/C	I²C 通訊數據信號
			TX_6*2	O	C	UART 通訊傳送信號
			PWM0_6*2	O	C	PWM0 輸出
			SEG6	O	C	Constant current source port, SEG6
			COM6	O	C	Sink current port, COM6
20	5	25	PT2.7/INT2.7/SCL_6*2/RC_6*2/PWM1_6*2/SEG7/COM7			
			PT2.7	I/O	S/C	數位輸入/輸出引腳
			INT2.7	I	S	外部中斷源
			SCL_6*2	I/O	S/C	I²C 通訊時鐘信號
			RC_6*2	I	S	UART 通訊接收信號
			PWM1_6*2	O	C	PWM1 輸出
			SEG7	O	C	Constant current source port, SEG7
			COM7	O	C	Sink current port, COM7
-	8	28	NC	I/O	S/C	不連接(Not connected), 該腳請保持空接
-	7	27	NC	I	S	不連接(Not connected), 該腳請保持空接

1 仿真 ICE 除錯、模擬與讀/寫晶片的通訊引腳，該模式下 GPIO 複用功能無法使用。

2 經由晶片內部設置，可規劃複用引腳功能在該引腳輸出或輸入。*表示為複用選擇的腳位。

表 2-1 引腳編號與說明

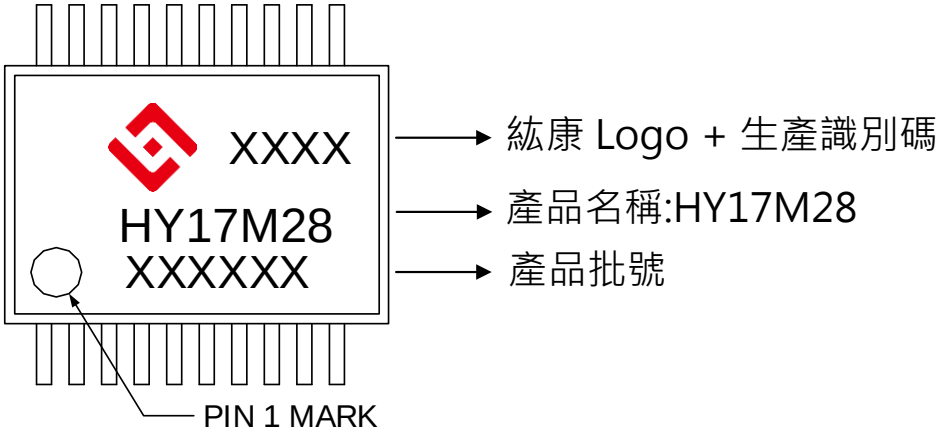
2.2. 復用引腳定義說明

QFN32	SSOP28	SSOP20	PAD Name	I/O Type	INT	Internal Pull high	Special Function	Buzzer	Timer B	I²C	UART	Comparator	Analog	Touch Key	PWM
17	25	12	**VDD**	P											
			VDD1	P											
16	24	11	**VDDA**	P											
26	6	1	**VSS**	P											
15	23	10	**AI0**	AIO									AI0		
14	22	9	**AI1**	AIO			V12_1						AI1		
13	21	NC	**AI2**	AIO			V12_2						AI2		
12	20	NC	**AI3**	AI									AI3		
8	17	8	**PT1.0**	DAI/O	INT1.0	PU1.0	MCLR, REFO,		TBI0					TX1	
9	18	NC	**PT1.1**	DAI/O	INT1.1	PU1.1	XTI				TX_4				PWM0_4
10	19	NC	**PT1.2**	DAI/O	INT1.2	PU1.2	XTO	BZ_3			RC_4				PWM1_4
11	NC	NC	**PT1.3**	DAI/O	INT1.3	PU1.3				SDA_7	TX_7		**AI14**		PWM0_7
29	NC	NC	**PT1.4**	DAI/O	INT1.4	PU1.4				SCL_7	RC_7		**AI13**		PWM1_7
30	NC	NC	**PT1.5**	DAI/O	INT1.5	PU1.5		BZ_8		SDA_8	TX_8		**AI12**		PWM0_8
31	NC	NC	**PT1.6**	DAI/O	INT1.6	PU1.6				SCL_8	RC_8		**AI11**		PWM1_8
18	26	13	**PT2.0**	DI/O	INT2.0	PU2.0	COM0/SEG0	BZ_4		SDA_5	TX_5				PWM0_5
19	27	14	**PT2.1**	DI/O	INT2.1	PU2.1	COM1/SEG1			SCL_5	RC_5				PWM1_5
20	28	15	**PT2.2**	DI/O	INT2.2	PU2.2	COM2/SEG2								
21	1	16	**PT2.3**	DI/O	INT2.3	PU2.3	COM3/SEG3								
22	2	17	**PT2.4**	DI/O	INT2.4	PU2.4	COM4/SEG4								
23	3	18	**PT2.5**	DI/O	INT2.5	PU2.5	COM5/SEG5	BZ_5							
24	4	19	**PT2.6**	DI/O	INT2.6	PU2.6	COM6/SEG6			SDA_6	TX_6				PWM0_6
25	5	20	**PT2.7**	DI/O	INT2.7	PU2.7	COM7/SEG7			SCL_6	RC_6				PWM1_6
32	9	NC	**PT3.0**	DAI/O	INT3.0	PU3.0		BZ_2		SDA_1	TX_1		AI5		PWM0_1
1	10	NC	**PT3.1**	DAI/O	INT3.1	PU3.1				SCL_1	RC_1	CH0	AI6		PWM1_1
2	11	2	**PT3.2**	DAI/O	INT3.2	PU3.2	EDIO	BZ	TBI1	SDA	TX				PWM0
3	12	3	**PT3.3**	DAI/O	INT3.3	PU3.3	ECK	BZ_1	TBI0_1	SCL	RC	CH1			PWM1
4	13	4	**PT3.4**	DAI/O	INT3.4	PU3.4				SDA_2	TX_2		AI7		PWM0_2
5	14	5	**PT3.5**	DAI/O	INT3.5	PU3.5				SCL_2	RC_2		AI8	RX1	PWM1_2
6	15	6	**PT3.6**	DAI/O	INT3.6	PU3.6				SDA_3	TX_3		AI9	RX2	PWM0_3
7	16	7	**PT3.7**	DAI/O	INT3.7	PU3.7	**PCAL**		TBI1_1	SCL_3	RC_3	CH2	AI10	TX2	PWM1_3
27	7	NC	**NC**	DI/O											
28	8	NC	**NC**	DI/O											

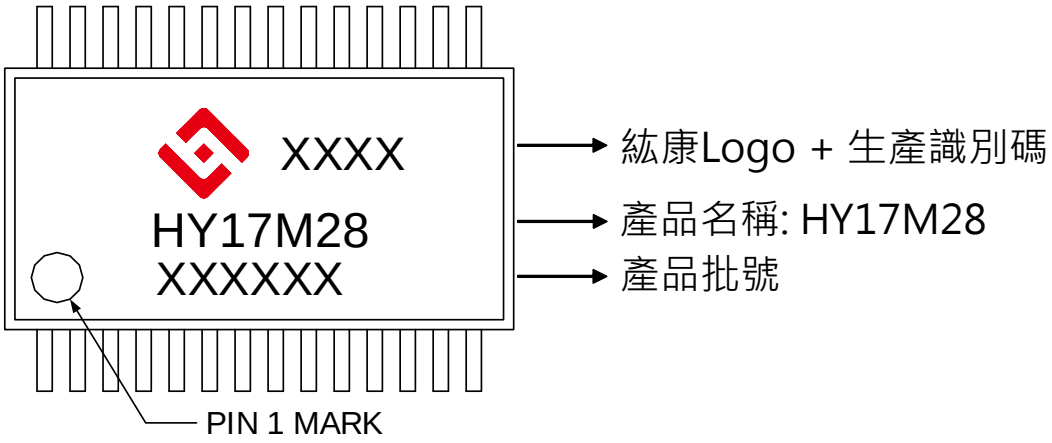
表 2-2 引腳編號與說明

2.3. 封裝片標記信息

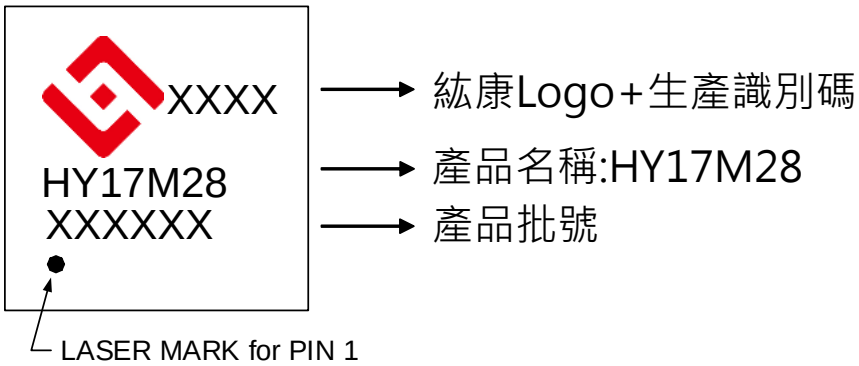
2.3.1. SSOP20 封裝片標記信息



2.3.2. SSOP28 封裝片標記信息



2.3.3. QFN32(4x4)封裝片標記信息



3. 應用參考電路

3.1. 雙通道紅外測溫 LED 顯示應用

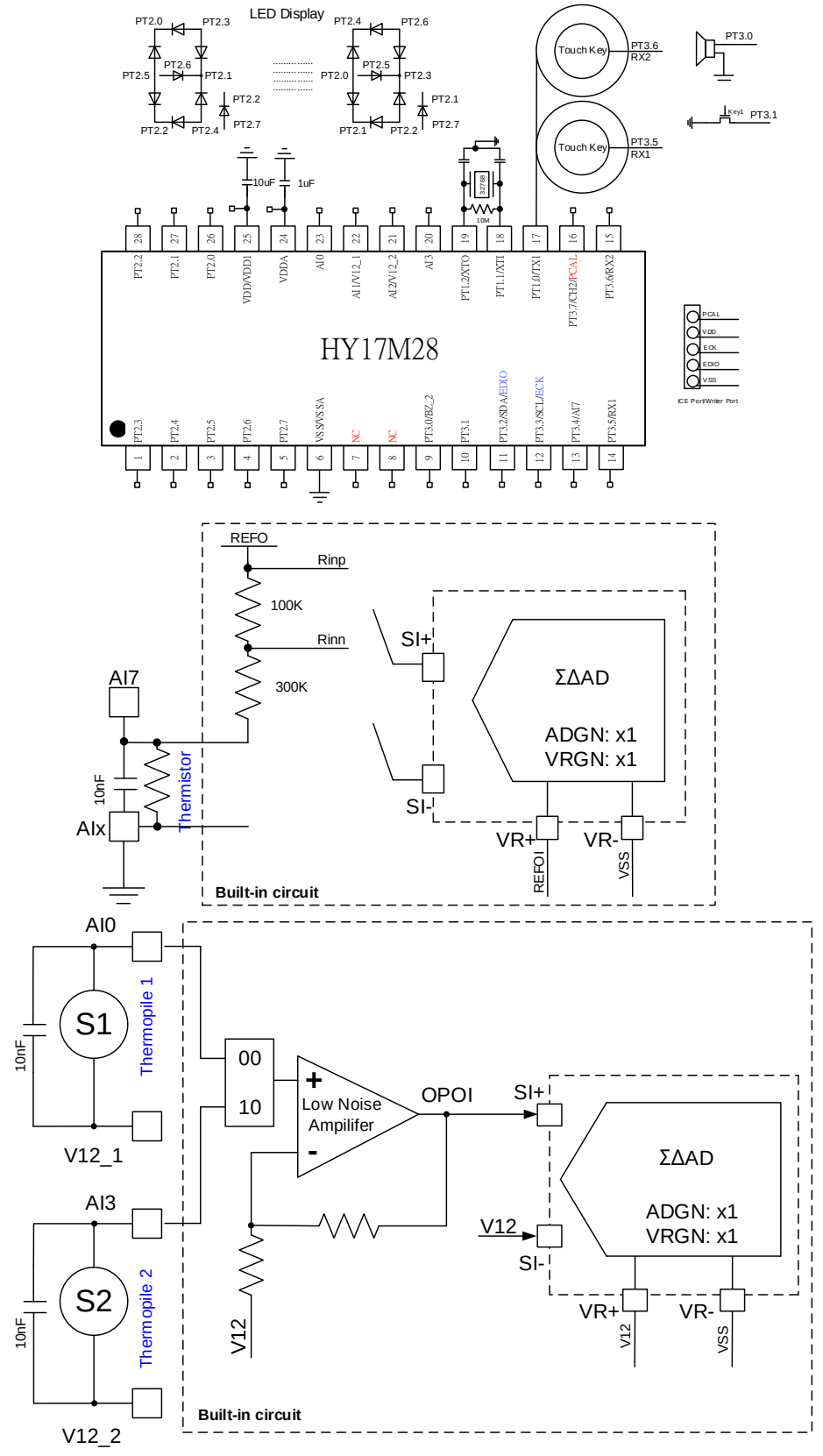


圖 3-1 雙通道紅外測溫應用參考電路

4. 功能概述

4.1. 內部方塊圖

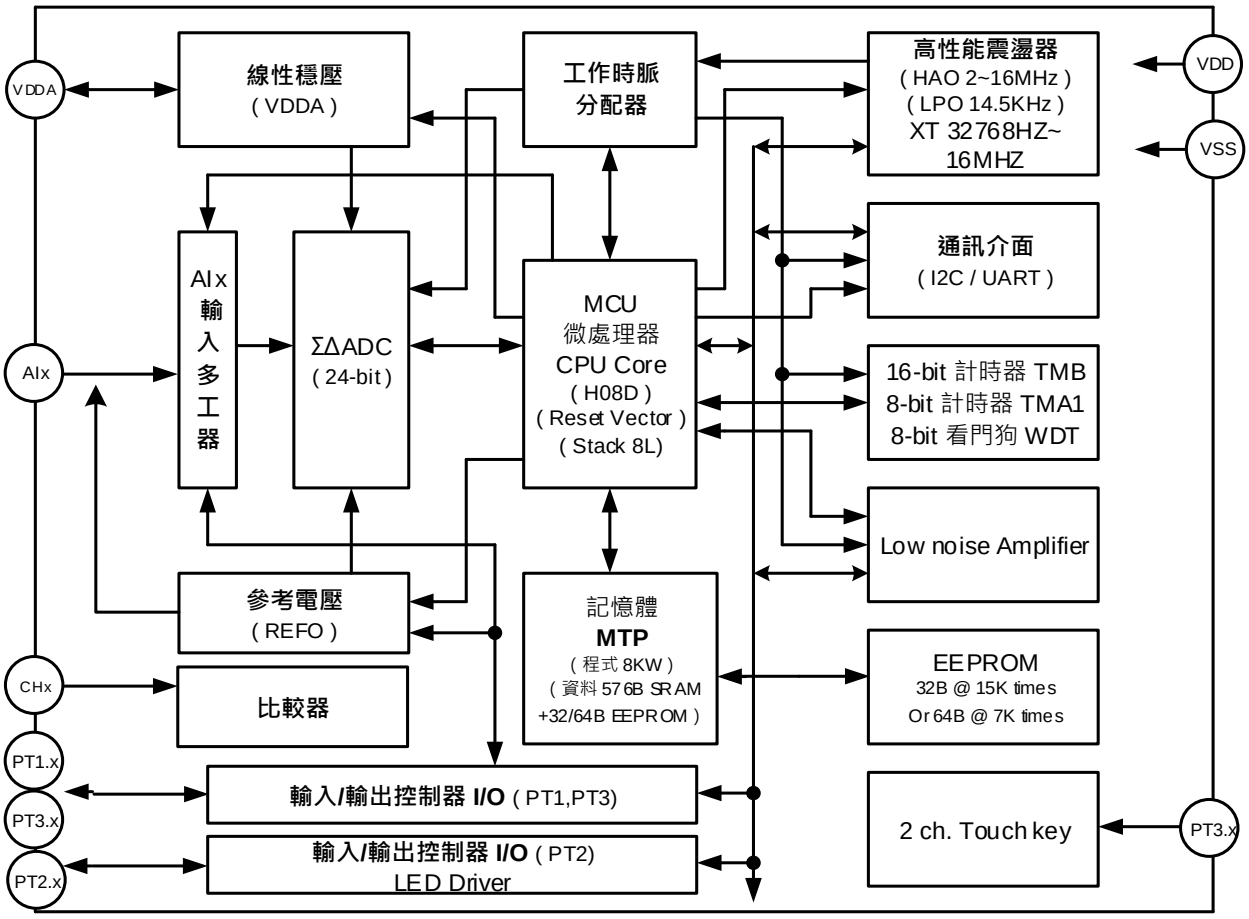


圖 4-1 內部方塊圖

4.2. 相關說明與支援文件

晶片功能相關使用說明書

DS-HY17M28	HY17M28 規格說明書
UG-HY17M28	HY17M28 使用說明書
APD-CORE002	H08A, H08C, H08D 組合語言指令集說明書
APD-HYIDE016	H08C CIDE 軟體使用說明書

開發工具相關使用說明書

APD-HY17MIDE001	HY17M Aseies Assembly IDE 軟體使用說明書
APD-HY17MIDE012	HY17M28 Series IDE 硬體使用說明書

產品生產相關使用說明書

APD-HY17MIDE0xx	HY17M28 生產線專用燒錄器說明書

4.3. Clock System

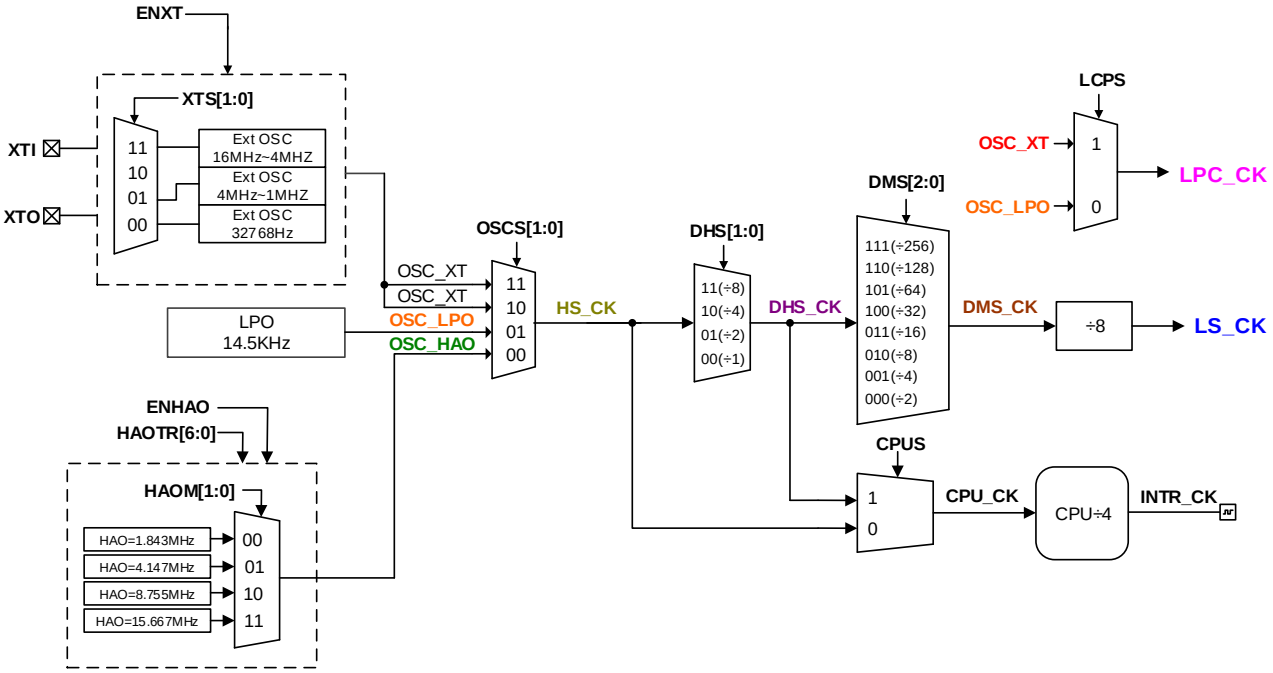


圖 4-2 Clock System(一)

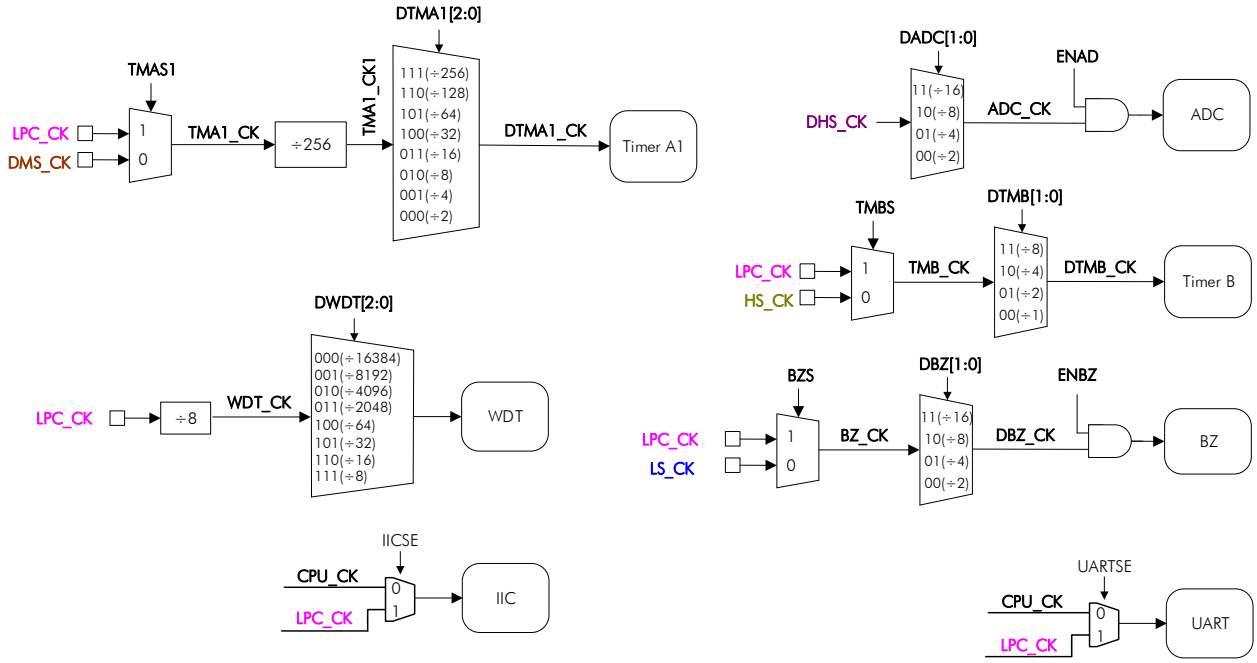


圖 4-3 Clock System(二)

4.4. GPIO PT1~PT3 System

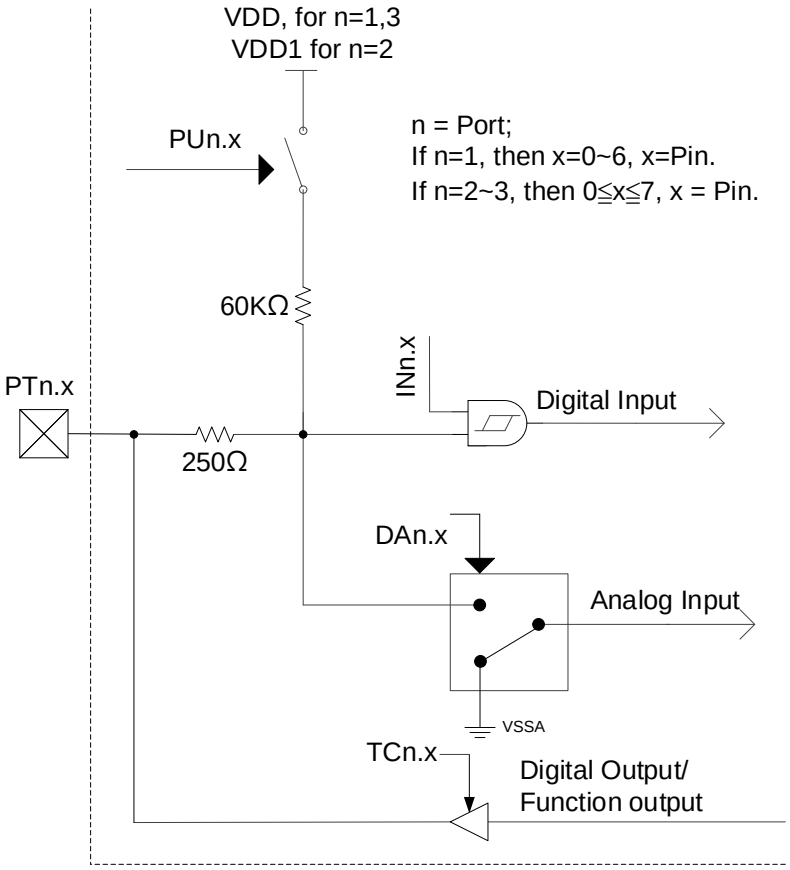


圖 4-4 GPIO PT1 ~ PT3 System

4.5. Reset System

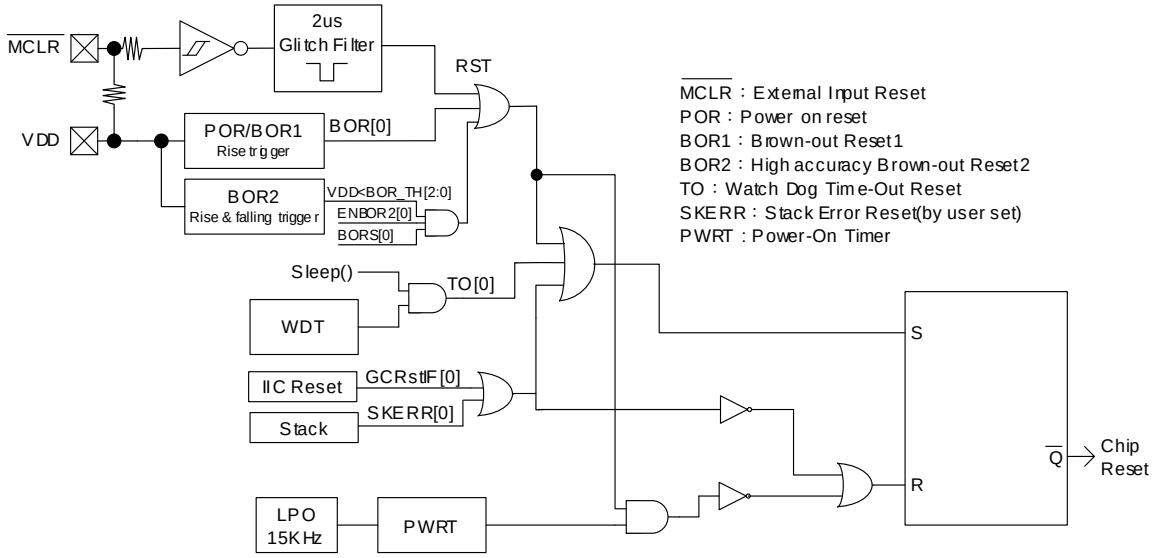


圖 4-5 Reset

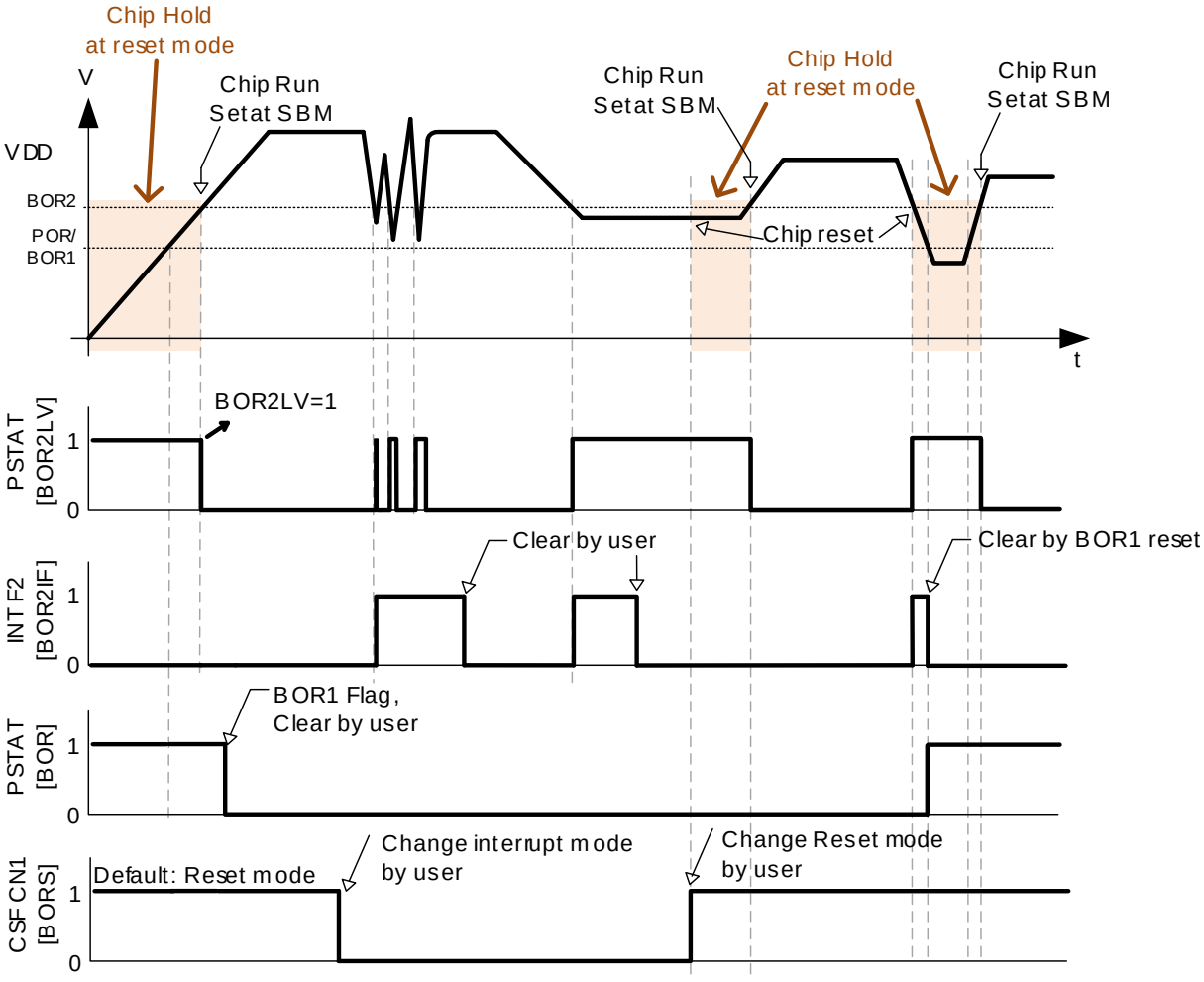


圖 4-6 BOR1 and BOR2 Chart

4.6. Power System

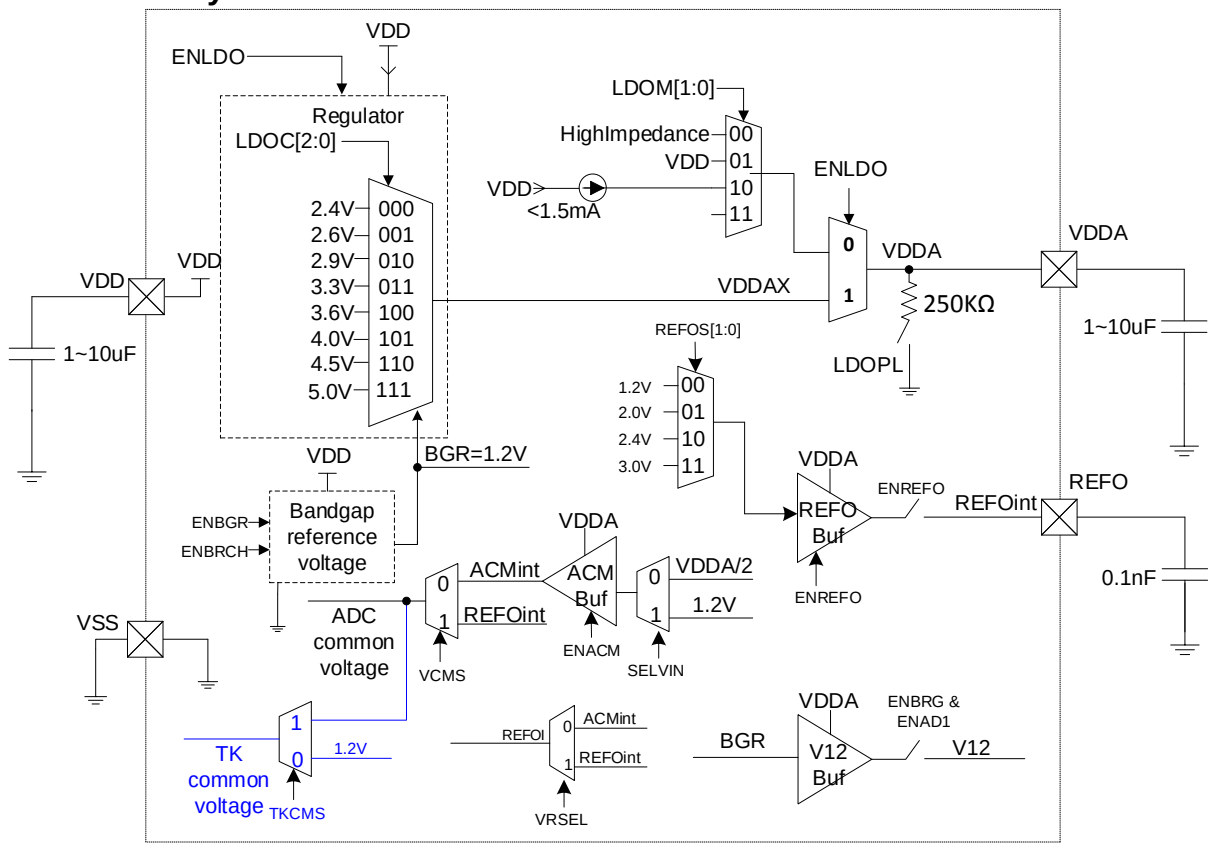


圖 4-7 Power System

4.7. ADC Network

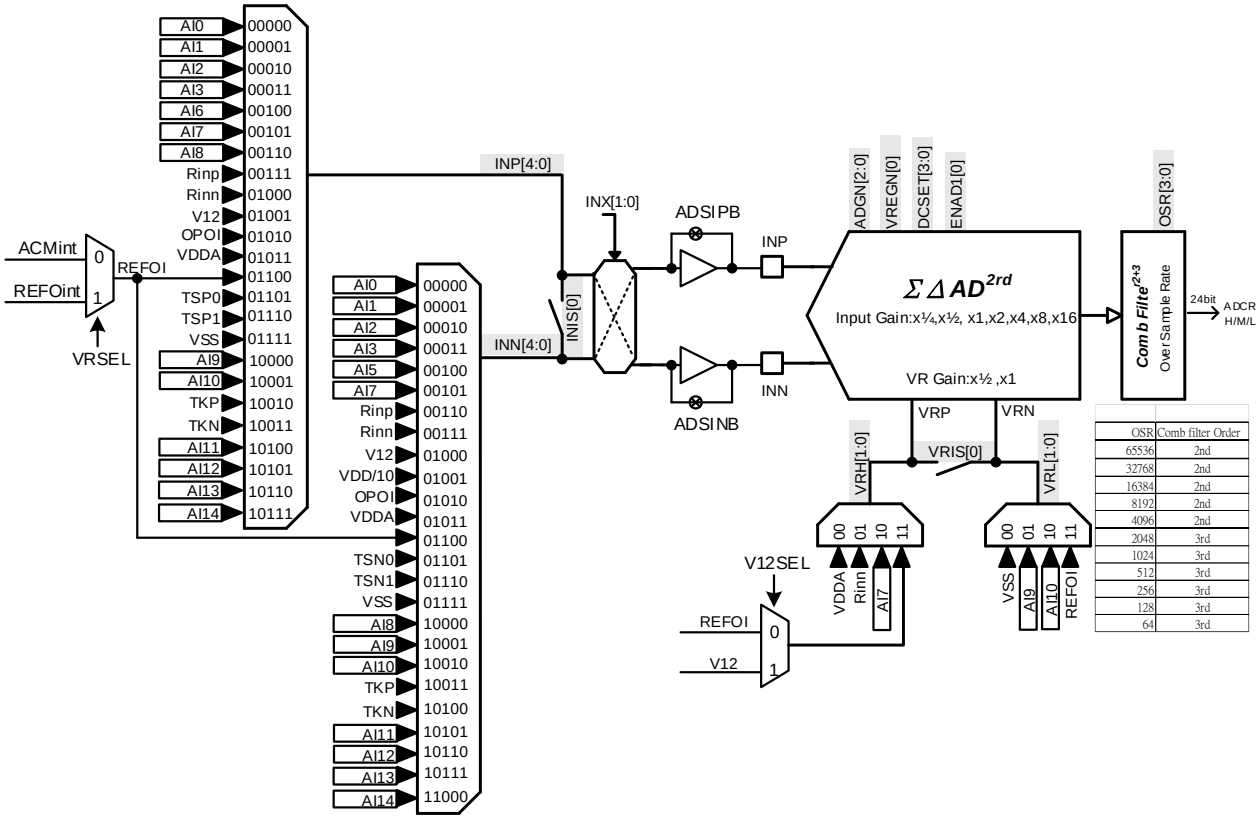


圖 4-8 ADC Network

4.8. Low Noise PGA Network

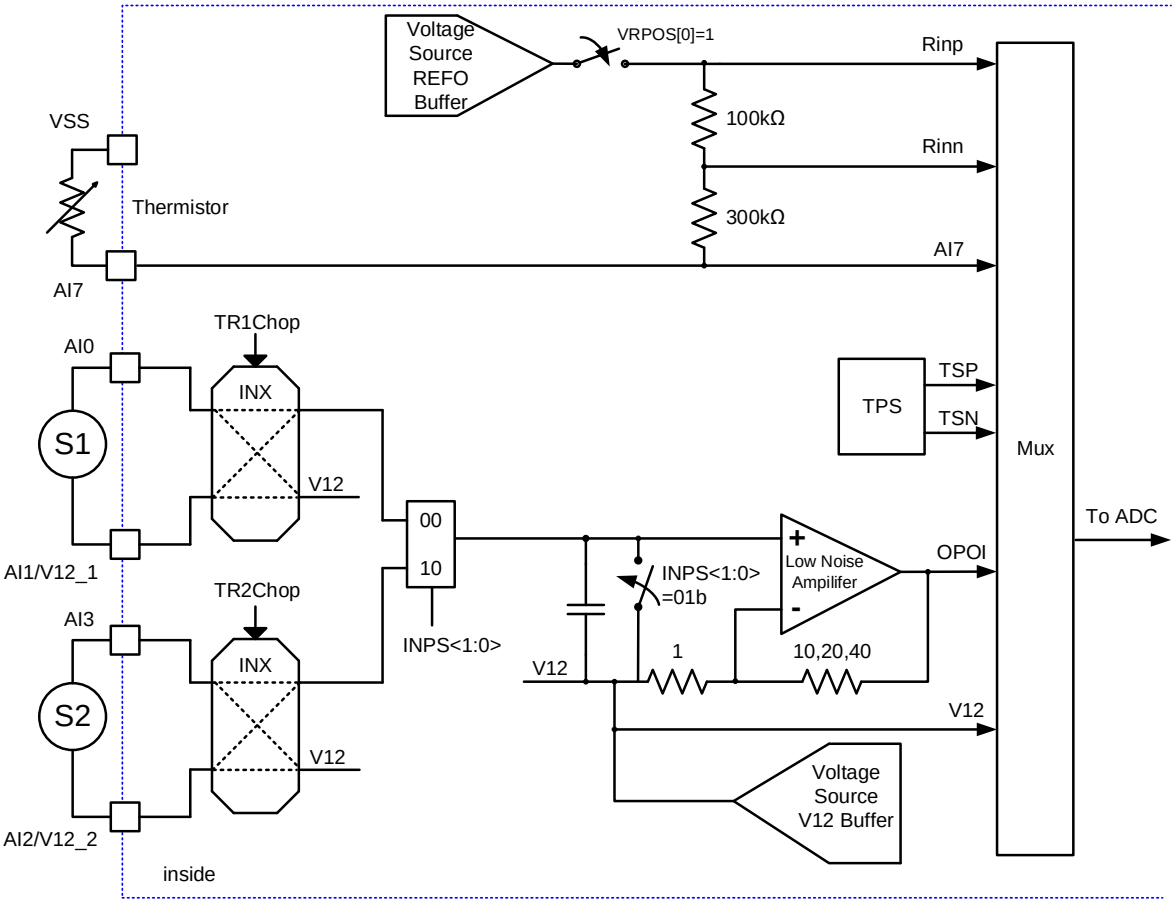


圖 4-9 Low Noise PGA Network

4.9. Comparator Network

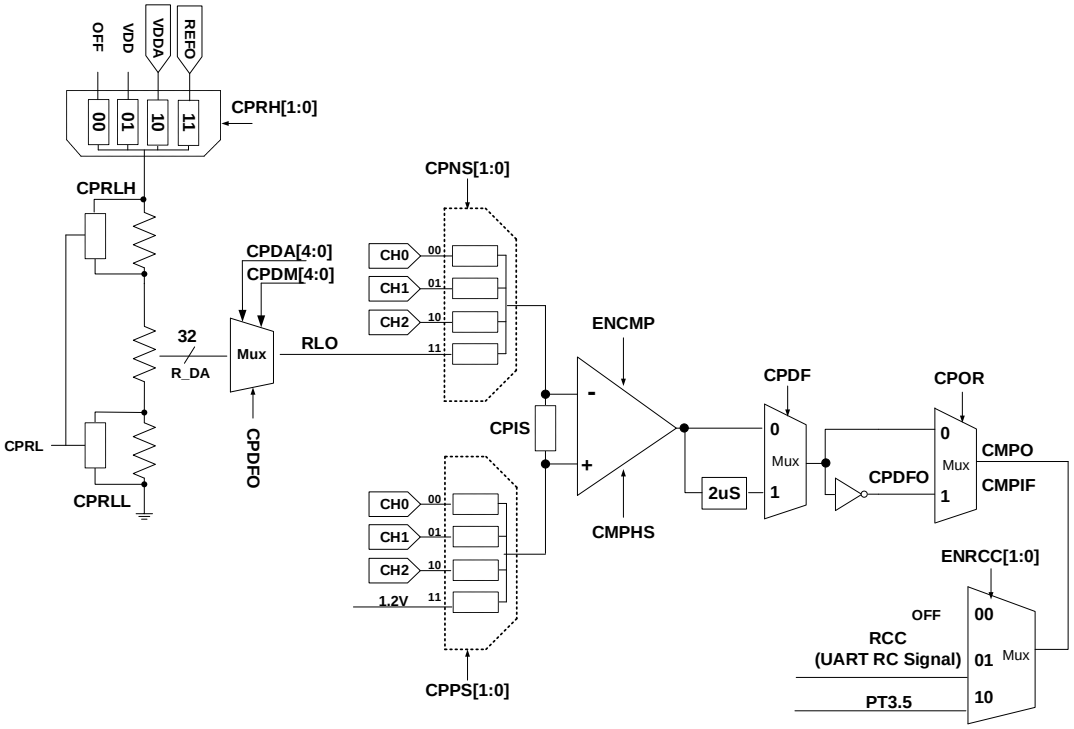


圖 4-10 Comparator Network

4.10. Watch Dog System

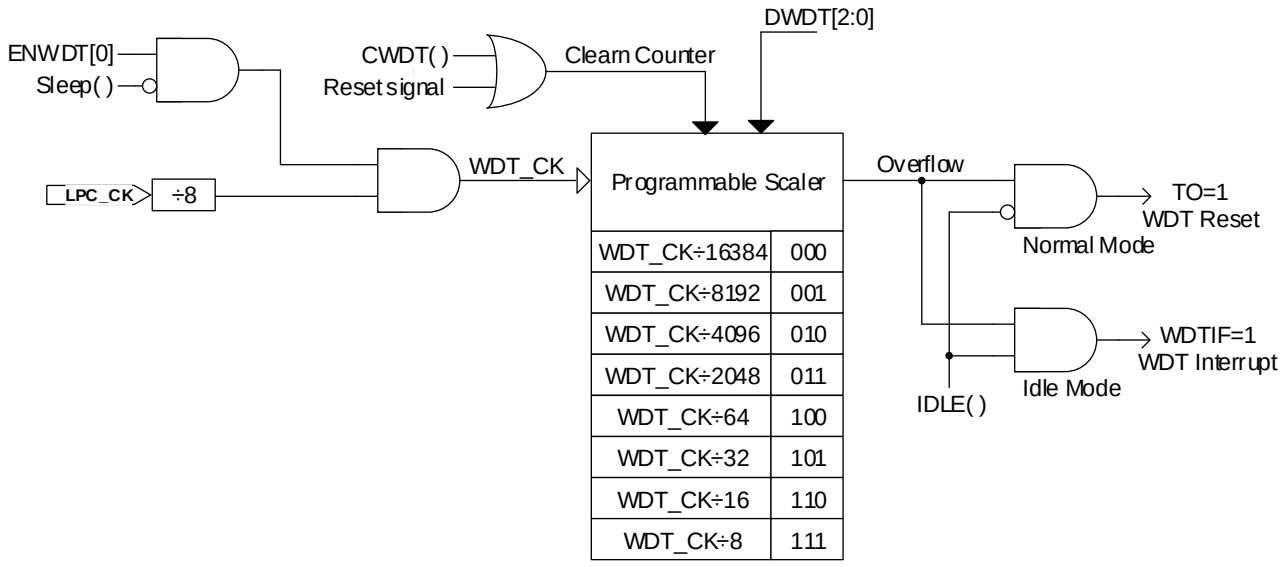


圖 4-11 Watch Dog System

4.11. 8-bit Timer A1 System (TMA1)

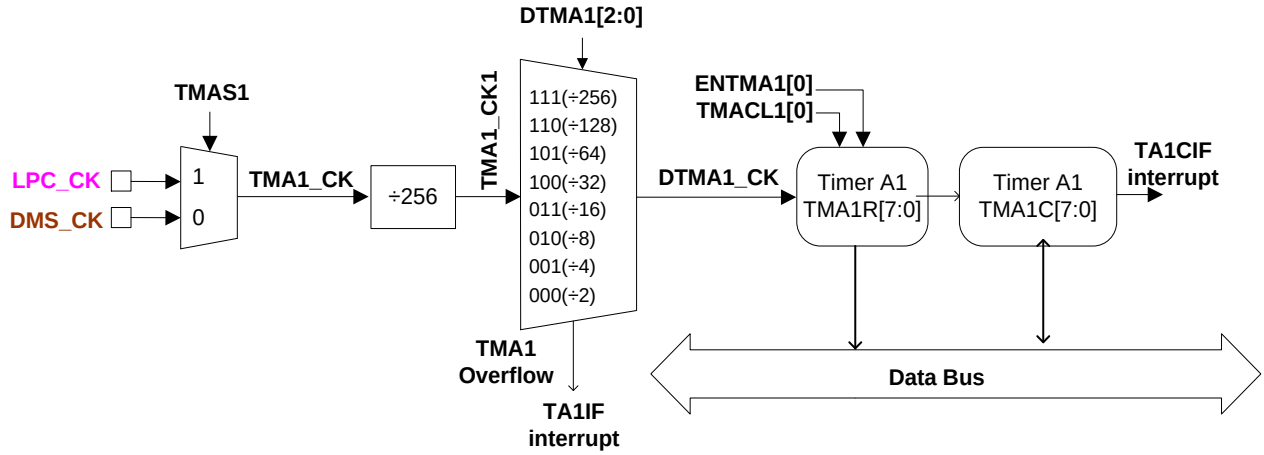


圖 4-12 Timer A1 System

4.12. 16-bit Timer B System (TMB)

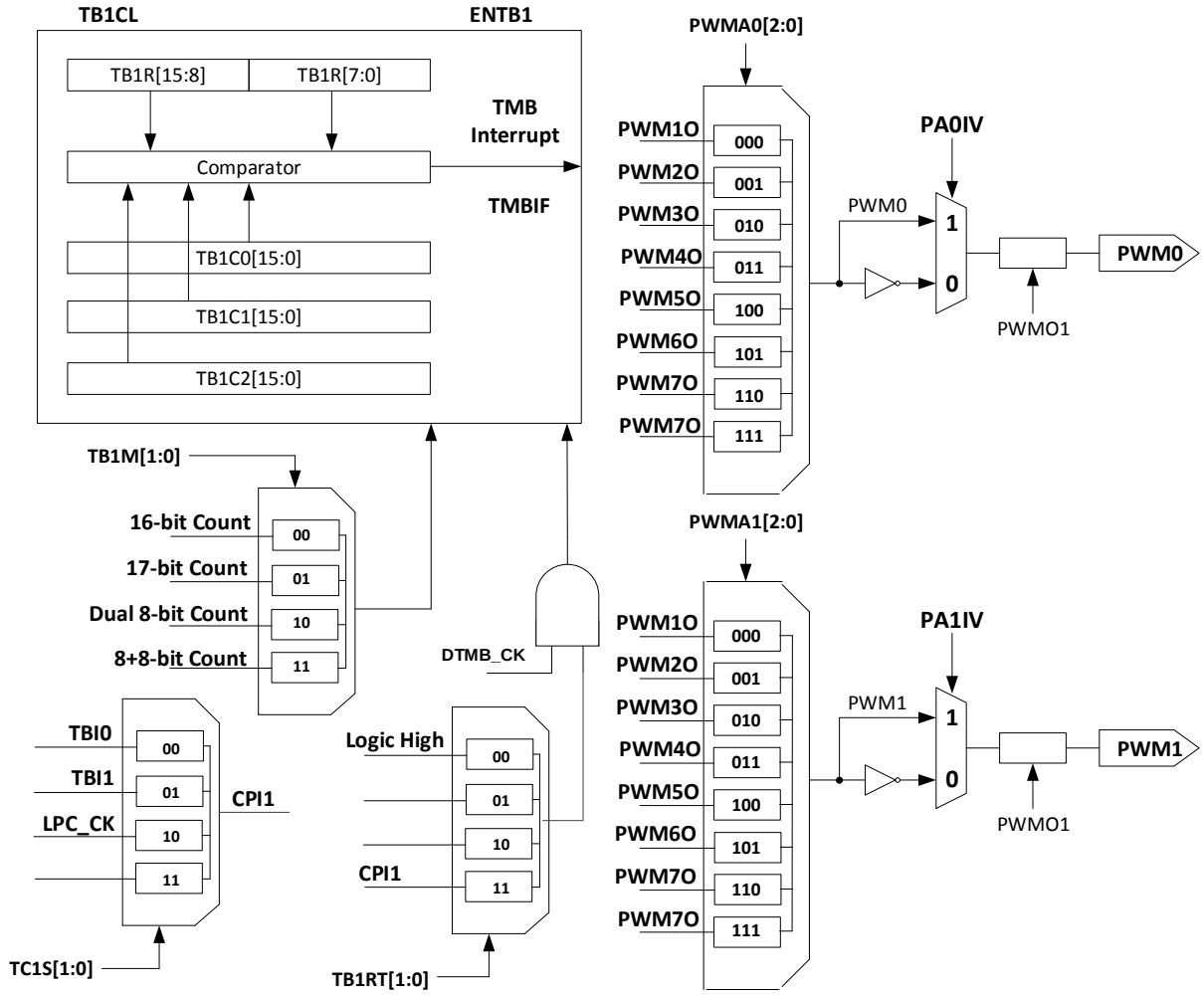


圖 4-13 Timer B System

4.13. I2C

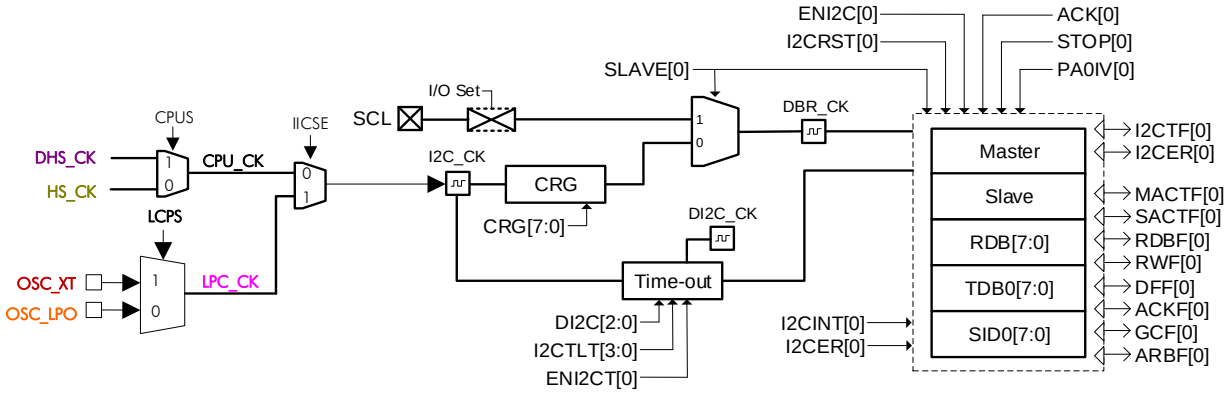


圖 4-14 I2C 方塊圖

4.14. EUART

EUART TRANSMIT BLOCK DIAGRAM

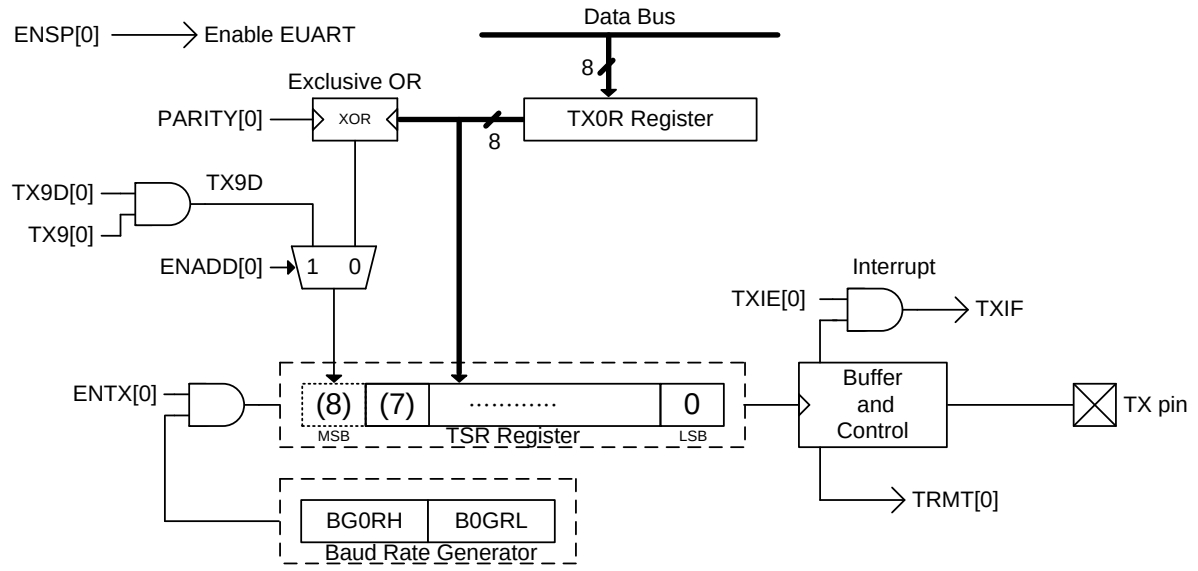
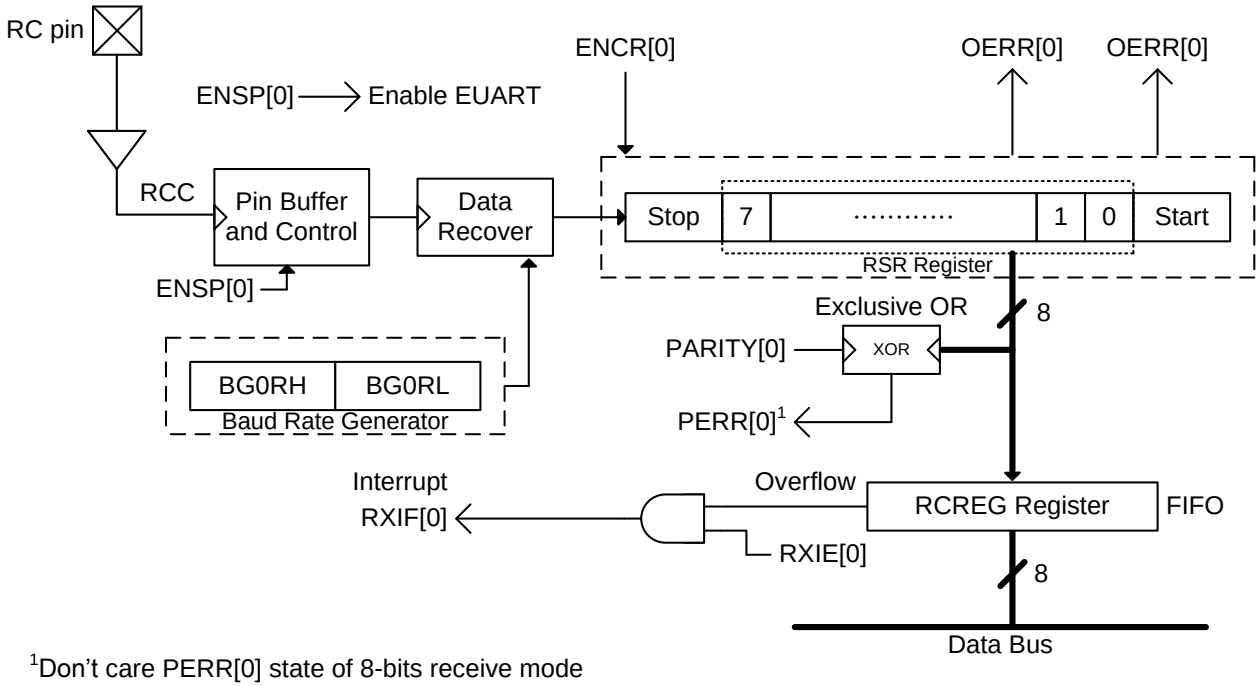


圖 4-15 EUART 傳送方塊圖

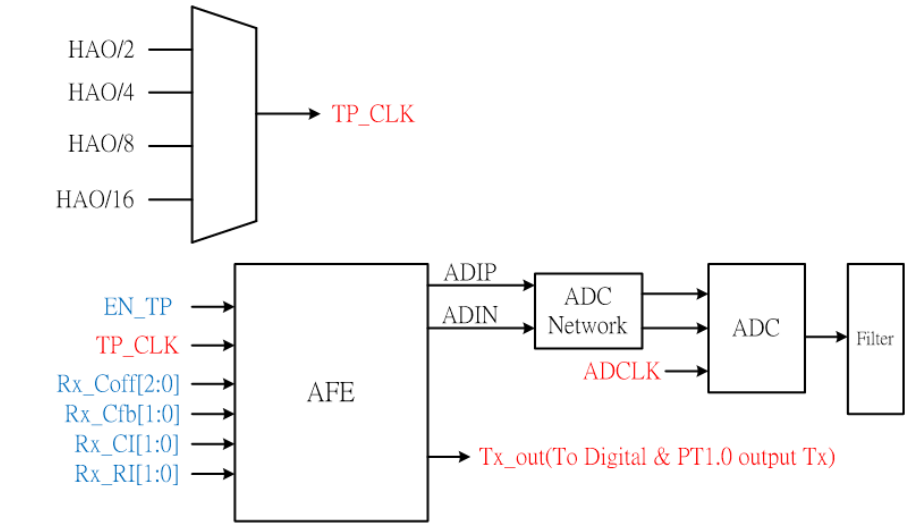
EUART 8-BITs RECEIVE BLOCK DIAGRAM

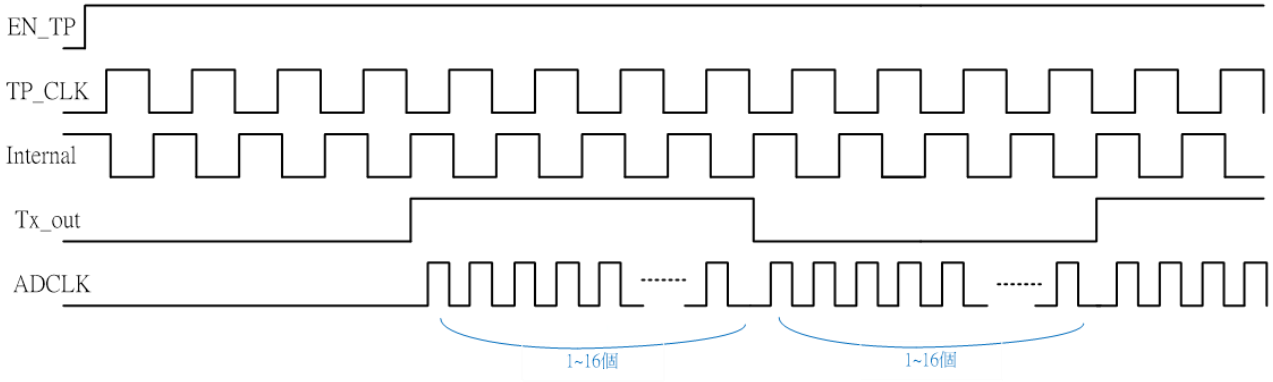


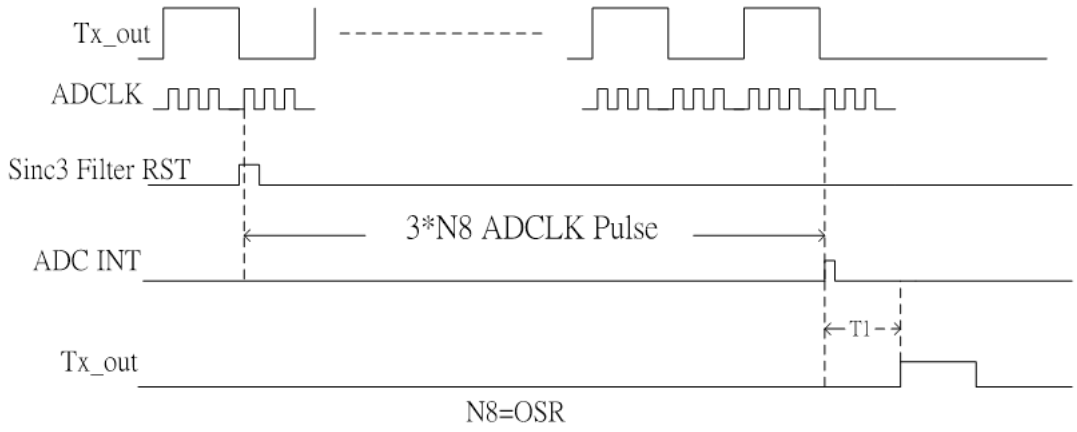
[1]Don't care PERR[0] state of 8-bits receive mode

圖 4-16 EUART 8-bits 接收方塊圖

4.15. Touch KEY







5. 暫存器列表

"-"no use,"*"read/write,"w"write,"r"read,"r0"only read 0,"r1"only read 1,"w0"only write 0,"w1"only write 1
"$"for event status,"."unimplemented bit,"x"unknown,"u"unchanged,"d"depends on condition

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	ARST	IRST	R/W
000h	INDF0	Contents of FSR0 to address data memory value of FSR0 not changed								xxxx xxxx	uuuu uuuu	*,*,*,*,*,*,*,*
001h	POINC0	Contents of FSR0 to address data memory value of FSR0 post-incremented								xxxx xxxx	uuuu uuuu	*,*,*,*,*,*,*,*
002h	PODEC0	Contents of FSR0 to address data memory value of FSR0 post-decremented								xxxx xxxx	uuuu uuuu	*,*,*,*,*,*,*,*
003h	PRINC0	Contents of FSR0 to address data memory value of FSR0 pre-incremented								xxxx xxxx	uuuu uuuu	*,*,*,*,*,*,*,*
004h	PLUSW0	Contents of FSR0 to address data memory value of FSR0 offset by W								xxxx xxxx	uuuu uuuu	*,*,*,*,*,*,*,*
005h	INDF1	Contents of FSR1 to address data memory value of FSR1 not changed								xxxx xxxx	uuuu uuuu	*,*,*,*,*,*,*,*
006h	POINC1	Contents of FSR1 to address data memory value of FSR1 post-incremented								xxxx xxxx	uuuu uuuu	*,*,*,*,*,*,*,*
007h	PODEC1	Contents of FSR1 to address data memory value of FSR1 post-decremented								xxxx xxxx	uuuu uuuu	*,*,*,*,*,*,*,*
008h	PRINC1	Contents of FSR1 to address data memory value of FSR1 pre-incremented								xxxx xxxx	uuuu uuuu	*,*,*,*,*,*,*,*
009h	PLUSW1	Contents of FSR1 to address data memory value of FSR1 offset by W								xxxx xxxx	uuuu uuuu	*,*,*,*,*,*,*,*
00Ah	INDF2	Contents of FSR2 to address data memory value of FSR2 not changed								xxxx xxxx	uuuu uuuu	*,*,*,*,*,*,*,*
00Bh	POINC2	Contents of FSR2 to address data memory value of FSR2 post-incremented								xxxx xxxx	uuuu uuuu	*,*,*,*,*,*,*,*
00Ch	PODEC2	Contents of FSR2 to address data memory value of FSR2 post-decremented								xxxx xxxx	uuuu uuuu	*,*,*,*,*,*,*,*
00Dh	PRINC2	Contents of FSR2 to address data memory value of FSR2 pre-incremented								xxxx xxxx	uuuu uuuu	*,*,*,*,*,*,*,*
00Eh	PLUSW2	Contents of FSR2 to address data memory value of FSR2 offset by W								xxxx xxxx	uuuu uuuu	*,*,*,*,*,*,*,*
00Fh	FSR0H	-	-	-	-	-	-	FSR0[9:8]		xx	.... ..uu	-,-,-,- -,-,*,*
010h	FSR0L	Indirect Data Memory Address Pointer 0 Low Byte,FSR0[7:0]								xxxx xxxx	uuuu uuuu	*,*,*,*,*,*,*,*
011h	FSR1H	-	-	-	-	-	-	FSR1[9:8]		xx	.... ..uu	-,-,-,- -,-,*,*
012h	FSR1L	Indirect Data Memory Address Pointer 0 Low Byte,FSR1[7:0]								xxxx xxxx	uuuu uuuu	*,*,*,*,*,*,*,*
013h	FSR2H	-	-	-	-	-	-	FSR2[9:8]		xx	.... ..uu	-,-,-,- -,-,*,*
014h	FSR2L	Indirect Data Memory Address Pointer 0 Low Byte,FSR2[7:0]								xxxx xxxx	uuuu uuuu	*,*,*,*,*,*,*,*
016h	TOSH	-	-	-	TOS[12:8]					...x xxxx	...u uuuu	-,-,-,-*,*,*,*
017h	TOSL	Top-of-Stack Low Byte (TOS[7:0])								xxxx xxxx	uuuu uuuu	*,*,*,*,*,*,*,*
018h	SKCN	SKFL	SKUN	SKOV	-	SKPRT[3:0]				000. 0000	u$$. $$$$	rw 0,rw 0,rw 0,- *,*,*,*
01Ah	PCLATH	-	-	-	PC[12:8]					 0000	 0000	-,-,-,- *,*,*,*
01Bh	PCLATL	PC Low Byte for PC[7:0]								0000 0000	0000 0000	*,*,*,*,*,*,*,*
01Dh	TBLPTRH	-	-	-	TBLPTR[12:8]					 xxxx	.... uuuu	-,-,-,- *,*,*,*
01Eh	TBLPTRL	Program Memory Table Pointer Low Byte (TBLPTR[7:0])								xxxx xxxx	uuuu uuuu	*,*,*,*,*,*,*,*
01Fh	TBLDH	Program Memory Table Latch High Byte								xxxx xxxx	uuuu uuuu	*,*,*,*,*,*,*,*
020h	TBLDL	Program Memory Table Latch Low Byte								xxxx xxxx	uuuu uuuu	*,*,*,*,*,*,*,*
021h	PRODH	Product Register of Multiply High Byte								xxxx xxxx	uuuu uuuu	*,*,*,*,*,*,*,*
022h	PRODL	Product Register of Multiply Low Byte								xxxx xxxx	uuuu uuuu	*,*,*,*,*,*,*,*
023h	INTE0	GIE	TA1CIE	ADIE	WDTIE	TB1IE		E1IE	E0IE	0000 0.00	0uuu uuuu	*,*,*,*,*,*,*,*
024h	INTE1	TA1IE		TXIE	RCIE	I2CERIE	I2CIE		E2IE	0.00 00.0	uuuu uuuu	*,*,*,*,*,*,*,*
025h	INTE2						CMPIE		BOR2IE	.... .0.0	uuuu uuuu	*,*,*,*,*,*,*,*
026h	INTF0	-	TA1CIF	ADIF	WDTIF	TB1IF		E1IF	E0IF	.000 0000	.uuu uuuu	*,*,*,*,*,*,*,*
027h	INTF1	TA1IF		TXIF	RCIF	I2CERIF	I2CIF		E2IF	0.00 00.0	uuuu uuuu	*,*,*,*,r,r,*,*
028h	INTF2						CMPIF		BOR2IF	.... .0.0	uuuu uuuu	*,*,*,*,*,*,*,*
029h	WREG	Working Register								xxxx xxxx	uuuu uuuu	*,*,*,*,*,*,*,*
02Ah	BSRCN	-	-	-	-	-	-	BSR[1:0]		x	....u	-,-,-,- -,-,-,*
02Bh	MSTAT	-	-	-	C	DC	N	OV	Z	...x xxxx	...u uuuu	-,-,-,*,*,*,*,*
02Ch	PSTAT	BOR	PD	TO	IDL	RST	SKERR	BOR2LV	GCRstIF	$000 $000	uu$u u$uu	rw0,rw0,rw0,rw0 rw0,rw0,r,rw0
02Eh	PWRCN	ENBGR	LDOC[2:0]			LDOM[1:0]		ENLDO	CSFON	1000 0000	uuuu uu0u	*,*,*,*,*,*,*,*
02Fh	OSCCN0	OSCS[1:0]		DHS[1:0]		DMS[2:0]			CUPS	0000 0000	uuuu uuuu	*,*,*,*,*,*,*,*
030h	OSCCN1	CCOPT	LCPS	DADC[1:0]		DTMB[1:0]		TMBS	-	0000 000.	uuuu uuu.	*,*,*,*,*,*,*,-
031h	OSCCN2	IDLEM1	IDLEM0	ENXT	XTS[1:0]		HAOM[1:0]		ENHAO	0000 0001	uuuu uuu1	*,*,*,*,*,*,*,*
032h	CSFCN0	SKRST	HAOTR[6:0]							.1..	....	-,-,-,- -,-,-,-
033h	CSFCN1	MCLR	-	ENINXCH	BOR_TH[2:0]			BORS	ENBOR2	0.00 0011	0.uu uuuu	*,-,*,*,*,*,*,*
034h	WDTCN	ENBZ	BZS	BZ[1:0]		ENWDT	DWDT[2:0]			0000 0000	uuuu $000	-,*,*,* rw 1,*,*,*
035h	AD1H	ADC1 conversion high byte data register								0000 0000	uuuu uuuu	r,r,r,r r,r,r,r
036h	AD1M	ADC1 conversion middle byte data register								0000 0000	uuuu uuuu	r,r,r,r r,r,r,r
037h	AD1L	ADC1 conversion low byte data register								0000 0000	uuuu uuuu	r,r,r,r r,r,r,r
038h	AD1HH	ADC1 conversion high byte data register								0000 0000	uuuu uuuu	*,*,*,*,*,*,*,*
039h	AD1MM	ADC1 conversion middle byte data register								0000 0000	uuuu uuuu	*,*,*,*,*,*,*,*
03Ah	AD1LL	ADC1 conversion low byte data register								0000 0000	uuuu uuuu	*,*,*,*,*,*,*,*
03Bh	AD1CN0	ENAD1	-		OSR[3:0]				CMFR	0000 0000	uuuu uuuu	*,*,*,*,*,*,*,*
03Ch	AD1CN1	-	REFO1	VREGN	REFOS[1:0]		ADGN[2:0]			0000 0000	uuuu uuuu	*,*,*,*,*,*,*,*
03Dh	AD1CN2	ADSIPB	ADSINB	-	SELVIN	DCSET[3:0]				0000 0000	uuuu uuuu	*,*,*,*,*,*,*,*
03Eh	AD1CN3	INP[3:0]				INN[3:0]				0000 0000	uuuu uuuu	*,*,*,*,*,*,*,*
03Fh	AD1CN4	VRH[1:0]		VRL[1:0]		INX[1:0]		VRIS	INIS	0000 0000	uuuu uuuu	*,*,*,*,*,*,*,*
040h	AD1CN5	ENACM	V12SEL	VCMS	LDOPL	ENREFO	-	ENTPS	TPSCH	0000 0000	uuuu uuuu	*,*,*,*,*,*,*,*

表 5-1 資料記憶體列表

"-"no use,"*"read/write,"w"write,"r"read,"r0"only read 0,"r1"only read 1,"w0"only write 0,"w1"only write 1

"$"for event status,"."unimplemented bit,"x"unknown,"u"unchanged,"d"depends on condition

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	ARST	IRST	R/W
041h	LVDCN	DAFM	ENCH	-	-	-	-	-	-	00..	uu..	*,*,*,*,*,*,*,*
042h	LNAMP0	INP[4]	INN[4]	-	TR2Chop	TR1Chop	VRPOS	-	-	00.0 00..	uu.u uu..	*,*,*,*,*,*,*,*
043h	LNAMP1	ENPGA	-	INPS[1:0]		PGAG[1:0]		PGACH[1:0]		0000 0000	uuuu uuuu	*,*,*,*,*,*,*,*
044h	TMA1CN	ENTMA1	TMACL1	TMAS1	DTMA1[2:0]			-		0000 0000	u0uu uuuu	*,rw 1,*,*,*,*,*
045h	TMA1R	TMA1 counter Register								0000 0000	uuuu uuuu	rw0,rw0,rw0,rw0 rw0,rw0,rw0,rw0
046h	TMA1C	TMA1C counter Register								0000 0000	uuuu uuuu	rw0,rw0,rw0,rw0 rw0,rw0,rw0,rw0
047h	TB1Flag	-	PWM7A	PWM6A	PWM5A	PWM4A	PWM3A	PWM2A	PWM1A	..00 0000	..uu uuuu	-,-,r,r r,r,r,r
048h	TB1CN0	ENTB1	TB1M[1:0]		TB1RT[1:0]		TB1CL	PWMO1	PWMO0	0000 0000	uuuu u0uu	*,*,*,*,rw 1,*,*
049h	TB1CN1	PA1IV	PWMA1[2:0]			PA0IV	PWMA0[2:0]			0000 0000	uuuu uuuu	*,*,*,*,*,*,*,*
04Ah	TB1RH	TimerB1 counter Register [15:8]								xxxx xxxx	uuuu uuuu	r,r,r,r r,r,r,r
04Bh	TB1RL	TimerB1 counter Register [7:0]								xxxx xxxx	uuuu uuuu	r,r,r,r r,r,r,r
04Ch	TB1C0H	TimerB1 counter Condition Register [15:8]								xxxx xxxx	uuuu uuuu	*,*,*,*,*,*,*,*
04Dh	TB1C0L	TimerB1 counter Condition Register [7:0]								xxxx xxxx	uuuu uuuu	*,*,*,*,*,*,*,*
04Eh	TB1C1H	TimerB1 counter Condition Register [15:8]								xxxx xxxx	uuuu uuuu	*,*,*,*,*,*,*,*
04Fh	TB1C1L	TimerB1 counter Condition Register [7:0]								xxxx xxxx	uuuu uuuu	*,*,*,*,*,*,*,*
050h	TB1C2H	TimerB1 counter Condition Register [15:8]								xxxx xxxx	uuuu uuuu	*,*,*,*,*,*,*,*
051h	TB1C2L	TimerB1 counter Condition Register [7:0]								xxxx xxxx	uuuu uuuu	*,*,*,*,*,*,*,*
052h	TC1CN0	-	TC1S[1:0]		-	-	-	-	-	0000 0000	uuuu uuuu	uuuu uuuu
053h	PT1	-	PT1.6	PT1.5	PT1.4	PT1.3	PT1.2	PT1.1	PT1.0	.xxx xxxx	.xxx xxxx	-,*,*,*,*,*,*,*
054h	PT1IN	-	IN1.6	IN1.5	IN1.4	IN1.3	IN1.2	IN1.1	IN1.0	0000 0000	uuuu uuuu	*,*,*,*,*,*,*,*
055h	TRISC1	-	TC1.6	TC1.5	TC1.4	TC1.3	TC1.2	TC1.1	TC1.0	0000 0000	uuuu uuuu	*,*,*,*,*,*,*,*
056h	PT1DA	-	DA1.6	DA1.5	DA1.4	DA1.3	DA1.2	DA1.1	DA1.0	0000 0000	uuuu uuuu	*,*,*,*,*,*,*,*
057h	PT1PU	-	PU1.6	PU1.5	PU1.4	PU1.3	PU1.2	PU1.1	PU1.0	0000 0000	uuuu uuuu	*,*,*,*,*,*,*,*
058h	PT1M1	-	-	INTEG2[1:0]		INTEG1[1:0]		INTEG0[1:0]		0000 0000	uuuu uuuu	*,*,*,*,*,*,*,*
059h	PT1INT	-	INTG1.6	INTG1.5	INTG1.4	INTG1.3	-	-	-	0000 0000	uuuu uuuu	*,*,*,*,*,*,*,*
05Ah	PT1INTE	-	INTE1.6	INTE1.5	INTE1.4	INTE1.3	-	-	-	0000 0000	uuuu uuuu	*,*,*,*,*,*,*,*
05Bh	PT1INTF	-	INTF1.6	INTF1.5	INTF1.4	INTF1.3	-	-	-	0000 0000	uuuu uuuu	*,*,*,*,*,*,*,*
05Ch	PT3	PT3.7	PT3.6	PT3.5	PT3.4	PT3.3	PT3.2	PT3.1	PT3.0	xxxx xxxx	xxxx xxxx	*,*,*,*,*,*,*,*
05Dh	PT3IN	IN3.7	IN3.6	IN3.5	IN3.4	IN3.3	IN3.2	IN3.1	IN3.0	0000 0000	uuuu uuuu	*,*,*,*,*,*,*,*
05Eh	TRISC3	TC3.7	TC3.6	TC3.5	TC3.4	TC3.3	TC3.2	TC3.1	TC3.0	0000 0000	uuuu uuuu	*,*,*,*,*,*,*,*
05Fh	PT3DA	DA3.7	DA3.6	DA3.5	DA3.4	DA3.3	DA3.2	DA3.1	DA3.0	0000 0000	uu.. ..uu	*,*,-,- -,-,*,*
060h	PT3PU	PU3.7	PU3.6	PU3.5	PU3.4	PU3.3	PU3.2	PU3.1	PU3.0	0000 0000	uuuu uuuu	*,*,*,*,*,*,*,*
061h	PT3INT	INTG3.7	INTG3.6	INTG3.5	INTG3.4	INTG3.3	INTG3.2	INTG3.1	INTG3.0	0000 0000	uuuu uuuu	*,*,*,*,*,*,*,*
062h	PT3INTE	INTE3.7	INTE3.6	INTE3.5	INTE3.4	INTE3.3	INTE3.2	INTE3.1	INTE3.0	0000 0000	uuuu uuuu	*,*,*,*,*,*,*,*
063h	PT3INTF	INTF3.7	INTF3.6	INTF3.5	INTF3.4	INTF3.3	INTF3.2	INTF3.1	INTF3.0	0000 0000	uuuu uuuu	*,*,*,*,*,*,*,*
064h	UR0CN	ENSP	ENTX	TX9	TX9D	PARITY	-	-	WUE	0000 0..0	uuuu u..u	*,*,*,*,-,-,*
065h	UR0STA	-	RC9D	PERR	FERR	OERR	RCIDL	TRMT	ABDOVF	.000 0010	.uuu uuuu	-,r,r,r r,r,r,rw 0
066h	BA0CN	UARTSE	-	-	-	ENCR	RC9	ENADD	ENABD	0... 0000	u... uuuu	*,-,-,- *,*,*,*
067h	BG0RH	-	-	-	Baud Rate Generator Register High Byte					...x xxxx	...u uuuu	-,-,-,*,*,*,*,*
068h	BG0RL	Baud Rate Generator Register Low Byte								xxxx xxxx	uuuu uuuu	*,*,*,*,*,*,*,*
069h	TX0R	UART Transmit Register								xxxx xxxx	uuuu uuuu	*,*,*,*,*,*,*,*
06Ah	RC0REG	UART Receive Register								xxxx xxxx	uuuu uuuu	r,r,r,r r,r,r,r
06Bh	MCCN0	ENRCC[1:0]		CMPO	CPIS	CPOR	CPDF	CMPHS	ENCMP	0000 0000	uuuu uuuu	*,*,r,*,*,*,*,*
06Ch	MCCN1	CPRL	VRSEL	CPRH[1:0]		CPPS[1:0]		CPNS[1:0]		0000 0000	uuuu uuuu	*,*,*,*,*,*,*,*
06Dh	MCCN2				CPDA[4:0]					0000 0000	uuuu uuuu	*,*,*,*,*,*,*,*
06Eh	MCCN3				CPDM[4:0]					0000 0000	uuuu uuuu	*,*,*,*,*,*,*,*
06Fh	-	-		-	-	-	-		-	0000 .000	uuuu .uuu	*,*,*,*-,*,*,*
070h	CFG0	IICSE	ENRSH	-	-	-	GCRst	ENI2CT	ENI2C	00.. .000	uu.. .uuu	*,*,-,- -,*,*,*
071h	ACT0	SLAVE	-	-	I2CER	START	STOP	I2CINT	ACK	0..0 0000	u..u uuuu	*,*,*,*,*,*,*,*
072h	STA0	MACTF	SACTF	RDBF	RWF	DFF	ACKF	GCF	ARBF	0001 0000	uuuu uuuu	*,*,*,*,*,*,*,*
073h	CRG0	CRG[7:0]								0000 0000	uuuu uuuu	*,*,*,*,*,*,*,*
074h	TOC0	I2CTF	DI2C[2:0]			I2CTLT[3:0]				0000 0000	uuuu uuuu	*,*,*,*,*,*,*,*
075h	RDB0	RDB[7:1]							RDB[0]	xxxx xxxx	uuuu uuuu	*,*,*,*,*,*,*,*
076h	TDB0	TDB0[7:1]							TDB0[0]	xxxx xxxx	uuuu uuuu	*,*,*,*,*,*,*,*
077h	SID0	SID0[7:1],The corresponding address of the 7-bit mode							SID0V[0]	0000 0000	uuuu uuuu	*,*,*,*,*,*,*,*
078h	GPort0	GBuz[2:0]			GTBI1[1:0]		-	GTBI0[1:0]		0000 0000	uuuu uuuu	*,*,*,*,*,*,*,*
079h	GPort1	GPWM1[3:0]				GPWM0[3:0]				0000 0000	uuuu uuuu	*,*,*,*,*,*,*,*
07Ah	GPort2	GSCL[3:0]				GTX[3:0]				0000 0000	uuuu uuuu	*,*,*,*,*,*,*,*
07Bh	GPort3	-	-	-	-	-	-	GTKTX[1:0]		0000 0000	uuuu uuuu	*,*,*,*,*,*,*,*
07Ch	FWRST	FWRST data register[7:0]								0000 0000	uuuu uuuu	*,*,*,*,*,*,*,*
07Fh	VerID	VerID data register[7:0]								0001 0000	0001 0000	r,r,r,r r,r,r,r

表 5-2 資料記憶體列表

"-"no use,"*"read/write,"w"write,"r"read,"r0"only read 0,"r1"only read 1,"w0"only write 0,"w1"omly write 1

"$"for event status,"."unimplemented bit,"x"unknown,"u"unchanged,"d"depends on condition

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	ARST	IRST	R/W
180h	-	-	-	-	-	-	-	-	-	0.0. .000	0u0u u000	r,-,*,- -,*,*
181h	-	-	-	-	-					xxxx xxxx	uuuu uuuu	*,*,*,*,*,*,*,*
182h	-	-								xxxx xxxx	uuuu uuuu	*,*,*,*,*,*,*,*
183h	-	-								xxxx xxxx	uuuu uuuu	*,*,*,*,*,*,*,*
184h	-	-								xxxx xxxx	uuuu uuuu	*,*,*,*,*,*,*,*
185h	-	-								0000 0000	0000 0000	*,*,*,*,*,*,*,*
186h	BIECN	-	-	-	-	-	-	-	-	x000 $000	u000 $uuu	r,*,*,* r,*,*,*
187h	BIEARH	-	-	-	-	-	-	-	-	0.xx xxxx	u.uu uuuu	*,-,*,*,*,*,*,*
188h	BIEARL	-								xxxx xxxx	uuuu uuuu	*,*,*,*,*,*,*,*
189h	BIEDRH	-								xxxx xxxx	uuuu uuuu	*,*,*,*,*,*,*,*
18Ah	BIEDRL	-								xxxx xxxx	uuuu uuuu	*,*,*,*,*,*,*,*
18Bh	EECR1	EEMODE		-	-	-	-	-	EEWR	0000 0000	uuuu uuuu	*,*,*,*,*,*,*,*
18Ch	EECR2	Read Command : Write 0xA5, then reload datas to EERD0~ EERD31								0000 0000	uuuu uuuu	*,*,*,*,*,*,*,*
190h	-	-	-	-	-			-	-	0000 0000	0000 0000	r,r,r,r *,*,*,*
191h	-	-						-		0000 0000	0000 0000	*,*,*,*,*,*,*,*
192h	-	-								0000 0000	0000 0000	*,*,*,*,*,*,*,*
193h	-							-		xxxx xxxx	xxxx xxxx	r,r,r,r r,r,r,r
194h	-	-								xxxx xxxx	xxxx xxxx	r,r,r,r r,r,r,r
195h	-		-							xxxx xxxx	xxxx xxxx	r,r,r,r r,r,r,r
196h	-	-					-			0000 0000	0000 0000	*,*,*,*,*,*,*,*
197h	BIEKEY	BIE KEY Data Register								0000 0000	0000 0000	*,*,*,*,*,*,*,*
198h	PT2	PT2.7	PT2.6	PT2.5	PT2.4	PT2.3	PT2.2	PT2.1	PT2.0	xxxx xxxx	xxxx xxxx	*,*,*,*,*,*,*,*
199h	PT2IN	IN2.7	IN2.6	IN2.5	IN2.4	IN2.3	IN2.2	IN2.1	IN2.0	0000 0000	uuuu uuuu	*,*,*,*,*,*,*,*
19Ah	TRISC2	TC2.7	TC2.6	TC2.5	TC2.4	TC2.3	TC2.2	TC2.1	TC2.0	0000 0000	uuuu uuuu	*,*,*,*,*,*,*,*
19Bh	PT2DA	-	-	-	-	-	-	-	-	xxxx xxxx	xxxx xxxx	-,-,-,- -,-,-,-
19Ch	PT2PU	PU2.7	PU2.6	PU2.5	PU2.4	PU2.3	PU2.2	PU2.1	PU2.0	0000 0000	uuuu uuuu	*,*,*,*,*,*,*,*
19Dh	PT2INT	INTG2.7	INTG2.6	INTG2.5	INTG2.4	INTG2.3	INTG2.2	INTG2.1	INTG2.0	0000 0000	uuuu uuuu	*,*,*,*,*,*,*,*
19Eh	PT2INTE	INTE2.7	INTE2.6	INTE2.5	INTE2.4	INTE2.3	INTE2.2	INTE2.1	INTE2.0	0000 0000	uuuu uuuu	*,*,*,*,*,*,*,*
19Fh	PT2INTF	INTF2.7	INTF2.6	INTF2.5	INTF2.4	INTF2.3	INTF2.2	INTF2.1	INTF2.0	0000 0000	uuuu uuuu	*,*,*,*,*,*,*,*
1A0h	CCNT	-	-	-	-	-	CCLevel[2:0]			xxxx x000	uuuu uuuu	*,*,*,*,*,*,*,*
1A1h	ENCCMode	ENCC7	ENCC6	ENCC5	ENCC4	ENCC3	ENCC2	ENCC1	ENCC0	0000 0000	uuuu uuuu	*,*,*,*,*,*,*,*
1A2h	TKCN1	ENTP	Rx_RI[1:0]		RX_CI[1:0]		Rx_Coff[2:0]			0000 0000	uuuu uuuu	*,*,*,*,*,*,*,*
1A3h	TKCN2	TXADCKCNT[3:0]				Rx_Cfb[1:0]		TP_CLK[1:0]		0000 0000	uuuu uuuu	*,*,*,*,*,*,*,*
1A4h	TKCN3	-	MRx	RxMx[1:0]		TXSettle[2:0]			TKCMS	0000 0000	uuuu uuuu	*,*,*,*,*,*,*,*
1A5h	-	-			-			-	-	0000 0000	uuuu uuuu	*,*,*,*,*,*,*,*
1A6h	-	-			-					0000 0000	uuuu uuuu	*,*,*,*,*,*,*,*
1A7h	-	-			-					0000 0000	uuuu uuuu	*,*,*,*,*,*,*,*
080h ~ 0FFh		SRAM as 128Byte								uuuu uuuu	uuuu uuuu	*,*,*,*,*,*,*,*
100h ~ 17Fh		SRAM as 128Byte								uuuu uuuu	uuuu uuuu	*,*,*,*,*,*,*,*
200h ~ 2FFh		SRAM as 256Byte								uuuu uuuu	uuuu uuuu	*,*,*,*,*,*,*,*
300h ~ 33Fh		EE Data Buffer (64Byte)								uuuu uuuu	uuuu uuuu	*,*,*,*,*,*,*,*

表 5-3 資料記憶體列表

6. 電氣特性

Absolute Maximum Ratings :
Absolute maximum ratings over operating free-air temperature (unless otherwise noted)
Voltage applied at V_{DD} /V_{DD1} to V_{SS} . . . . −0.2 V to 6.0 V
Voltage applied to any pin . . . . −0.2 V to V_{DD} + 0.3 V
Diode current at any device terminal . . . . ±2 mA
Storage temperature, ... −55℃ to 125℃
(Operation Mode) . . . . −40℃ to 85℃
Total power dissipation. 0.5w
Maximum output current sink by any I/O pin. 20mA

6.1. Recommended operating conditions

T_A = -40℃ ~ 85℃,unless otherwise noted

Sym.	Parameter		Test Conditions		Min.	Typ.	Max.	Unit
V_{DD}	Supply Voltage		All digital peripherals and CPU V_{DD} = 1.9V~5.5V, Frequency<=9.6MHz, V_{DD} = 3.6V~5.5V, Frequency<=16MHz,		1.9		5.5	V
V_{DDA}	Supply Voltage		Analog peripherals		2.4		5.5	
V_{SS}	Supply Voltage				0		0	
XT	External Oscillator Frequency	Watch crystal	V_{DD} =2.2V~5.5V, ENXT[0]=1	XTS[1:0]=0x		32768		Hz
		Ceramic resonator, Crystal		XTS[1:0]=10	450K		4M	
				XTS[1:0]=11	1M		8M	
		Ceramic resonator, Crystal	V_{DD} = 3.6V~5.5V, ENXT[0]=1	XTS[1:0]=11	450K		16M	

6.2. Internal RC Oscillator

T_A = 25℃,VDD = 3.3V,unless otherwise noted

Sym.	Parameter	Test Conditions		Min.	Typ.	Max.	Unit
HAO	High Speed Oscillator frequency, After writer Trim.	ENHAO[0]=1b, HAOM[1:0]=00b	VDD=3V/5V, T_A = 25℃	-1%	1.843	+1%	MHz
			VDD=3V/5V, T_A = -40℃~ 85℃	-3%	1.843	+3%	
			VDD=2.2V~5.5V, T_A = 25℃	-3%	1.843	+3%	
			VDD=2.2V~5.5V, T_A = -40℃~ 85℃	-6%	1.843	+6%	
		ENHAO[0]=1b, HAOM[1:0]=01b	VDD=3V/5V, T_A = 25℃	-1%	4.147	+1%	MHz
			VDD=3V/5V, T_A = -40℃~ 85℃	-3%	4.147	+3%	
			VDD=2.2V~5.5V, T_A = 25℃	-3%	4.147	+3%	
			VDD=2.2V~5.5V, T_A = -40℃~ 85℃	-6%	4.147	+6%	
		ENHAO[0]=1b, HAOM[1:0]=10b	VDD=3V/5V, T_A = 25℃	-1%	8.755	+1%	MHz
			VDD=3V/5V, T_A = -40℃~ 85℃	-3%	8.755	+3%	
			VDD=2.2V~5.5V, T_A = 25℃	-4%	8.755	+4%	
			VDD=2.2V~5.5V, T_A = -40℃~ 85℃	-8%	8.755	+8%	
		ENHAO[0]=1b, HAOM[1:0]=11b	VDD=3.6V/5V, T_A = 25℃	-1%	15.667	+1%	MHz
			VDD=3.6V/5V, T_A = -40℃~ 85℃	-3%	15.667	+3%	
			VDD=3.6V~5.5V, T_A = 25℃	-2%	15.667	+2%	
			VDD=3.6V~5.5V, T_A = -40℃~ 85℃	-5%	15.667	+5%	
LPO	Low Power Oscillator frequency	VDD=2.2V~5.5V, T_A = 25℃		-20%	14.5	+20%	KHz

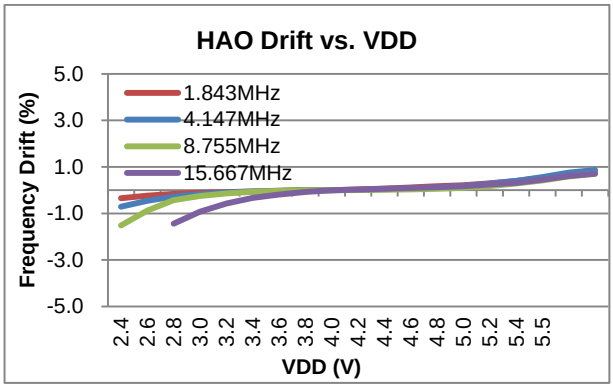


Figure 6.2-1 HAO vs. VDD

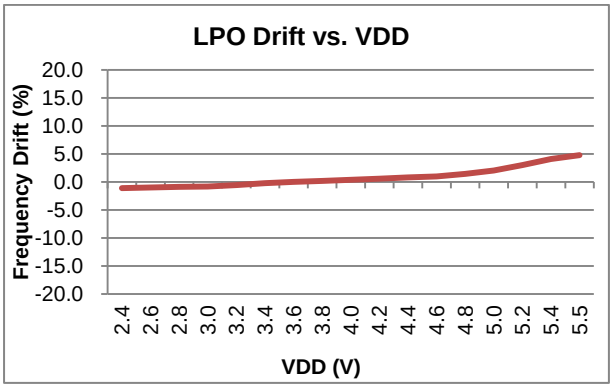


Figure 6.2-2 LPO vs. VDD

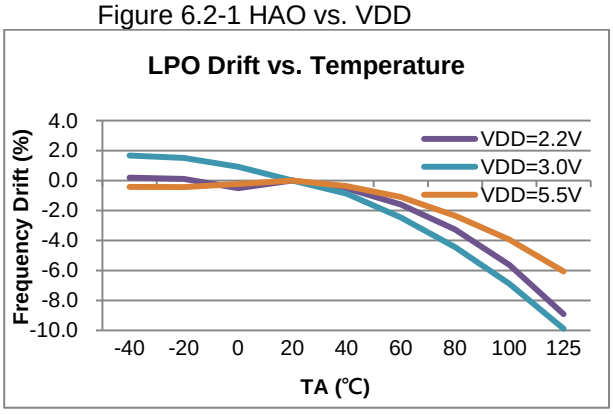


Figure 6.2-3 LPO vs. Temperature

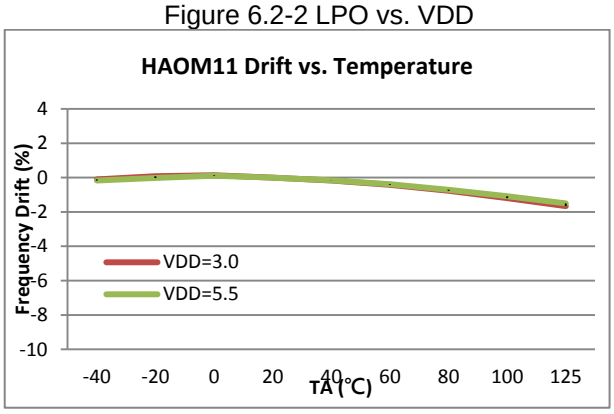


Figure 6.2-4 HAO(17.51MHz) vs. Temperature

6.3. Supply current into VDD excluding peripherals current

T_A = 25℃,V_{DD} = 3.3V, BOR2 OFF, OSC_CY = off, unless otherwise noted

Sym.	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
I_{AM1}	Active mode 1	OSC_HAO = 15.6MHz, CPU_CK = 15.6MHz		1700	2500	uA
I_{AM5}	Active mode 5	OSC_HAO = 4.147MHz, CPU_CK = OSC_HAO		785	1200	uA
I_{LP1}	Low Power 1	OSC_HAO=off, CPU_CK = LPO		490	735	uA
I_{LP2}	Low Power 2	OSC_HAO=off, CPU_CK = LPO, Idle state		0.5	2	uA
I_{LP3}	Low Power 3	OSC_HAO=off, CPU_CK = off, Sleep state		0.1	1	uA

OSC_CY：External Oscillator frequency.
OSC_HAO：Internal High Accuracy Oscillator frequency.
CPU_CK：CPU core work frequency.

T_A = 25℃,V_{DD} = 5.5V, BOR2 OFF, OSC_CY = off, unless otherwise noted

Sym.	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
I_{AM1}	Active mode 1	OSC_HAO = 15.6MHz, CPU_CK = 15.6MHz		2850	4200	uA
I_{AM5}	Active mode 5	OSC_HAO = 4.147MHz, CPU_CK = OSC_HAO		1100	1650	uA
I_{LP1}	Low Power 1	OSC_HAO = off, CPU_CK = LPO		510	765	uA
I_{LP2}	Low Power 2	OSC_HAO=off, CPU_CK = LPO, Idle state		1.3	4	uA
I_{LP3}	Low Power 3	OSC_HAO=off, CPU_CK = off, Sleep state		0.3	2	uA

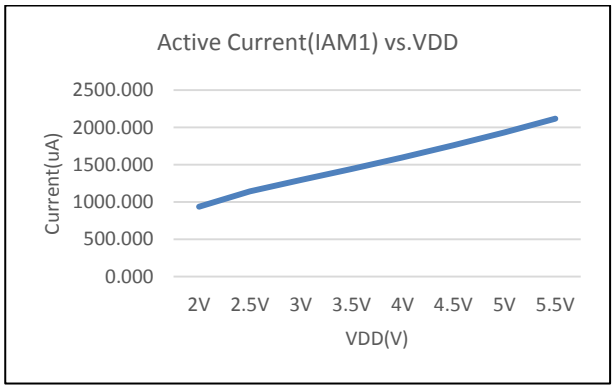


Figure 6.3-1 I_{AM1} vs. VDD

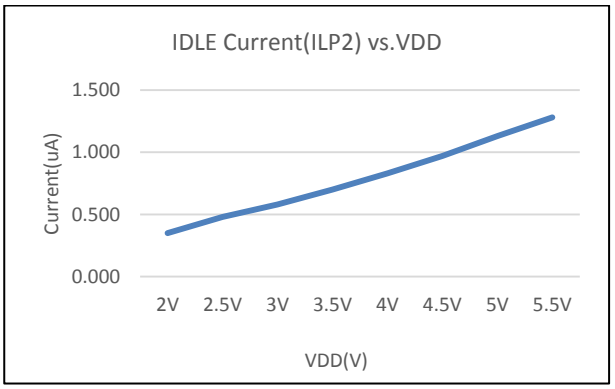


Figure 6.3-3 I_{LP2} vs. VDD

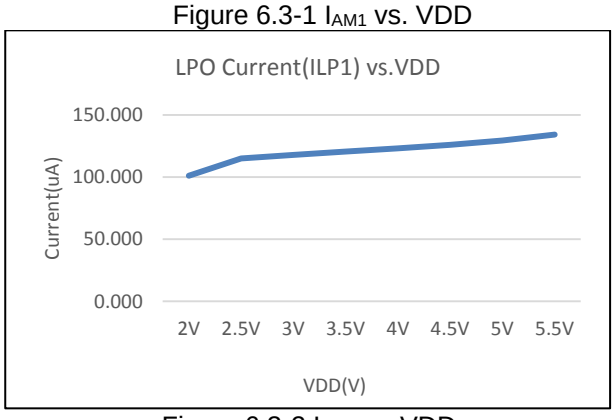


Figure 6.3-2 I_{LP1} vs. VDD

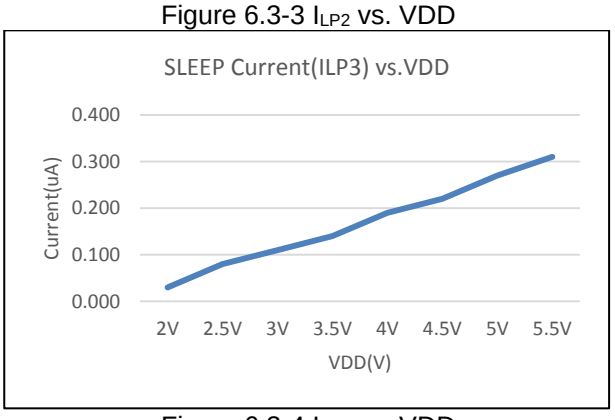


Figure 6.3-4 I_{LP3} vs. VDD

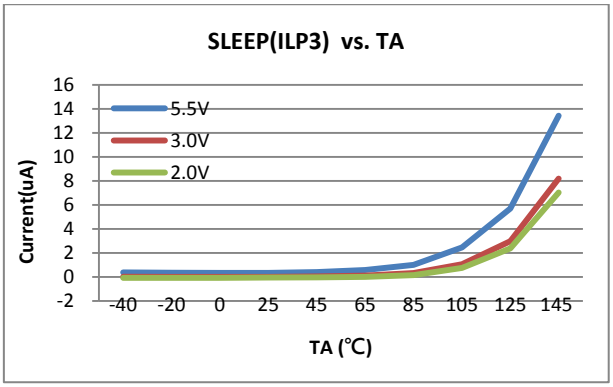


Figure 6.3-5 I_{LP3} vs. Temperature

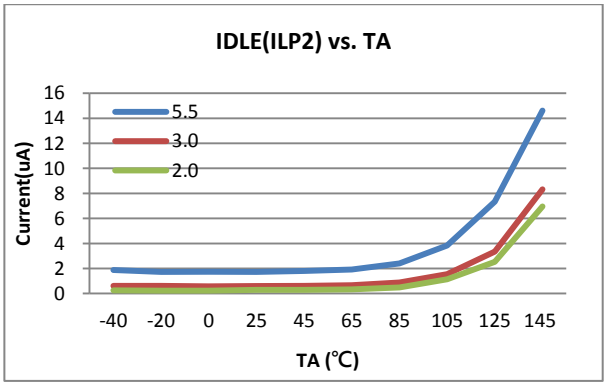


Figure 6.3-6 I_{LP2} vs. Temperature

6.4. Port 1、3

T_A = 25℃,VDD = 3.3V,unless otherwise noted

Sym.	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
Input voltage and Schmitt trigger and leakage current and timing						
V_{IH}	High-Level input voltage				0.7*VDD	V
V_{IL}	Low-Level input voltage		0.3*VDD			
V_{hys}	Input Voltage hysteresis(V_{IH} - V_{IL})			0.3*VDD		V
I_{LKG}	Leakage Current				0.1	uA
R_{PU}	Port pull high resistance			60		kΩ
Output voltage and current and frequency						
V_{OH}	High-level output voltage	VDD=3V, I_{OH}=-10mA,	V_{DD} -0.5			V
		VDD=5V, I_{OH}=-15mA,	V_{DD} -0.5			
V_{OL}	Low-level output voltage	VDD=3V, I_{OL}=10mA			V_{SS} +0.4	
		VDD=5V, I_{OL}=15mA			V_{SS} +0.4	

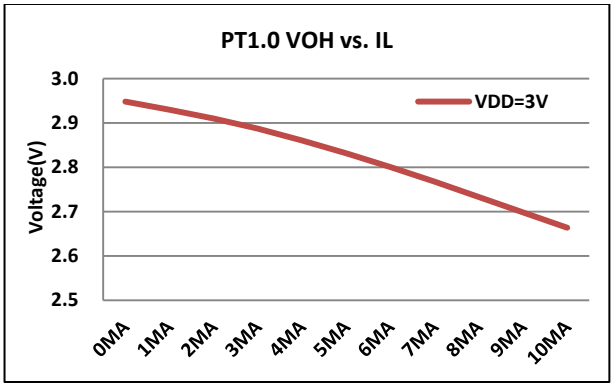


Figure 6.4-1 V_{OH} vs. I_{OH}

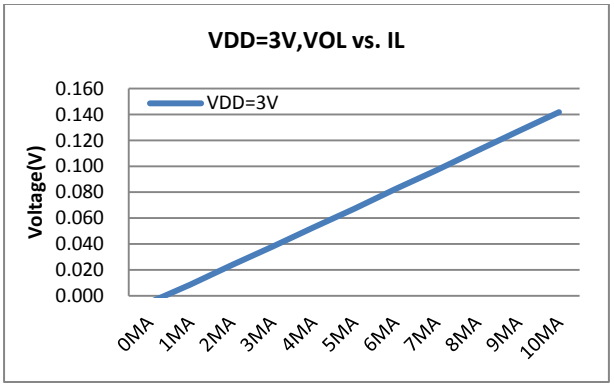


Figure 6.4-2 V_{OL} vs. I_{OL}

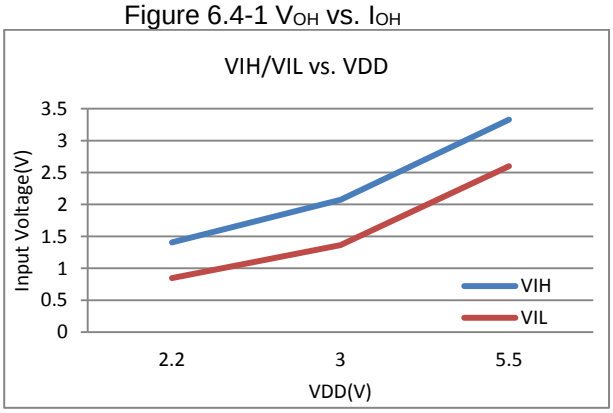


Figure 6.4-3 V_{IH}/V_{IL} vs. VDD

6.5. Port2 and Constant current control circuit

T_A = 25℃,V_{DD1} = 3.0V,unless otherwise noted

Sym.	Parameter	VDD 1	Test Conditions	Min.	Typ.	Max.	Unit
Input voltage and Schmitt trigger and leakage current and timing							
V_{IH}	High-Level input voltage	3				2.1	V
V_{IL}	Low-Level input voltage	3		0.9			
V_{hys}	Input Voltage hysteresis(VIH - VIL)	3			0.4		V
I_{LKG}	Leakage Current	3				0.1	uA
R_{PU}	Port pull high resistance	-			60		kΩ
Output voltage and current							
I_{OH}	Standard GPIO, SEG and COM Source Current	3V	Voh=0.9*VDD	-4	-8		mA
		5V		-8	-15		mA
	COM Sink Current	3V	Vol=0.1*VDD	16	32		mA
		5V		40	80		mA
CC	Constant current level	5V	CCLevel=2'b111		-15		mA
			CCLevel =2'b110		-13		
			CCLevel =2'b101		-11		
			CCLevel =2'b100		-9		
			CCLevel =2'b011		-7		
			CCLevel =2'b010		-5		
			CCLevel =2'b001		-3		
			CCLevel =2'b000		-2		
	Current Skew (Channel)	3V/5V	Vds=0.5V, CCLevel=2'b111		±3		%
	Current Skew (IC)	3V/5V	Vds=0.5V, CCLevel=2'b111		±3		%
	Output Current vs. Output Voltage Regulation	5V	Vds=0.5V~3.5V, CCLevel=2'b111		1		%
	Output Current vs. Supply Voltage Regulation	-	VDD=3.0V~5.5V, VF=2.5V, CCLevel=2'b111		1	3	%

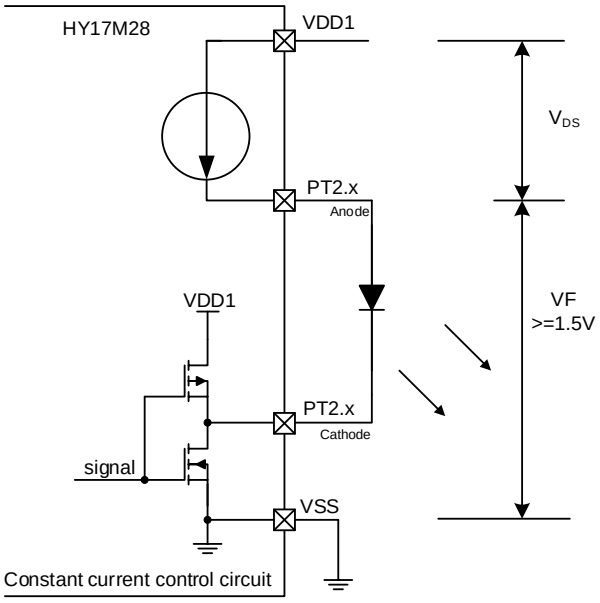


圖 6-11 Constant control circuit 方塊圖

6.6. Reset(Brownout)

T_A = 25℃,V_{DD} = 3.0V,unless otherwise noted

Sym.	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
BOR1	Pulse length needed to accepted reset internally, td-LVR		2			uS
	VDD Start Voltage to accepted reset internally (L➔H),VLVR		1.0	1.35	1.65	V
	BOR1 current, I_{BOR1}			0.1	0.5	uA
	Temperature Drift			15		%
BOR2	Pulse length needed to accepted reset internally, td-LVR		2			us
	V_{DD} Start Voltage to accepted reset internally (L➔H),$V_{HYS2,}$	BOR_TH[2:0]=001b, TA=25°C	-10%	2.0	+10%	V
	V_{DD} Start Voltage to accepted reset internally (H➔L),$V_{LVR2,}$	BOR_TH[2:0]=001b, TA=25°C	-10%	1.96	+10%	V
	Hysteresis, $V_{HYS2-LVR2}$		25	60	90	mV
	VDD Start Voltage to accepted reset internally (H➔L),VLVR2, and BOR_TH[2:0]:	BOR_TH[2:0]=000b	-10%	1.67	+10%	V
		BOR_TH[2:0]=010b	-10%	2.17	+10%	V
		BOR_TH[2:0]=011b	-10%	2.44	+10%	V
		BOR_TH[2:0]=100b	-10%	2.69	+10%	V
		BOR_TH[2:0]=101b	-10%	2.96	+10%	V
		BOR_TH[2:0]=110b	-10%	3.58	+10%	V
		BOR_TH[2:0]=111b	-10%	3.94	+10%	V
	BOR2 current, I_{BOR2}			10	15	uA
	Temperature Drift			3	5	%
MCLR	Pulse length needed as MCLR pin to accepted reset internally, t_{d-RST}		2			us
	Input Voltage to accepted reset voltage			1.1		V
	Reset release voltage			2		V
BOR1/BOR2：Brownout Reset; LVR：Low Voltage Reset of BOR; MCLR：External Reset pin						

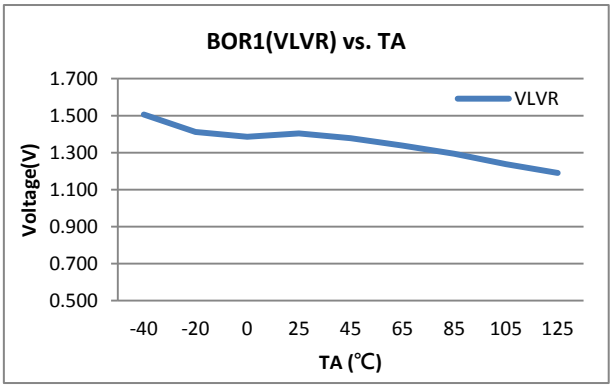


Figure 6.5-1 BOR vs. Temperature

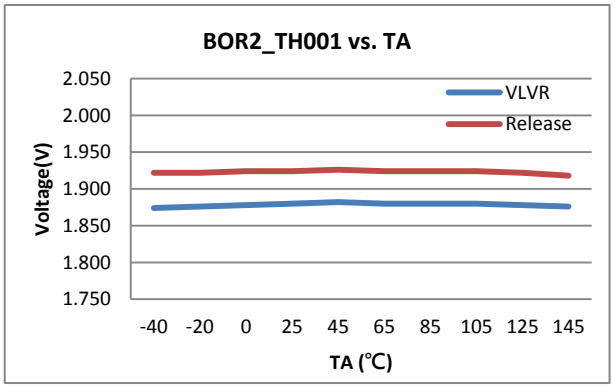


Figure 6.5-2 BOR2 vs. Temperature

6.7. Power System

T_A = 25℃,VDD = 3.3V,unless otherwise noted

Sym.	Parameter	Test Conditions		Min.	Typ.	Max.	Unit
VDDA	VDDA operation current, I_{VDDA}	I_L = 0mA	LDOC[2:0]=000b		20		uA
	Select VDDA output voltage	I_L = 0.1mA, VDD=5.5V	LDOC [2:0]=000b	-5%	2.4	+5%	V
			LDOC [2:0]=001b		2.6		
			LDOC [2:0]=010b		2.9		
			LDOC [2:0]=011b		3.3		
			LDOC [2:0]=100b		3.6		
			LDOC [2:0]=101b		4.0		
			LDOC [2:0]=110b		4.5		
			LDOC [2:0]=111b		5.0		
		I_L = 10mA, VDD=2.6V	LDOC [2:0]=000b	-6%	2.4	+5%	V
	Dropout voltage	VDD=2.9V, VDDA=2.9V mode (LDOC [2:0]=010b), IL = 10mA			200		mV
	Temperature drift	LDOC [2:0]=000b I_L = 0.1mA	T_A=-40℃~85℃		50		PPM/℃
	V_{DD} Voltage drift	LDOC [2:0]=000b	V_{DD}=2.2V~5.5V		±0.2		%/V
REFO	operation current, I_{RERFO}	I_L = 10uA VDDA=2.4V, ENLDO[0]=1b,	ENREFO[0]=1b		50		uA
	output voltage, V_{REFO}		REFOS=00b	-5%	1.2	+5%	V
			REFOS=01b		2.0		V
		VDDA=3.6V, ENLDO[0]=1b,	REFOS=10b		2.4		V
			REFOS=11b		3.0		V
	Output voltage with Load	VDDA=2.4V,	I_L = ±200uA	0.95		1.05	V_{REFO}
	Temperature drift		T_A=-40℃~85℃		50		PPM/℃
	V_{DDA} Voltage drift				100		uV/V
V12	operation current, I_{V12}		ENVCM[0]=1b		50		uA
	Internal V12 buffer voltage, V_{V12}	ENBRG[0]=1b, ENAD1[0]=1b			1.2		V

VDDA：Adjust Voltage Regulator
REFO：Analog common mode voltage
V12：Internal V12 buffer voltage

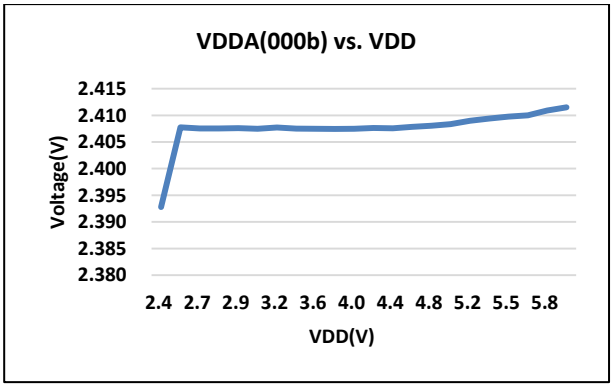


Figure 6.6-1 VDDA(000b) vs. VDD

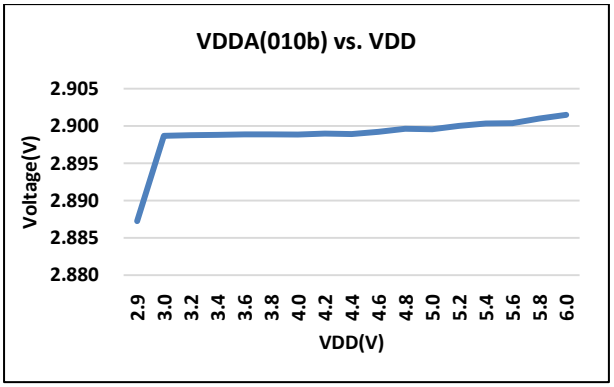


Figure 6.6-2 VDDA(010b) vs. VDD

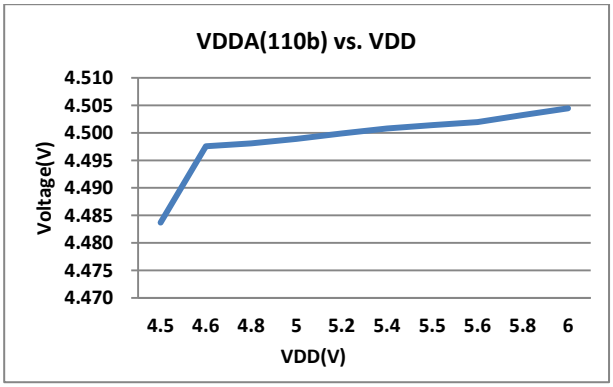


Figure 6.6-3 VDDA(110b) vs. VDD

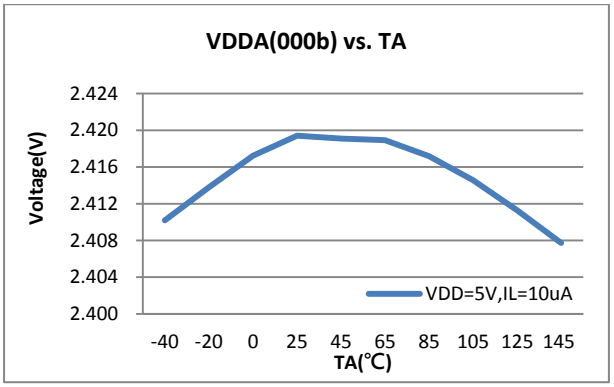


Figure 6.6-4 VDDA(000b) vs. Temperature

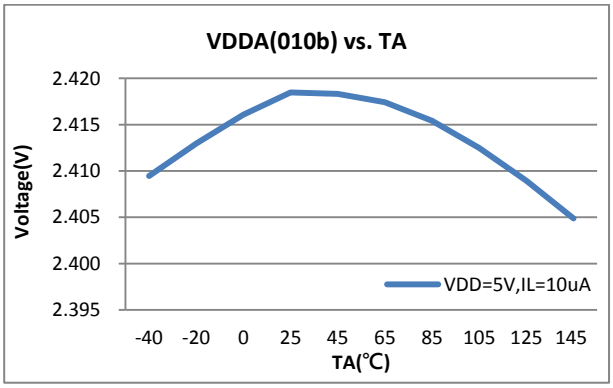


Figure 6.6-5 VDDA(010b) vs. Temperature

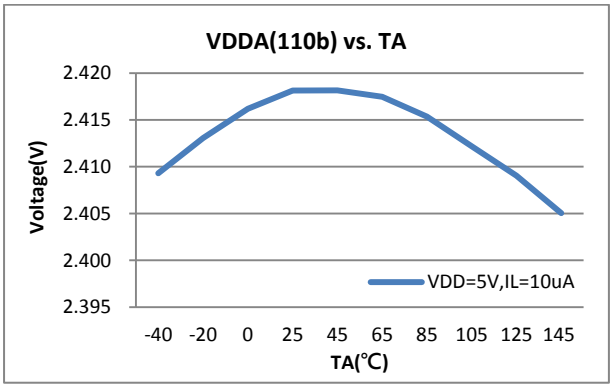


Figure 6.6-6 VDDA(110b) vs. Temperature

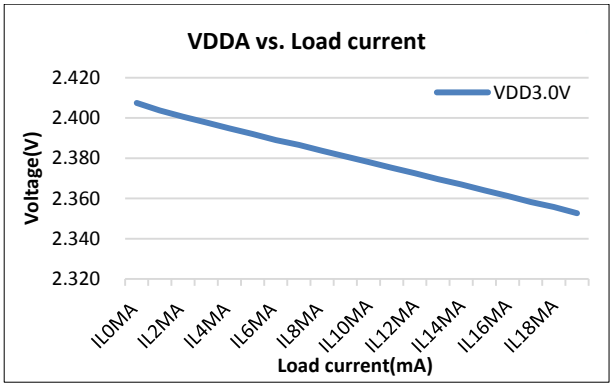


Figure 6.6-7 VDDA vs. Load current

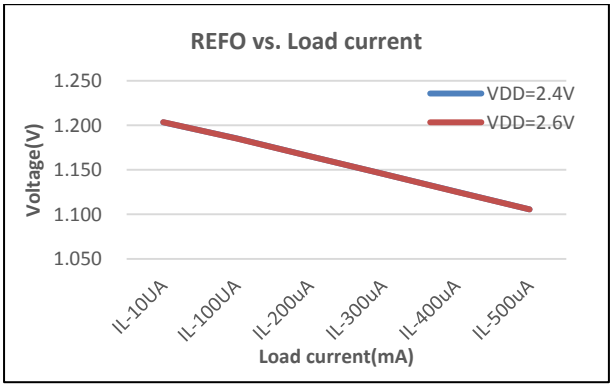


Figure 6.6-8 REFO vs. Load current

6.8. Multi-Comparator

T_A = 25℃,V_{DD} = 3.3V, unless otherwise noted.

Sym.	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
I_{MC}	Operation supply current	ENCMP[0]=1, CMPHS[0]=1b		5		uA
	Low Power Mode	ENCMP[0]=1, CMPHS [0]=0b		1		
V_{IC}	Common-mode input voltage		0		V_{DD}-1	V
V_{accy}	Reference Voltage	ENLDO[0]=1b, CPPS[1:0]=11b, VRSEL[0]=1b	-5%	1.2	5%	V
	Temperature Drift			50		ppm/℃
	VDD Voltage drift			±0.2		%/V
I_R	Multi-node resistor current	CPRL[0]=0b		10		uA
		CPRL[0]=1b		30		
LVD	ENLDO[0]=1b,CPPS[1:0]=11b,CPRH[1:0]=01b,CPRL[0]=0b.	CPDA[4:0]=00001b		4.30		V
		CPDA[4:0]=00010b		4.09		
		CPDA[4:0]=00101b		3.60		
		CPDA[4:0]=00110b		3.46		
		CPDA[4:0]=00111b		3.33		
		CPDA[4:0]=01000b		3.21		
		CPDA[4:0]=01001b		3.10		
		CPDA[4:0]=01010b		3.00		
		CPDA[4:0]=01011b		2.90		
		CPDA[4:0]=01100b		2.81		
		CPDA[4:0]=01101b		2.73		
		CPDA[4:0]=01110b		2.65		
		CPDA[4:0]=01111b		2.57		
		CPDA[4:0]=10000b		2.50		
	CPDA[3:0]=others (reserved)			-		

LVD：Low Voltage Detect.

6.9. Low Noise PGA

TA = 25℃,VDD = 3.3V, VDDA=3.3V,unless otherwise noted

Sym.	Parameter	Test Conditions		Min.	Typ.	Max.	Unit
V_{LNPGA}	Supply Voltage at VDDA	ENLDO[0]=0		2.6		5.5	V
I_{LNPGA}	Operation supply current	ENPGA[0]=1	PGA GAIN =20, ADC_CK=1MHz		500		uA
	Input Noise	0.1Hz ~ 30Hz, Positive and short chop			600		nVrms
	Low noise PGA Gain	PGAG[2:0]=00b			10		
		PGAG[2:0]=01b			20		
		PGAG[1:0]=10b			40		
	Input Leakage	VDD@3.0V, Vin@1.2V 25C			0.1		uA
	PGA input Offset	Vin=short with chopper, PGA=40, ADC Gain=8 VR=V12-VSS OSR=16384=61sps, @25℃			60		uV
	PGA Temperature Offset Coefficient	Vin=short with chopper PGA=40, ADC Gain=8 TA = –40℃ to +85℃			0.25		uV/℃
	PGA Temperature Gain Coefficient	0.7VinMax ~ -0.7VinMax, PGA=40, ADC Gain=8 TA = –40℃ to +85℃			150		PPM/℃

Note:
Mathematical formulas for PGA Temperature Gain Coefficient :
(Goal temperature – 25℃ temperature) / (25℃ temperature)/ (Goal temperature – 25℃ temperature)*10^6

6.10. ADC, Power Supply and recommended operating conditions

TA = 25℃,VDD = 3.3V, VDDA=2.6V,unless otherwise noted

Sym.	Parameter	Test Conditions		Min.	Typ.	Max.	Unit
V_{SD18}	Supply Voltage at VDDA	ENLDO[0]=0		2.6		5.5	V
f_{SD18}	Modulator sample frequency, ADC_CK			125	1000	1200	KHz
	Over Sample Ratio, OSR			64		65536	
I_{SD18}	Operation supply current	ENAD1 [0]=1	GAIN =16, ADC_CK=1MHz		260		uA

6.10.1 ADC Performance

T_A = 25℃,V_{DD}=3.3V,VDDA=2.6V,V_{VR}=(VDDA-VSS)/2,GAIN=1,f_{ADC}=1000KHz,unless otherwise noted

Sym.	Parameter	Test Conditions		Min.	Typ.	Max.	Unit
INL	Integral Nonlinearity(INL)	VDDA=2.6V,V_{VR}= VDDA/2, ΔSI=±450mV			±0.003	±0.01	%FSR
	No Missing Codes[3]	ADC_CK=1000KHz,OSR[3:0]=0000b		23			Bits
G_{SD18}	Temperature drift Gain x16	T_A = -40℃~ 85℃			20		ppm/℃
E_{OS}	Offset error of Full Scale Rang input voltage range with Chopper	ΔAI=0V ΔVR=1.2V DCSET[3:0]=0000b *ΔAI is external short Gain Normalized	Gain=2			1	%FSR
	Offset temperature drift with Chopper mode		GAIN=1		0.125		uV/℃
			GAIN=2		0.127		
			GAIN=4		0.123		
			GAIN=16		0.107		
CM_{SD18}	Common-mode rejection	V_{CM}=0.7V to 1.7V, V_{VR}= 1.0V	V_{SI}=0V, GAIN=1		90		dB
			V_{SI}=0V, GAIN=16		75		dB
PSRR	DC power supply rejection	VDDA=3.0V,ΔVDDA =±100mV, V_{VR}=1.0V, V_{SI}=1.2V,V_{SI-}=1.2V,	GAIN=1	75			dB
			GAIN=16				dB

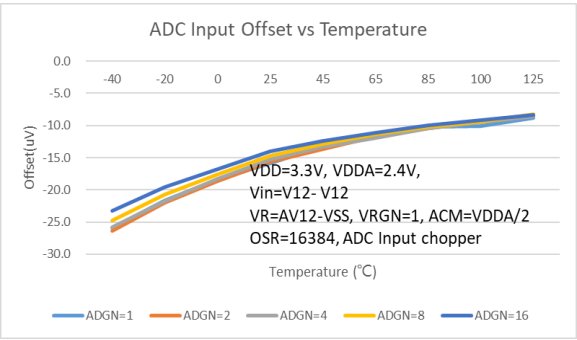


Figure 6.10-1 ADC Offset drift with Temperature

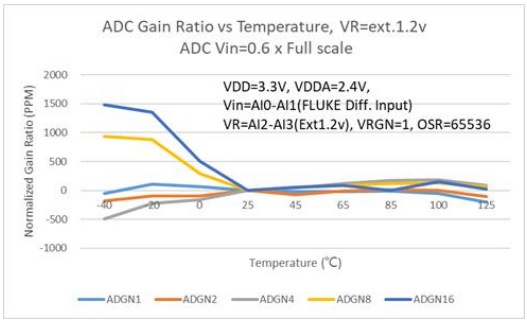


Figure 6.10-2 ADC Gain drift with Temperature

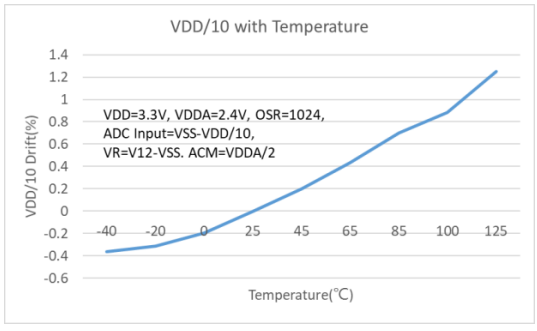


Figure 6.10-3 VDD/10 drift with Temperature

6.10.2 ADC and PGA Noise Performance

Provide important input noise specifications for the ΣΔ ADC and PGA. Table 6.10-1(a)~(c) lists typical noise specifications such as gain, output rate and single-ended maximum input voltage, etc. The test conditions are set on the external input short, chopper mode, and the ADC reference voltage source is using the internal V12 and VSS. Then the equivalent reference voltage is 1.2V, sampling 1024 data.

ENOB(RMS) with OSR/GAIN at A/D Clock=1MHz, VDDA=2.4V, VREF=V12, Chopper Off												
OSR					**64**	**128**	**256**	**512**	**1024**	**2048**	**4096**	**8196**	**16384**	**32768**	**65536**
Output rate(Hz)					**15625**	**7813**	**3906**	**1953**	**977**	**488**	**244**	**122**	**61**	**31**	**15**
Gain	**=**	**PGAGN**	**x**	**ADGN**											
0.25	**=**	**off**	**x**	**0.25**	14.59	16.54	17.07	17.52	17.92	18.5	18.73	19.32	19.88	20.29	20.82
0.5	**=**	**off**	**x**	**0.5**	14.42	16.53	17.12	17.5	17.9	18.49	18.72	19.33	19.87	20.3	20.75
1	**=**	**off**	**x**	**1**	14.19	16.5	16.97	17.44	17.83	18.37	18.66	19.23	19.78	20.3	20.6
2	**=**	**off**	**x**	**2**	13.72	16.35	16.88	17.24	17.71	18.2	18.46	19.03	19.58	20.01	20.49
4	**=**	**off**	**x**	**4**	13.19	16.09	16.6	17.05	17.53	18.05	18.33	18.84	19.35	19.81	20.19
8	**=**	**off**	**x**	**8**	12.47	15.78	16.32	16.7	17.23	17.69	18.11	18.58	19.13	19.51	19.91
16	**=**	**off**	**x**	**16**	11.54	15.32	15.79	16.32	16.94	17.3	17.69	18.19	18.72	19.04	19.54
RMS Noise(uV) with OSR/GAIN at A/D Clock=1MHz, VDDA=2.4V, VREF=V12, Chopper Off															
OSR					**64**	**128**	**256**	**512**	**1024**	**2048**	**4096**	**8196**	**16384**	**32768**	**65536**
Output rate(Hz)					**15625**	**7813**	**3906**	**1953**	**977**	**488**	**244**	**122**	**61**	**31**	**15**
Gain	**=**	**PGAGN**	**x**	**ADGN**											
0.25	**=**	**off**	**x**	**0.25**	392.73	101.09	70.15	51.34	39.01	26.05	22.16	14.71	10.01	7.55	5.22
0.5	**=**	**off**	**x**	**0.5**	219.98	51.10	33.81	26.00	19.74	13.13	11.17	7.31	5.05	3.74	2.75
1	**=**	**off**	**x**	**1**	129.44	26.12	18.81	13.58	10.38	7.13	5.83	3.92	2.69	1.87	1.52
2	**=**	**off**	**x**	**2**	89.39	14.42	9.98	7.80	5.62	4.01	3.34	2.25	1.54	1.14	0.82
4	**=**	**off**	**x**	**4**	64.50	8.64	6.08	4.44	3.20	2.22	1.83	1.29	0.90	0.66	0.50
8	**=**	**off**	**x**	**8**	53.15	5.35	3.69	2.83	1.96	1.43	1.07	0.77	0.52	0.40	0.31
16	**=**	**off**	**x**	**16**	50.69	3.68	2.66	1.84	1.20	0.93	0.71	0.50	0.35	0.28	0.20

Table 6.10-1(a) ADC ENOB and RMS NoiseTable

ENOB(RMS) with OSR/GAIN at A/D Clock=1MHz, VDDA=2.4V, VREF=V12, Chopper On													
OSR					**64**	**128**	**256**	**512**	**1024**	**2048**	**4096**	**8196**	**16384**	**32768**	**65536**
Output rate(Hz)					**5208**	**2604**	**1302**	**651**	**326**	**163**	**122**	**61**	**31**	**15**	**8**
Gain	**=**	**PGAGN**	**x**	**ADGN**											
0.25	**=**	**off**	**x**	**0.25**	15.74	17.05	17.57	18.02	18.5	19.06	19.25	19.95	20.62	20.85	21.53
0.5	**=**	**off**	**x**	**0.5**	15.81	16.98	17.58	18.01	18.37	18.88	19.21	19.83	20.48	20.74	21.42
1	**=**	**off**	**x**	**1**	15.78	16.9	17.42	17.95	18.39	18.8	19.22	19.79	20.29	20.78	21.24
2	**=**	**off**	**x**	**2**	15.69	16.82	17.29	17.75	18.1	18.64	18.96	19.57	20.16	20.6	21.12
4	**=**	**off**	**x**	**4**	15.59	16.51	17.05	17.58	18.04	18.44	18.81	19.36	19.93	20.39	20.9
8	**=**	**off**	**x**	**8**	15.43	16.26	16.75	17.3	17.69	18.29	18.55	19.12	19.6	20.02	20.58
16	**=**	**off**	**x**	**16**	15.04	15.87	16.4	16.84	17.41	17.73	18.19	18.79	19.2	19.73	20.1
ENOB(RMS) with OSR/GAIN at A/D Clock=1MHz, VDDA=2.4V, VREF=V12, Chopper On															
OSR					**64**	**128**	**256**	**512**	**1024**	**2048**	**4096**	**8196**	**16384**	**32768**	**65536**
Output rate(Hz)					**5208**	**2604**	**1302**	**651**	**326**	**163**	**122**	**61**	**31**	**15**	**8**
Gain	**=**	**PGAGN**	**x**	**ADGN**											
0.25	**=**	**off**	**x**	**0.25**	176.92	71.18	49.53	36.39	26.05	17.64	15.52	9.57	6.00	5.12	3.18
0.5	**=**	**off**	**x**	**0.5**	83.93	37.43	24.58	18.29	14.27	10.01	7.97	5.17	3.30	2.75	1.73
1	**=**	**off**	**x**	**1**	43.00	19.72	13.79	9.55	7.01	5.30	3.96	2.67	1.88	1.34	0.98
2	**=**	**off**	**x**	**2**	22.88	10.43	7.54	5.49	4.29	2.95	2.37	1.55	1.03	0.76	0.53
4	**=**	**off**	**x**	**4**	12.24	6.48	4.43	3.08	2.24	1.70	1.32	0.90	0.61	0.44	0.31
8	**=**	**off**	**x**	**8**	6.85	3.85	2.74	1.87	1.42	0.94	0.78	0.53	0.38	0.28	0.19
16	**=**	**off**	**x**	**16**	4.49	2.52	1.75	1.29	0.87	0.69	0.51	0.33	0.25	0.17	0.13

Table 6.10-1(b) ADC ENOB and RMS NoiseTable

ENOB(RMS) with OSR/GAIN at A/D Clock=1MHz, VDDA=2.4V, VREF=V12, Chopper Off													
OSR					**64**	**128**	**256**	**512**	**1024**	**2048**	**4096**	**8196**	**16384**	**32768**	**65536**
Output rate(Hz)					**15625**	**7813**	**3906**	**1953**	**977**	**488**	**244**	**122**	**61**	**31**	**15**
Gain	**=**	**PGAGN**	**x**	**ADGN**											
10	**=**	**10**	**x**	**1**	14.12	15.51	16.34	16.61	16.73	17.33	17.48	17.81	18.31	18.62	18.39
20	**=**	**20**	**x**	**1**	13.94	15.68	16.2	16.54	16.84	17.11	17.37	17.68	17.96	17.74	17.82
40	**=**	**40**	**x**	**1**	14.03	15.52	15.89	16.12	16.04	16.64	16.9	17.07	17.41	17.27	17.29
160	**=**	**10**	**x**	**16**	11.07	12.28	12.78	12.79	12.82	13.39	13.63	13.86	14.38	14.75	14.69
160	**=**	**20**	**x**	**8**	12.06	13.18	13.52	13.76	13.79	14.13	14.39	14.64	15.13	14.97	14.69
160	**=**	**40**	**x**	**4**	12.74	13.8	14.1	14.23	14.23	14.72	14.73	14.99	15.08	15.11	15.13
RMS Noise(uV) with OSR/GAIN at A/D Clock=1MHz, VDDA=2.4V, VREF=V12, Chopper Off															
OSR					**64**	**128**	**256**	**512**	**1024**	**2048**	**4096**	**8196**	**16384**	**32768**	**65536**
Output rate(Hz)					**15625**	**7813**	**3906**	**1953**	**977**	**488**	**244**	**122**	**61**	**31**	**15**
Gain	**=**	**PGAGN**	**x**	**ADGN**											
10	**=**	**10**	**x**	**1**	13.58	5.17	2.92	2.41	2.23	1.46	1.32	1.05	0.74	0.60	0.70
20	**=**	**20**	**x**	**1**	7.67	2.29	1.60	1.27	1.03	0.85	0.71	0.57	0.47	0.55	0.52
40	**=**	**40**	**x**	**1**	3.61	1.28	0.99	0.85	0.90	0.59	0.49	0.44	0.35	0.38	0.38
160	**=**	**10**	**x**	**16**	7.01	3.04	2.14	2.13	2.09	1.41	1.19	1.01	0.71	0.55	0.57
160	**=**	**20**	**x**	**8**	3.54	1.63	1.28	1.09	1.07	0.84	0.70	0.59	0.42	0.47	0.57
160	**=**	**40**	**x**	**4**	2.20	1.06	0.86	0.79	0.78	0.56	0.55	0.46	0.44	0.43	0.42

Table 6.10-1(c) Low noise PGA ENOB and RMS NoiseTable

The RMS Noise are referred to the input. The Effective Number of Bits (ENOB(RMS Bit)) is defined as:

$$\text{ENOB(RMS)} = \ln\left(\frac{\text{FSR}}{\text{RMS Noise}}\right) \Big/ \ln(2)$$

$$\text{RMS Noise} = \left(2 \times \text{VREF} \times \sqrt{\sum_{k=1}^{1024} (\text{ADO}[k] - \text{Average})^2}\right) \Big/ 2^{23}$$

$$\text{Where FSR (Full - Scale Range)} = 2 \times \text{VREF/Gain.}$$

$$\text{Average} = \frac{\sum_{k=1}^{1024} (\text{ADO}[k])}{1024}$$

6.10.3 ADC ,Temperature Sensor

T_A = 25℃,V_{DD} = 3.3V, VDDA=2.6V,unless otherwise noted

Sym.	Parameter	Test Conditions	Min.	Typ.	Max.	unit
TC_S	Sensor temperature drift			173		uV/℃
KT	Absolute Temperature Scale 0°K			-277		℃
TC_{ERR}	One point calibrate error temperature	Calibration at 25℃ of -40℃~85℃		±2		℃

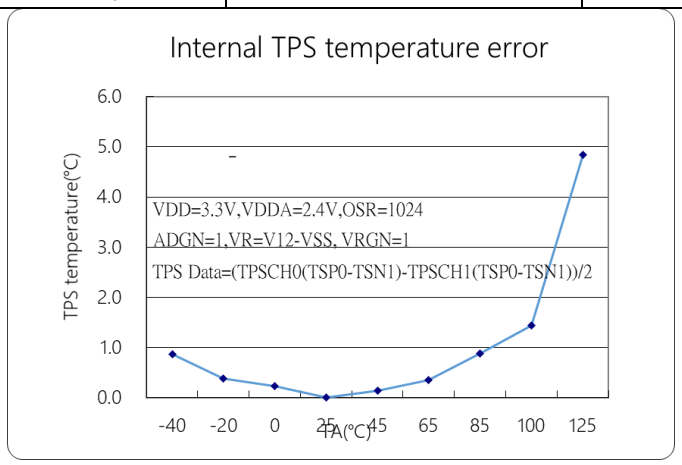


Figure 6.13-1 Internal Temperature Sensor (TPS) temperature error

6.11. MTP Memory

T_A = -40℃~85℃, V_{DD}=3V,unless otherwise noted

Sym.	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
Main MTP Program Memory/ Build-In EEPROM Data Memory						
V_{DD}	Read/Write/Program/Erase Memory Operation supply Voltage		2.75		5.5	V
I_{BIEE}	Read/Write/Program/Erase Memory Operation supply current				22	mA
T_{DART}	Data retention time		10			Years
C_{MAIN}	Endurance cycles at main MTP block		100			Cycles
C_{EEPROM}	Endurance cycles at 32 bytes EEPROM block	EEMODE[1:0]=00b	1.5			k Cycles
	Endurance cycles at 64 bytes EEPROM block	EEMODE[1:0]=01b	0.7			

7. 訂貨資訊

下單品名 1	封裝型式	引腳數	封裝型式		程式碼	出貨包裝	個裝	材料	MSL3
			描述方式		編號 2	形式	數量	組成	
HY17M28-NS32	QFN	32	N	S32	000	Tape & Reel	5000	Green[4]	MSL-3
HY17M28-E028	SSOP	28	E	028	000	Tube	48	Green[4]	MSL-3
HY17M28-E028	SSOP	28	E	028	000	Tape & Reel	2000	Green[4]	MSL-3
HY17M28-ES20	SSOP	20	E	S20	000	Tube	58	Green[4]	MSL-3
HY17M28-ES20	SSOP	20	E	S20	000	Tape & Reel	3000	Green[4]	MSL-3

[1] **產品名稱 品名封裝型式描述方式 裝型程式碼編號 (空白片 / 標準品 / 代客燒錄碼)**

例如：您的需求是 HY17M28 不帶程式碼的空白片且需要的產品是封裝片 QFN32 出貨，則下單品名為 HY17M28-NS32，並請特別註明出貨包裝形式為 Tape & Reel

例如：您的 HY17M28 代客燒錄服務申請的程式碼編號為 009，而需求的產品是封裝片 QFN32 出貨，則下單品名為 HY17M28-NS32-009，並請特別註明出貨包裝形式為 Tape & Reel

例如：您的需求是 HY17M28 不帶程式碼的空白片且需要的產品是封裝片 SSOP28 出貨，則下單品名為 HY17M28-E028，且需以 Tape & Reel 出貨，則除下單品名外，請特別註明出貨包裝形式為 Tape & Reel

例如：您的 HY17M28 代客燒錄服務申請的程式碼編號為 009，而需求的產品是封裝片 SSOP28 出貨，則下單品名為 HY17M28-E028-009，且需以 Tape & Reel 出貨，則除下單品名外，請特別註明出貨包裝形式為 Tape & Reel

[2] 程式碼編號

“001” ~ “999” 為標準品或代客燒錄申請的程式碼編號，而空白晶片不帶此碼。

[3] MSL:

濕度敏感性等級係依據 IPC/JEDEC J-STD-020 的規範加以試驗分級，並參考 IPC/JEDEC J-STD-033 的標準處理、包裝、運輸與使用。

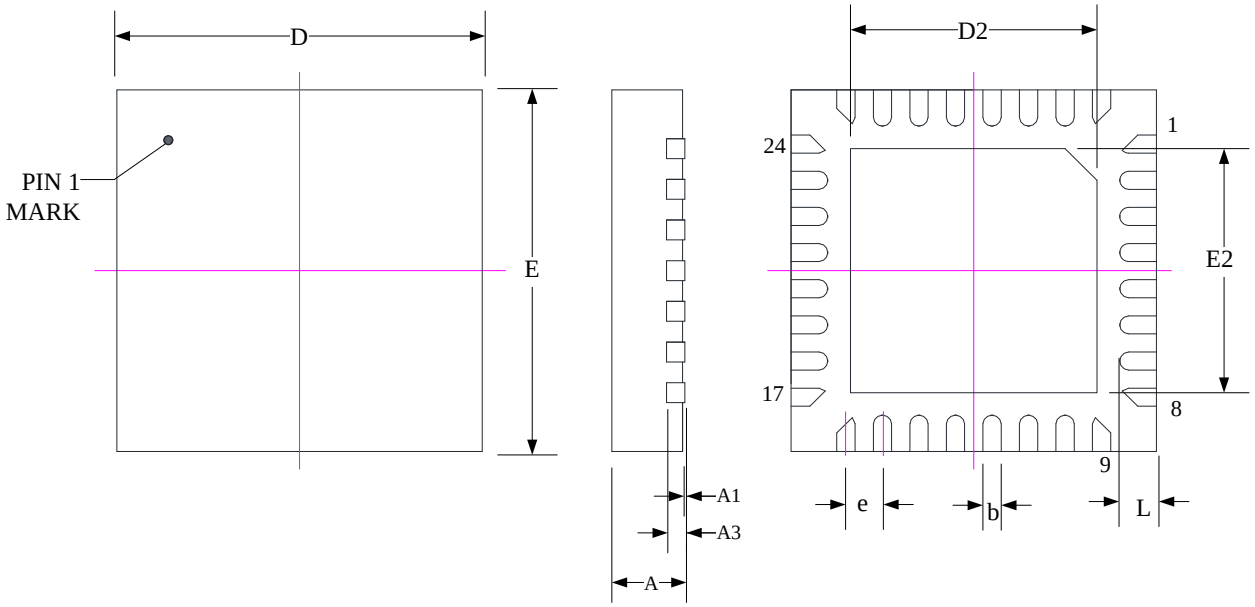
[4] Green (RoHS & no Cl/Br):

HYCON 產品皆為 Green Product，符合 RoHS 指令，REACH 高關注物質(SVHC)以及無鹵素規定 (Br<900ppm or Cl<900ppm or (Br+Cl)<1500ppm)。

8. 封裝型式資訊

8.1. QFN32(NS32)

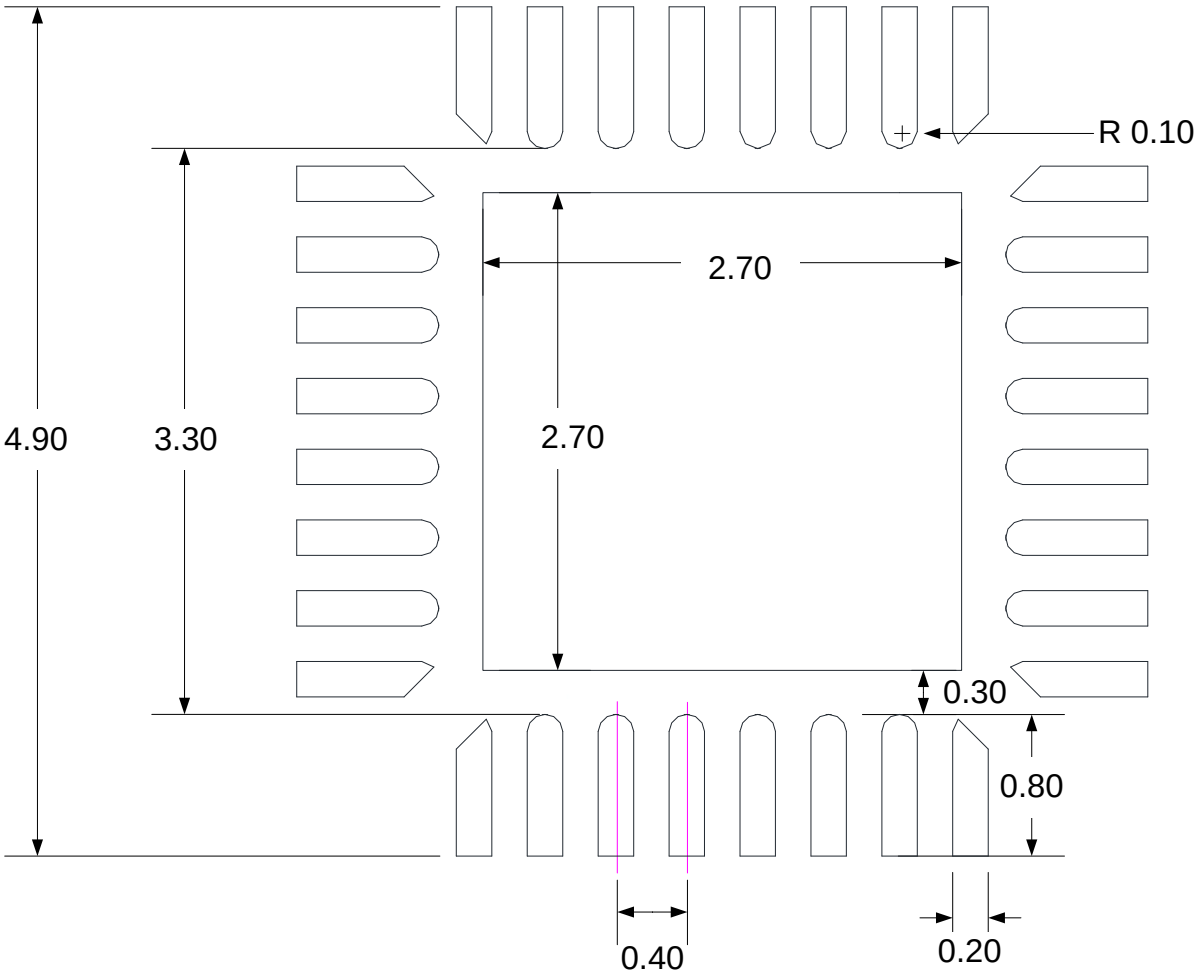
8.1.1. Package Dimensions QFN32(4x4x0.55)



SYMBOLS	MIN	NOM	MAX
A	0.50	0.55	0.60
A1	0.00	0.02	0.05
A3		0.15 REF.	
b	0.15	0.20	0.25
D	3.90	4.00	4.10
E	3.90	4.00	4.10
D2	2.65	2.70	2.75
E2	2.65	2.70	2.75
L	0.25	0.30	0.35
e		0.40 BASIC	

Note:
1. All dimensions refer to JEDEC OUTLINE MO-220.
2. Do not include Mold Flash or Protrusions.
3. Unit: mm.
4. https://www.hycontek.com/hy_mcu/QFN_DFN_PCB.pdf

8.1.2. Land Pattern Design Recommendations

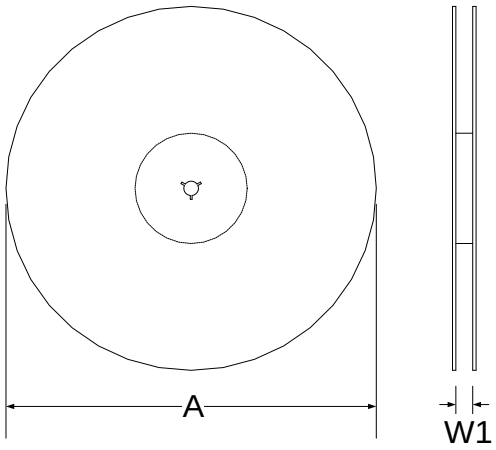


Note:
1. Publication IPC-7351 is recommended for alternate designs.
2. http://www.hycontek.com/hy_mcu/QFN_DFN_PCB.pdf
3. Unit: mm.

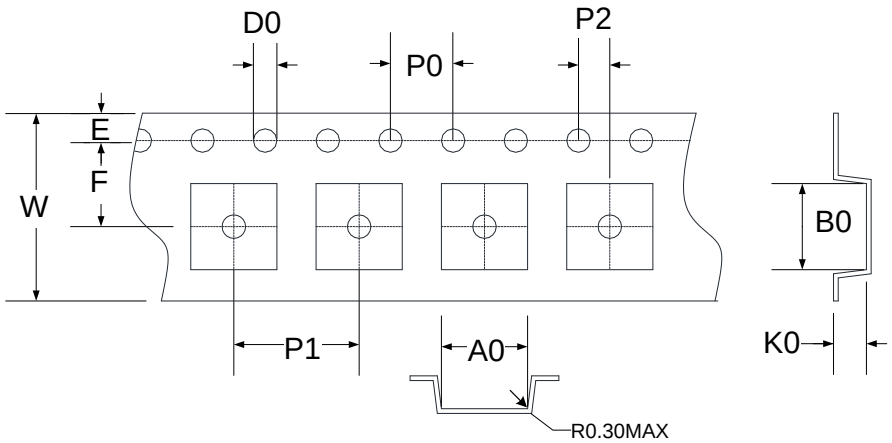
8.1.3. Tape & Reel Information

8.1.3.1. Reel Dimensions

Unit: mm



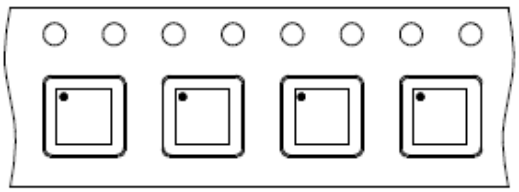
8.1.3.2. Carrier Tape Dimensions



SYMBOLS	Reel Dimensions		Carrier Tape Dimensions									
	A	W1	A0	B0	K0	P0	P1	P2	E	F	D0	W
Spec.	330	12.5	4.35	4.35	1.10	4.00	8.00	2.00	1.75	5.50	1.50	12.00
Tolerance	+6/-3	+1.5/-0	±0.10	±0.10	±0.10	±0.10	±0.10	±0.05	±0.10	±0.05	+0.1/-0	±0.30

Note: 10 Sprocket hole pitch cumulative tolerance is ±0.20mm.

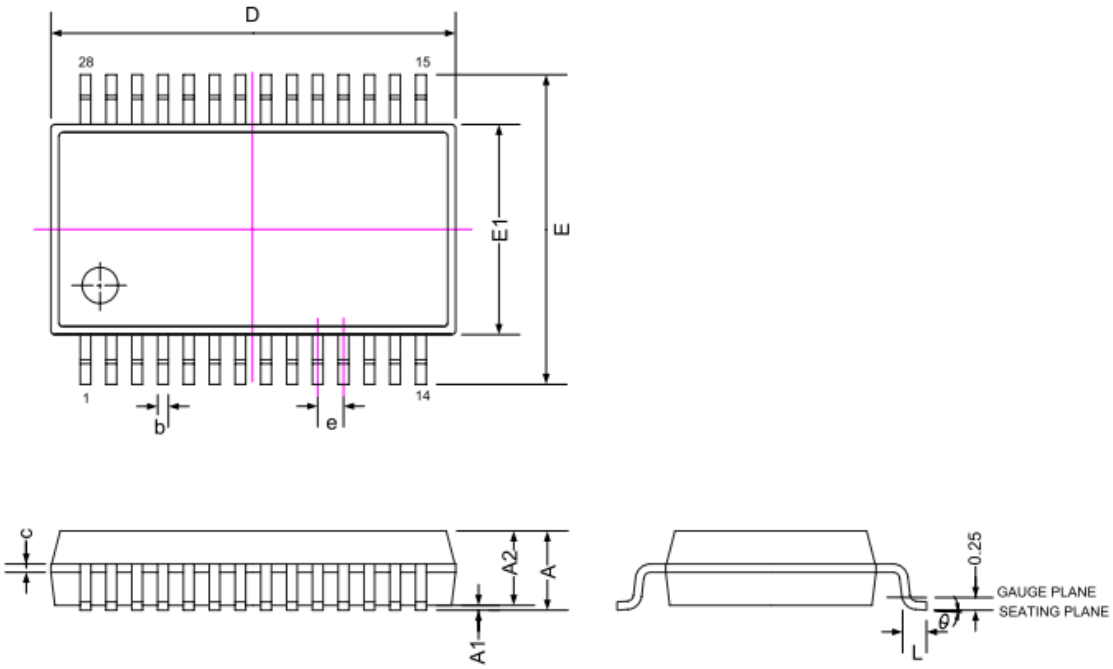
8.1.3.3. Pin1 direction



8.2. SSOP28(E028)

8.2.1. Package Dimensions SSOP28(209mil)

Unit:mm

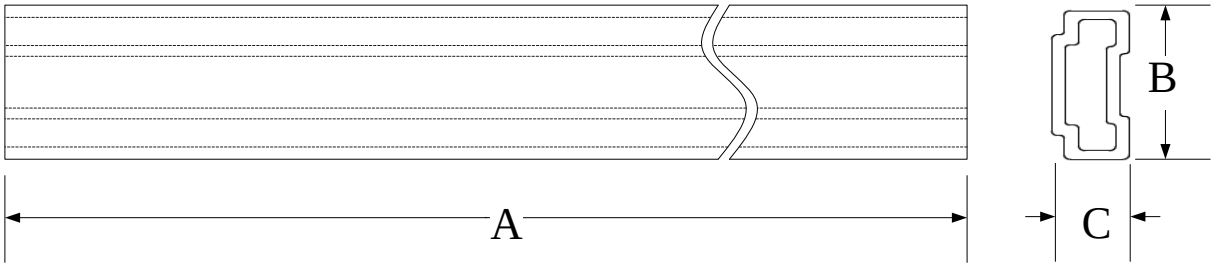


SYMBOLS	MIN	NOM	MAX
A	-	-	2.00
A1	0.05	-	-
A2	1.65	1.75	1.85
b	0.22	-	0.38
c	0.09	-	0.25
D	10.05	10.20	10.50
E1	5.00	5.30	5.60
E	7.65	7.80	7.90
L	0.55	0.75	0.95
e	0.65 BASIC		
θ°	0	4	8

Note:
1. All dimensions refer to JEDEC OUTLINE MO -150.
2. Do not include Mold Flash or Protrusions.
3. Unit: mm.

8.2.2. Tube Dimensions SSOP28(209mil)

Unit : mm

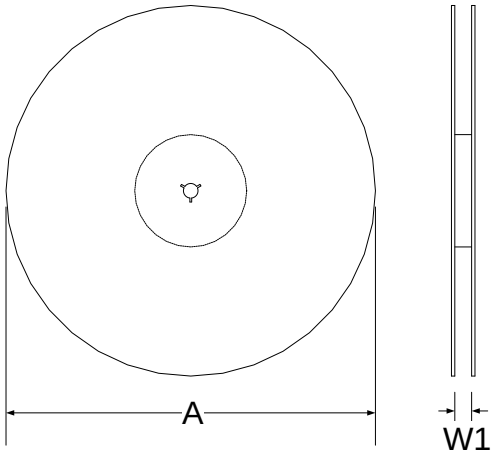


SYMBOLS	A	B	C
Spec.	510±1.5	10.20±0.10	3.75±0.10

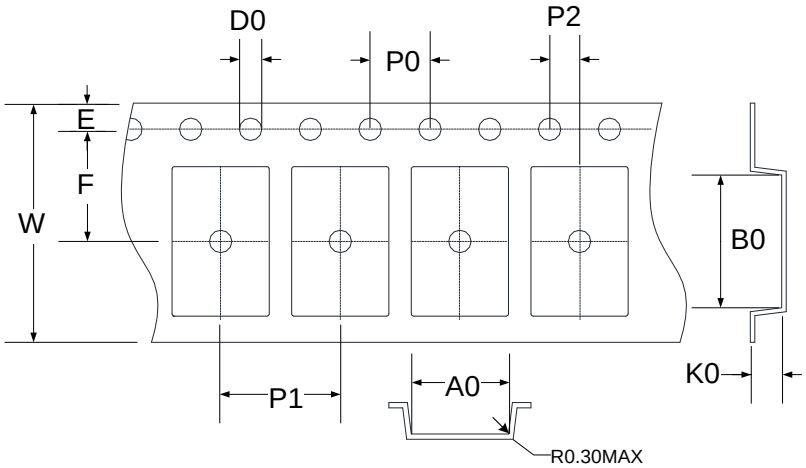
8.2.3. Tape & Reel Information SSOP28(209mil)

Unit : mm

8.2.3.1. Reel Dimensions



8.2.3.2. Carrier Tape Dimensions

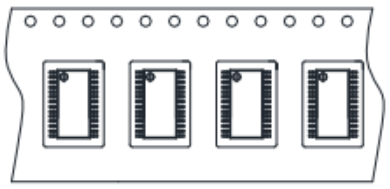


SYMBOLS	Reel Dimensions		Carrier Tape Dimensions									
	A	W1	A0	B0	K0	P0	P1	P2	E	F	D0	W
Spec.	330	24.5	8.40	10.65	2.40	4.00	12.00	2.00	1.75	11.50	1.50	24.00
Tolerance	+6/-3	+1.5/-0	±0.10	±0.10	±0.10	±0.10	±0.10	±0.10	±0.10	±0.10	+0.1/-0	±0.30

Unit: mm

Note: 10 Sprocket hole pitch cumulative tolerance is ±0.20mm.

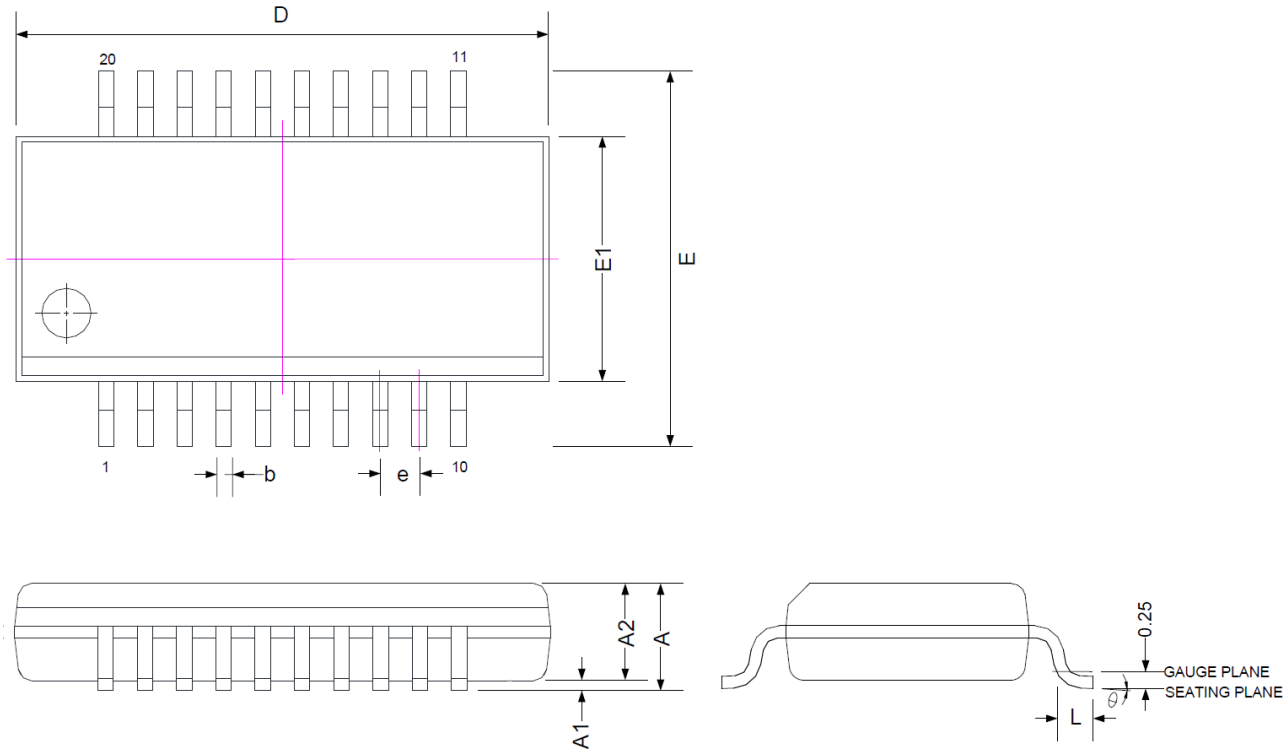
8.2.3.3. Pin1 direction



8.3. SSOP20(ES20)

8.3.1. Package Dimensions SSOP20(150mil)

Unit : mm

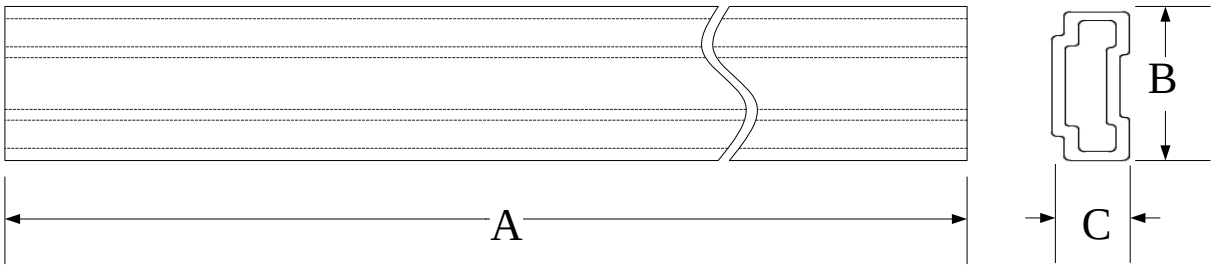


SYMBOLS	MIN	NOM	MAX
A	1.34	1.63	1.75
A1	0.10	0.15	0.25
A2	-	-	1.50
b	0.20	-	0.30
c	0.18	-	0.25
D	8.55	8.66	8.74
E1	3.81	3.91	3.99
E	5.79	5.99	6.20
L	0.41	0.64	1.27
e	0.635 BASIC		
θ°	0	-	8

Note:
1. All dimensions refer to JEDEC OUTLINE MS -137.
2. Do not include Mold Flash or Protrusions.
3. Unit: mm.

8.3.2. Tube Dimensions SSOP20(150mil)

Unit : mm

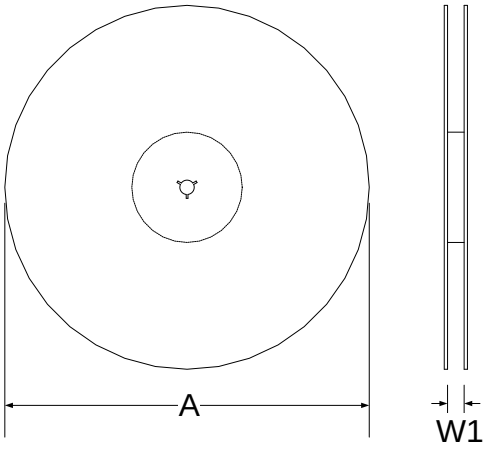


SYMBOLS	A	B	C
Spec.	529.6±1.0	8.001±0.127	3.937±0.127

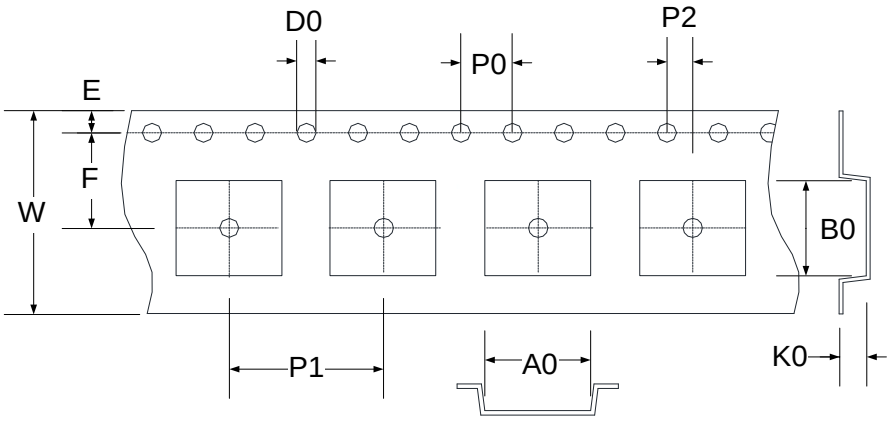
8.3.3. Tape & Reel Information SSOP20(150mil)

Unit : mm

8.3.3.1. Reel Dimensions



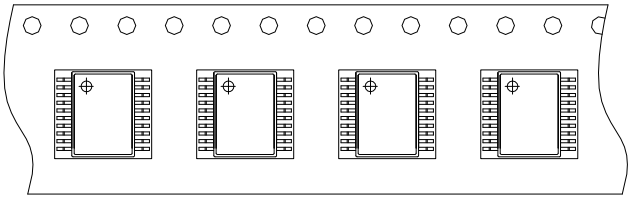
8.3.3.2. Carrier Tape Dimensions



SYMBOLS	Reel Dimensions		Carrier Tape Dimensions									
	A	W1	A0	B0	K0	P0	P1	P2	E	F	D0	W
Spec.	330	16.5	6.50	9.50	2.10	4.00	8.00	2.00	1.75	7.50	1.50	16.00
Tolerance	+6/-3	+1.5/-0	±0.10	±0.10	±0.10	±0.10	±0.10	±0.05	±0.10	±0.10	+0.1/-0	±0.30

Note: 10 Sprocket hole pitch cumulative tolerance is ±0.20mm.

8.3.3.3. Pin1 direction



9. 修訂記錄

以下描述本文件差異較大的地方，而標點符號與字形的改變不在此描述範圍。

文件版次	頁次	日期	摘要
V01	All	2023/07/24	初版發行