HY17M26
Datasheet

8-Bit RISC-like Mixed Signal Microcontroller
Embedded 24-Bit ΣΔADC

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注意：

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7、 本公司一直致力於提高產品的品質和可靠度，但所有的半導體產品都有一定的失效概率，這些失效概率可能會導致一些人身事故、火災事故等。當設計產品時，請充分留意冗餘設計並採用安全指標，這樣可以避免事故的發生。

8、 本規格書中內容，未經本公司許可，嚴禁用於其他目的之轉載或複製。

1. 特點

- **8-Bit RISC-like 微控制器**
  - 具有 71 條高性能指令集 H08D
  - 硬體乘法器及查表器
  - Power On/ Brown Out 1/ Brown Out 2
  - WDT/MCLR Reset
- **工作電壓與操作溫度範圍**
  - VDD = 1.9V ~ 5.5V 數位電路
  - VDDA = 2.4V ~ 5.5V 類比電路
  - - 40°C ~ 85°C 工作溫度
- **記憶體**
  - 8kW MTP 程式記憶體(燒錄次數 100 次)
  - 128 words Build-In EPROM(BIE)資料記憶體(燒錄次數 100 次)
  - 640 bytes SRAM
  - 8L 堆疊
- **24-Bit ΣΔADC 類比數位轉換器**
  - 最高取樣頻率達 1MHz
  - 超取樣頻率設置 64～65536
  - 二/三階梳狀濾波器，轉換頻率 15.6Ksps
  - 信號放大 x1/4, x1/2, x1,x2,x4,x8,x16
  - 全差動輸入信號與測量範圍的零點調整
  - 低溫飄係數與內置絕對溫度傳感器
- **低功耗與低溫飄係數電源系統**
  - VDDA 線性穩壓電源
    - 供應類比電路或外部傳感器電壓源
    - 採可外灌輸入電壓設計
    - 可設置穩壓輸出 2.4V/2.6V/2.9V/3.3V /3.6V /4.0V/4.5V/5.0V
- **通訊介面**
  - 2* I^2C、2* EUART、SPI 通訊介面
  - 2 線式 ICE 與燒錄引腳，支援片上仿真(OCD)及片上燒錄(IAP)功能
- **計時器**
  - Watch Dog
  - 2* 8-bit Timer A, (TMA1/TMA2)
  - 2* 16-bit Timer B, (TMB1/TMB2)
    - 2ch 16-Bit PWM or 4ch 8-bit PWM
  - 2* Timer C 支援波形 Capture 功能 (TMC1/TMC2)
- **低功耗特性**
  - 休眠模式 0.1uA@3.0V
  - 待機模式 0.5uA@3.0V
  - 待機模式下喚醒,支援 HAO 快速啟動功能 (喚醒時間 25uS@2MHz, 3V)
- **Bootloader 更新功能**
  - 支援 Bootloader 線上更新(ISP)功能
- **工作頻率**
  - 內置±2%@25℃高精度 HAO 震盪器 (燒錄器校正後)
  - 內置 HAO 震盪器，共有四種頻率可選：1.843MHz、4.147MHz、8.755MHz、17.51MHz
  - 內置低功耗 LPO 震盪器 14.5KHz
  - 外接石英震盪器 32768Hz ~ 16MHz
- **封裝**
  - SSOP16、SSOP28、QFN32
- **應用領域**
  - 橋式壓力傳感器、類比信號收集器

功能列表

Model No.	VDD (V)	Internal Clock (Hz)	System Clock (Hz)	Program Memory (word)	SRAM (byte)	Built-In EPROM (word)	ADC ENOB (bit x ch)	Sample Rate (sps)	I/O	Timer (bit x ch)	PWM (bit x ch)	Serial Interface (I/F x ch)	Package
HY17M26	1.9~5.5	14.5K 1.843M 4.147M 8.755M 17.51M	14.5K~16M	8K	640	128	21-bit x10	8~15.6K	9xIO	8-bit x 2 16-bit x 2	8-bit x 4 16-bit x 2	EUART x 2 I^2C x 2 SPI x 1	SSOP16
							21-bit x18		21xIO				SSOP28
							21-bit x18		23xIO				QFN32

2. 引腳定義

2.1. 引腳圖

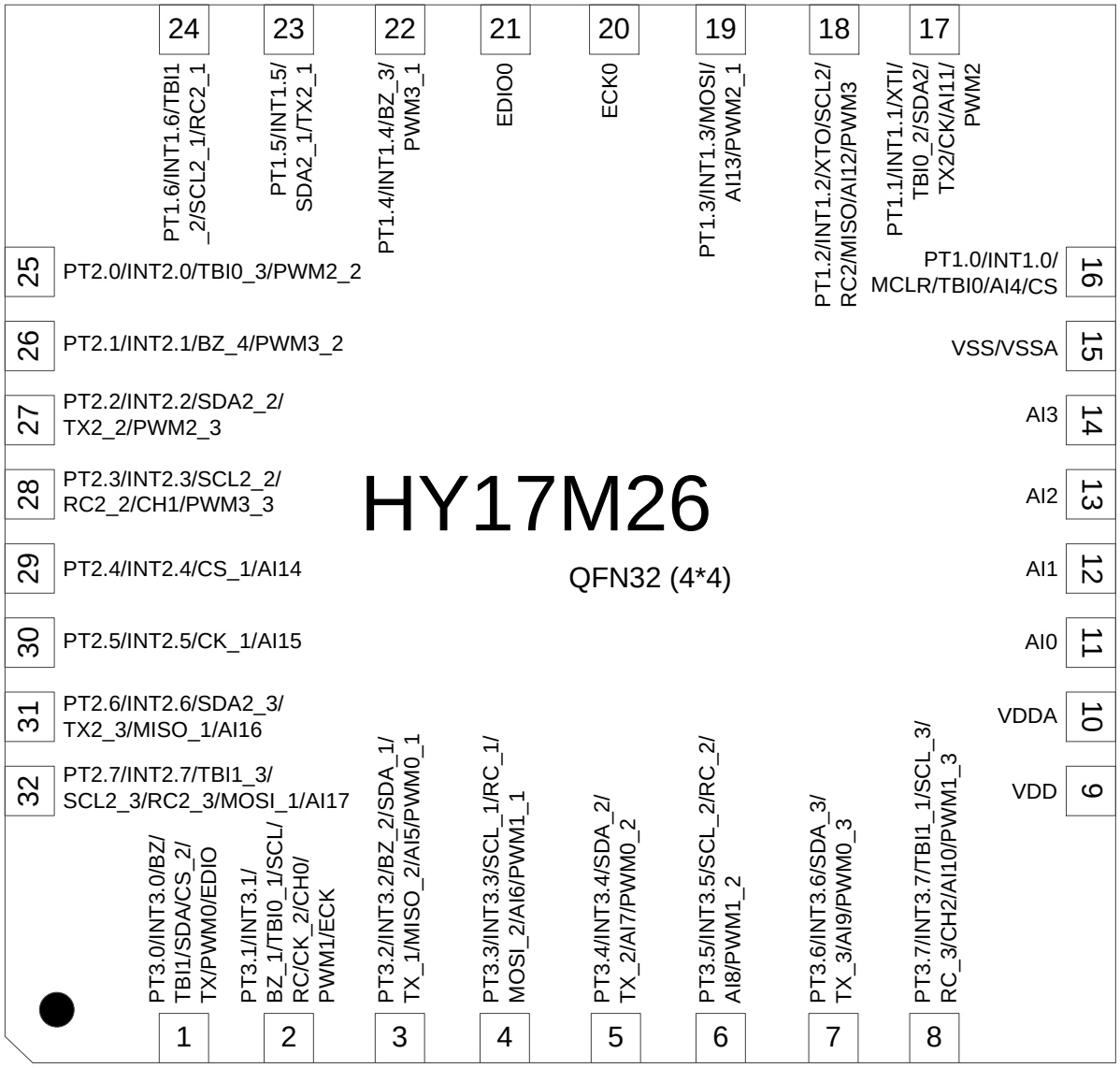


圖 2-1 引腳圖 QFN32(4*4)

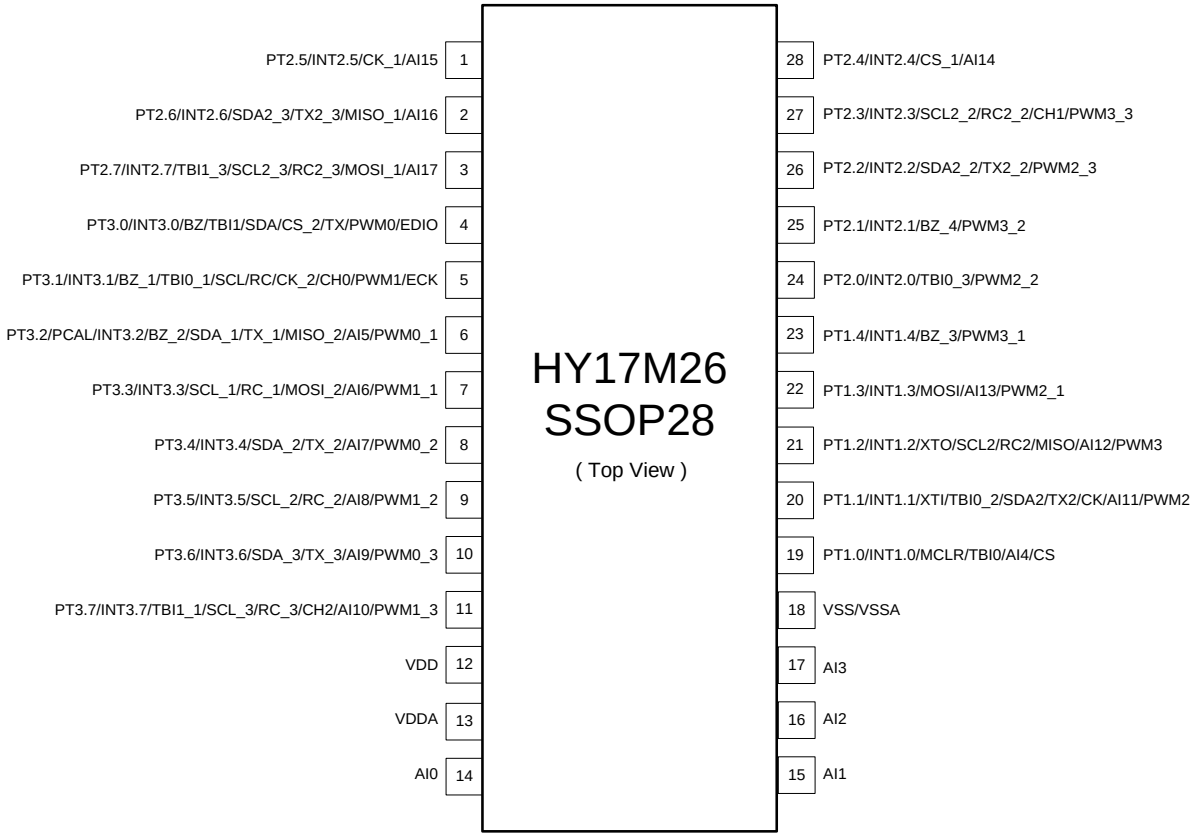


圖 2-2 引腳圖 SSOP28

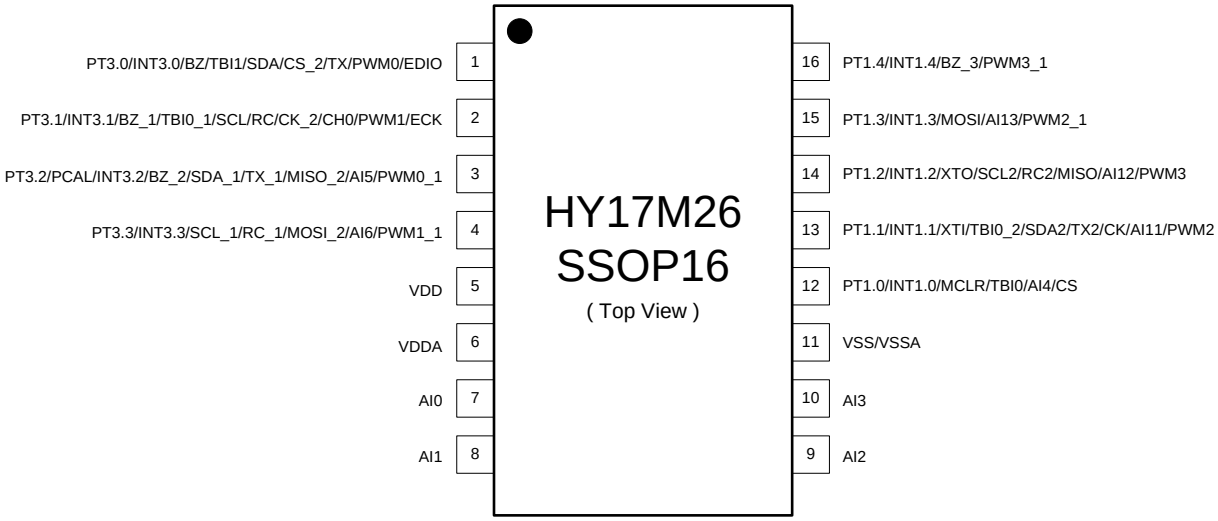


圖 2-3 引腳圖 SSOP16

2.2. I/O 定義與說明

"I/O"輸入/輸出,"I"輸入,"O"輸出,"S"史密斯觸發,"C"CMOS 特性兼容輸出與輸入,"P"電壓源,"A"類比通道

封裝腳位			設計			描述
QFN32	SSOP28	SSOP16	名稱/功能	型式	緩衝	
1	4	1	PT3.0/INT3.0/BZ/TBI1/SDA/CS_2*2/TX/PWM0/EDIO*1			
			PT3.0	I/O	S/C	數位輸入 / 輸出引腳
			INT3.0	I	S	外部中斷源
			BZ	O	C	蜂鳴器輸出端
			TBI1	I	S	TimerB CPI 輸入選擇源
			SDA	I/O	S/C	I²C 通訊數據信號
			TX	O	C	UART 通訊傳送信號
			CS_2*2	I	S	SPI 通訊使能引腳
			PWM0	O	C	PWM0 輸出
			EDIO*1	I/O	S/C	仿真及燒錄之通訊數據腳 EDIO
2	5	2	PT3.1/INT3.1/BZ_1*2/TBI0_1*2/SCL/RC/CK_2*2/CH0/PWM1/ECK*1			
			PT3.1	I/O	S/C	數位輸入 / 輸出引腳
			INT3.1	I	S	外部中斷源
			BZ_1*2	O	C	蜂鳴器輸出端
			TBI0_1*2	I	S	TimerB CPI 輸入選擇源
			SCL	I/O	S/C	I²C 通訊時鐘信號
			RC	I	S	UART 通訊接收信號
			CK_2*2	I/O	S/C	SPI 通訊時鐘引腳
			CH0	A	A	比較器輸入通道
			PWM1	O	C	PWM1 輸出
			ECK*1	I	S	仿真及燒錄之通訊時鐘腳 ECK
3	6	3	PT3.2/PCAL/INT3.2/BZ_2*2/SDA_1*2/TX_1*2/MISO_2*2/AI5/PWM0_1*2			
			PT3.2	I/O	S/C	數位輸入 / 輸出引腳
			PCAL*1	O	C	燒錄用之頻率校正輸出引腳
			INT3.2	I	S	外部中斷源
			BZ_2*2	O	C	蜂鳴器輸出端
			SDA_1*2	I/O	S/C	I²C 通訊數據信號
			TX_1*2	O	C	UART 通訊傳送信號
			MISO_2*2	I/O	S/C	SPI 通訊數據引腳(主機輸入，從機輸出)
			AI5	A	A	類比輸入通道
			PWM0_1*2	O	C	PWM0 輸出

封裝腳位			設計			描述
QFN32	SSOP28	SSOP16	名稱/功能	型式	緩衝	
4	7	4	PT3.3/INT3.3/SCL_1*2/RC_1*2/MOSI_2*2/AI6/PWM1_1*2			
			PT3.3	I/O	S/C	數位輸入 / 輸出引腳
			INT3.3	I	S	外部中斷源
			SCL_1*2	I/O	S/C	I²C 通訊時鐘信號
			RC_1*2	I	S	UART 通訊接收信號
			MOSI_2*2	I/O	S/C	SPI 通訊數據引腳(主機輸出，從機輸入)
			AI6	A	A	類比輸入通道
			PWM1_1*2	O	C	PWM1 輸出
5	8	-	PT3.4/INT3.4/TCI1_2*2/SDA_2*2/TX_2*2/AI7/PWM0_2*2			
			PT3.4	I/O	S/C	數位輸入 / 輸出引腳
			INT3.4	I	S	外部中斷源
			TCI1_2*2	I	S	Timer C 輸入引腳
			SDA_2*2	I/O	S/C	I²C 通訊數據信號
			TX_2*2	O	C	UART 通訊傳送信號
			AI7	A	A	類比輸入通道
			PWM0_2*2	O	C	PWM0 輸出
6	9	-	PT3.5/INT3.5/TCI2_2*2/SCL_2*2/RC_2*2/AI8/PWM1_2*2			
			PT3.5	I/O	S/C	數位輸入 / 輸出引腳
			INT3.5	I	S	外部中斷源
			TCI2_2*2	I	S	Timer C 輸入引腳
			SCL_2*2	I/O	S/C	I²C 通訊時鐘信號
			RC_2*2	I	S	UART 通訊接收信號
			AI8	A	A	類比輸入通道
			PWM1_2*2	O	C	PWM1 輸出
7	10	-	PT3.6/INT3.6/TBI2_2*2/SDA_3*2/TX_3*2/AI9/PWM0_3*2			
			PT3.6	I/O	S/C	數位輸入 / 輸出引腳
			INT3.6	I	S	外部中斷源
			TBI2_2*2	I	S	TimerB CPI 輸入選擇源
			SDA_3*2	I/O	S/C	I²C 通訊數據信號
			TX_3*2	O	C	UART 通訊傳送信號
			AI9	A	A	類比輸入通道
			PWM0_3*2	O	C	PWM0 輸出
8	11	-	PT3.7/INT3.7/TBI1_1*2/SCL_3*2/RC_3*2/CH2/AI10/PWM1_3*2			
			PT3.7	I/O	S/C	數位輸入 / 輸出引腳

封裝腳位			設計			描述
QFN32	SSOP28	SSOP16	名稱/功能	型式	緩衝	
			INT3.7	I	S	外部中斷源
			TBI1_1*2	I	S	TimerB CPI 輸入選擇源
			SCL_3*2	I/O	S/C	I²C 通訊時鐘信號
			RC_3*2	I	S	UART 通訊接收信號
			CH2	A	A	比較器輸入通道
			AI10	A	A	類比輸入通道
			PWM1_3*2	O	C	PWM1 輸出
9	12	5	VDD	P	P	晶片工作電壓源接正端引腳, 需外接 10uF 電容至 VSS.
10	13	6	VDDA	P	P	LDO 線性穩壓電源輸出引腳,啟動輸出時需外接 1uF 電容至 VSS.
11	14	7	AI0	A	A	類比輸入通道
12	15	8	AI1	A	A	類比輸入通道
13	16	9	AI2	A	A	類比輸入通道
14	17	10	AI3	A	A	類比輸入通道
15	18	11	VSS	P	P	晶片工作電壓源接地端引腳
15	18	11	VSSA	P	P	晶片類比電壓源接地端引腳
16	19	12	PT1.0/INT1.0/MCLR/TBI0/AI4/CS			
			PT1.0	I/O	S/C	數位輸入 / 輸出引腳
			INT1.0	I	S	外部中斷源
			MCLR	I	S	低電位有效，帶內部上拉電阻
			TBI0	I	S	TimerB CPI 輸入選擇源
			CS	I	S	SPI 通訊使能引腳
			AI4	A	A	類比輸入通道
17	20	13	PT1.1/INT1.1/XTI/TBI0_2*2/SDA2/TX2/CK/AI11/PWM2			
			PT1.1	I/O	S/C	數位輸入 / 輸出引腳
			INT1.1	I	S	外部中斷源
			XTI	A	A	外接震盪器輸入端
			TBI0_2*2	I	S	TimerB CPI 輸入選擇源
			SDA2	I/O	S/C	第二組 I2C 通訊數據信號
			TX2	O	C	第二組 UART 通訊傳送信號
			CK	I/O	S/C	SPI 通訊時鐘引腳
			AI11	A	A	類比輸入通道
			PWM2	O	C	PWM2 輸出

封裝腳位			設計			描述
QFN32	SSOP28	SSOP16	名稱/功能	型式	緩衝	
18	21	14	PT1.2/INT1.2/XTO/TBI2/SCL2/RC2/MISO/AI12/PWM3			
			PT1.2	I/O	S/C	數位輸入 / 輸出引腳
			INT1.2	I	S	外部中斷源
			XTO	A	A	外接震盪器輸出端
			TBI2	I	S	TimerB CPI 輸入選擇源
			SCL2	I/O	S/C	第二組 I²C 通訊時鐘信號
			RC2	I	S	第二組 UART 通訊接收信號
			MISO	I/O	S/C	SPI 通訊數據引腳(主機輸入，從機輸出)
			AI12	A	A	類比輸入通道
			PWM3	O	C	PWM3 輸出
19	22	15	PT1.3/INT1.3/TCI1/MOSI/AI13/PWM2_1*2			
			PT1.3	I/O	S/C	數位輸入 / 輸出引腳
			INT1.3	I	S	外部中斷源
			TCI1	I	S	Timer C 輸入引腳
			MOSI	I/O	S/C	SPI 通訊數據引腳(主機輸出，從機輸入)
			AI13	A	A	類比輸入通道
			PWM2_1*2	O	C	PWM2 輸出
20	-	-	ECK0	I	S	仿真及燒錄之通訊時鐘腳 ECK0
21	-	-	EDIO0	I/O	S/C	仿真及燒錄之通訊數據腳 EDIO0
22	23	16	PT1.4/INT1.4/TCI2/BZ_3/PWM3_1*2			
			PT1.4	I/O	S/C	數位輸入 / 輸出引腳
			INT1.4	I	S	外部中斷源
			TCI2	I	S	Timer C 輸入引腳
			BZ_3	O	C	蜂鳴器輸出端
			PWM3_1*2	O	C	PWM3 輸出
23	-	-	PT1.5/INT1.5/SDA2_1*2/TX2_1*2			
			PT1.5	I/O	S/C	數位輸入 / 輸出引腳
			INT1.5	I	S	外部中斷源
			SDA2_1*2	I/O	S/C	第二組 I²C 通訊數據信號
			TX2_1*2	O	C	第二組 UART 通訊傳送信號
24	-	-	PT1.6/INT1.6/TBI1_2*2/SCL2_1*2/RC2_1*2			
			PT1.6	I/O	S/C	數位輸入 / 輸出引腳
			INT1.6	I	S	外部中斷源
			TBI1_2*2	I	S	TimerB CPI 輸入選擇源

封裝腳位			設計			描述
QFN32	SSOP28	SSOP16	名稱/功能	型式	緩衝	
			SCL2_1*2	I/O	S/C	第二組 I²C 通訊時鐘信號
			RC2_1*2	I	S	第二組 UART 通訊接收信號
25	24	-	PT2.0/INT2.0/TBI0_3*2/PWM2_2*2			
			PT2.0	I/O	S/C	數位輸入 / 輸出引腳
			INT2.0	I	S	外部中斷源
			TBI0_3*2	I	S	TimerB CPI 輸入選擇源
			PWM2_2*2	O	C	PWM2 輸出
26	25	-	PT2.1/INT2.1/BZ_4*2/PWM3_2*2			
			PT2.1	I/O	S/C	數位輸入 / 輸出引腳
			INT2.1	I	S	外部中斷源
			BZ_4*2	O	C	蜂鳴器輸出端
			PWM3_2*2	O	C	PWM3 輸出
27	26	-	PT2.2/INT2.2/TCI1_1*2/SDA2_2*2/TX2_2*2/PWM2_3*2			
			PT2.2	I/O	S/C	數位輸入 / 輸出引腳
			INT2.2	I	S	外部中斷源
			TCI1_1*2	I	S	Timer C 輸入引腳
			SDA2_2*2	I/O	S/C	第二組 I²C 通訊數據信號
			TX2_2*2	O	C	第二組 UART 通訊傳送信號
			PWM2_3*2	O	C	PWM2 輸出
28	27	-	PT2.3/INT2.3/TCI2_1*2/SCL2_2*2/RC2_2*2/CH1/PWM3_3*2			
			PT2.3	I/O	S/C	數位輸入 / 輸出引腳
			INT2.3	I	S	外部中斷源
			TCI2_1*2	I	S	Timer C 輸入引腳
			SCL2_2*2	I/O	S/C	第二組 I²C 通訊時鐘信號
			RC2_2*2	I	S	第二組 UART 通訊接收信號
			CH1	A	A	類比輸入通道
			PWM3_3*2	O	C	PWM3 輸出
29	28	-	PT2.4/INT2.4/TBI2_1*2/CS_1*2/AI14			
			PT2.4	I/O	S/C	數位輸入 / 輸出引腳
			INT2.4	I	S	外部中斷源
			TBI2_1*2	I	S	TimerB CPI 輸入選擇源
			CS_1*2	I	S	SPI 通訊使能引腳
			AI14	A	A	類比輸入通道
30	1	-	PT2.5/INT2.5/CK_1*2/AI15			

封裝腳位			設計			描述
QFN32	SSOP28	SSOP16	名稱/功能	型式	緩衝	
			PT2.5	I/O	S/C	數位輸入 / 輸出引腳
			INT2.5	I	S	外部中斷源
			CK_1*2	I/O	S/C	SPI 通訊時鐘引腳
			AI15	A	A	類比輸入通道
31	2	-	PT2.6/INT2.6/SDA2_3*2/TX2_3*2/MISO_1*2/AI16			
			PT2.6	I/O	S/C	數位輸入 / 輸出引腳
			INT2.6	I	S	外部中斷源
			SDA2_3*2	I/O	S/C	第二組 I²C 通訊數據信號
			TX2_3*2	O	C	第二組 UART 通訊傳送信號
			MISO_1*2	I/O	S/C	SPI 通訊數據引腳(主機輸入，從機輸出)
			AI16	A	A	類比輸入通道
32	3	-	PT2.7/INT2.7/TBI1_3*2/SCL2_3*2/RC2_3*2/MOSI_1*2/AI17			
			PT2.7	I/O	S/C	數位輸入 / 輸出引腳
			INT2.7	I	S	外部中斷源
			TBI1_3*2	I	S	TimerB CPI 輸入選擇源
			SCL2_3*2	I/O	S/C	第二組 I²C 通訊時鐘信號
			RC2_3*2	I	S	第二組 UART 通訊接收信號
			MOSI_1*2	I/O	S/C	SPI 通訊數據引腳(主機輸出，從機輸入)
			AI17	A	A	類比輸入通道

[1] 仿真 ICE 與燒錄時用的引腳，該模式下 GPIO 複用功能無法使用。

該模式下連線控制器會有開關電源 VDD 行為，電路上 VDD 不可有較重的負載或連接較大電容。

[2] 經由晶片內部設置，可規劃複用引腳功能在該引腳輸出或輸入。*表示為複用選擇的腳位。

表 2-1 引腳編號與說明

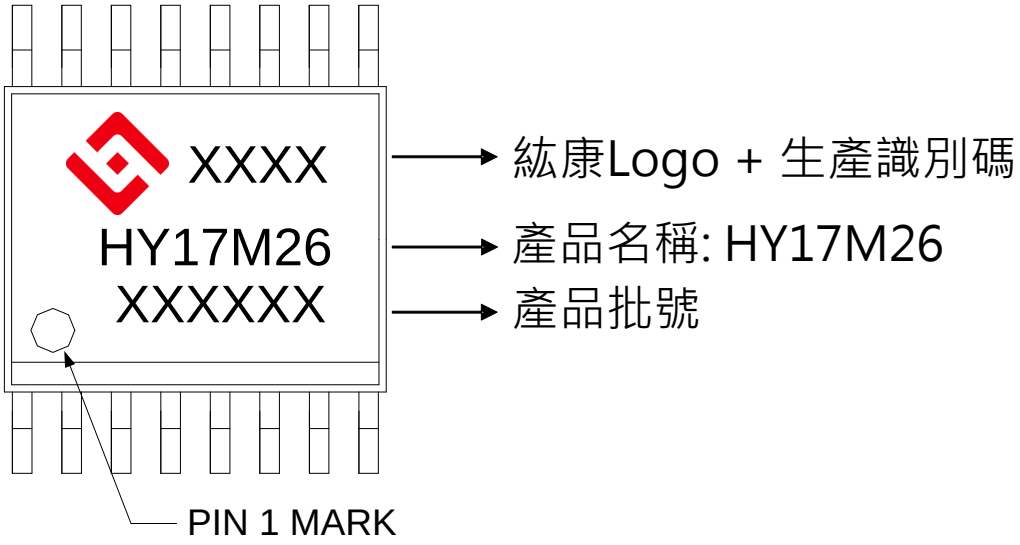
2.3. 復用引腳定義說明

Function	I/O Type	INT	Internal Pull high	Special Function	Buzzer	Timer B/C Enable, Input	I²C	UART	SPI	Comparator	Analog	PWM
AI0	AI	-	-	-	-	-	-	-	-	-	AI0	-
AI1	AI	-	-	-	-	-	-	-	-	-	AI1	-
AI2	AI	-	-	-	-	-	-	-	-	-	AI2	-
AI3	AI	-	-	-	-	-	-	-	-	-	AI3	-
PT1.0	DAI/O	INT1.0	PU1.0	MCLR	-	TBI0	-	-	CS	-	AI4	-
PT1.1	DAI/O	INT1.1	PU1.1	XTI	-	TBI0_2	SDA2	TX2	CK	-	AI11	PWM2
PT1.2	DAI/O	INT1.2	PU1.2	XTO	-	TBI2	SCL2	RC2	MISO	-	AI12	PWM3
PT1.3	DAI/O	INT1.3	PU1.3	-	-	TCI1	-	-	MOSI	-	AI13	PWM2_1
PT1.4	DI/O	INT1.4	PU1.4	-	BZ_3	TCI2	-	-	-	-	-	PWM3_1
PT1.5	DI/O	INT1.5	PU1.5	-	-	-	SDA2_1	TX2_1	-	-	-	-
PT1.6	DI/O	INT1.6	PU1.6	-	-	TBI1_2	SCL2_1	RC2_1	-	-	-	-
PT2.0	DI/O	INT2.0	PU2.0	-	-	TBI0_3	-	-	-	-	-	PWM2_2
PT2.1	DI/O	INT2.1	PU2.1	-	BZ_4	-	-	-	-	-	-	PWM3_2
PT2.2	DI/O	INT2.2	PU2.2	-	-	TCI1_1	SDA2_2	TX2_2	-	-	-	PWM2_3
PT2.3	DAI/O	INT2.3	PU2.3	-	-	TCI2_1	SCL2_2	RC2_2	-	CH1	-	PWM3_3
PT2.4	DAI/O	INT2.4	PU2.4			TBI2_1			CS_1		AI14	
PT2.5	DAI/O	INT2.5	PU2.5						CK_1		AI15	
PT2.6	DAI/O	INT2.6	PU2.6				SDA2_3	TX2_3	MISO_1		AI16	
PT2.7	DAI/O	INT2.7	PU2.7			TBI1_3	SCL2_3	RC2_3	MOSI_1		AI17	
PT3.0	DI/O	INT3.0	PU3.0	EDIO	BZ	TBI1	SDA	TX	CS_2			PWM0
PT3.1	DAI/O	INT3.1	PU3.1	ECK	BZ_1	TBI0_1	SCL	RC	CK_2	CH0		PWM1
PT3.2	DAI/O	INT3.2	PU3.2	PCAL	BZ_2	-	SDA_1	TX_1	MISO_2	-	AI5	PWM0_1
PT3.3	DAI/O	INT3.3	PU3.3	-	-	-	SCL_1	RC_1	MOSI_2	-	AI6	PWM1_1
PT3.4	DAI/O	INT3.4	PU3.4	-	-	TCI1_2	SDA_2	TX_2	-	-	AI7	PWM0_2
PT3.5	DAI/O	INT3.5	PU3.5	-	-	TCI2_2	SCL_2	RC_2	-	-	AI8	PWM1_2
PT3.6	DAI/O	INT3.6	PU3.6	-	-	TBI2_2	SDA_3	TX_3	-	-	AI9	PWM0_3
PT3.7	DAI/O	INT3.7	PU3.7	-	-	TBI1_1	SCL_3	RC_3	-	CH2	AI10	PWM1_3
ECK0	DI/O	-	-	ECK0	-	-	-	-	-	-	-	-
EDIO0	DI/O	-	-	EDIO0	-	-	-	-	-	-	-	-

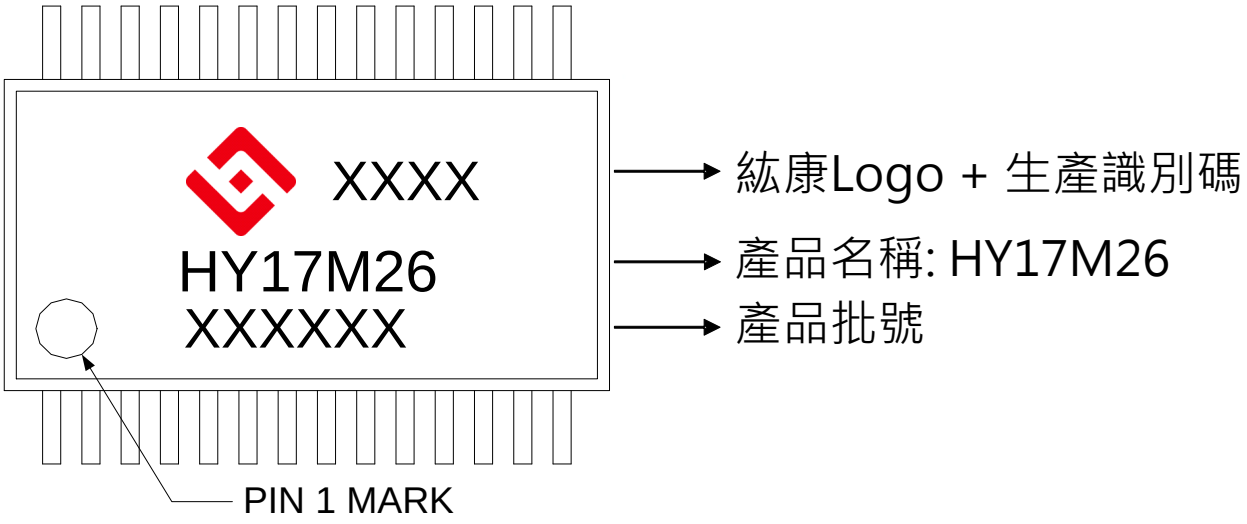
表 2-2 引腳編號與說明

2.4. 封裝片標記信息

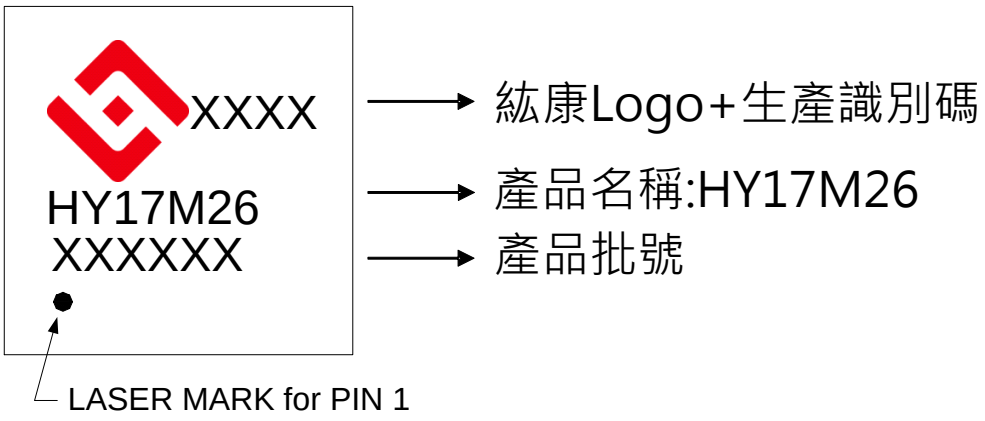
2.4.1. SSOP16 封裝片標記信息



2.4.2. SSOP28 封裝片標記信息



2.4.3. QFN32 封裝片標記信息



3. 應用電路

3.1. 壓力感測應用

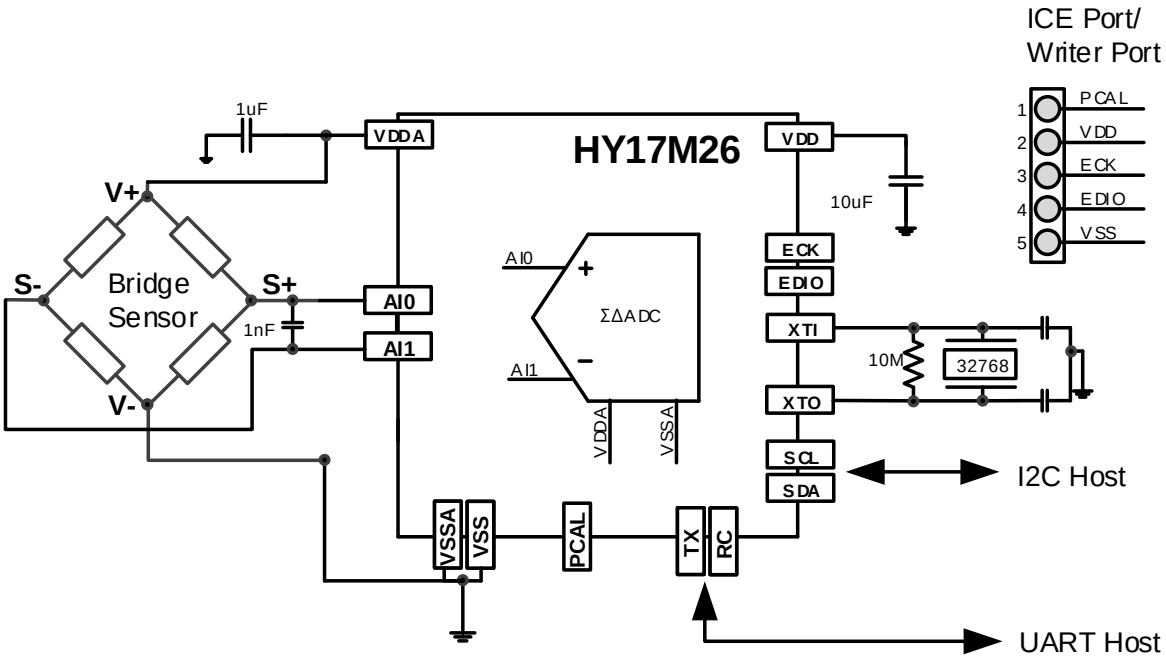


圖 3-1 壓力感測應用參考電路

4. Function Outline

4.1. 內部方塊圖

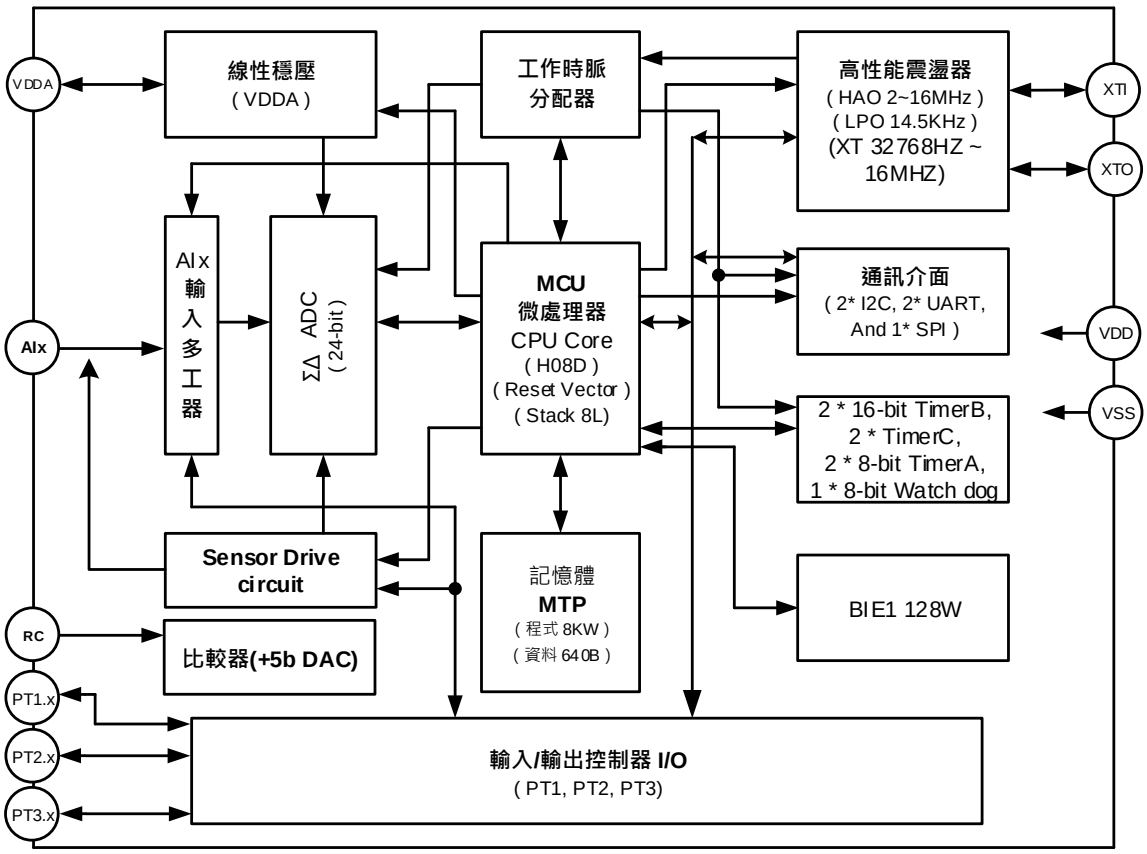


圖 4-1 內部方塊圖

4.2. 相關說明與支援文件

晶片功能相關使用說明書

DS-HY17M26	HY17M26 規格說明書
UG-HY17M26	HY17M26 使用說明書
APD-CORE002	H08A、H08C、H08D 組合語言指令集說明書
APD-HYIDE016	H08 CIDE 軟體使用說明書

開發工具相關使用說明書

APD-HY17MIDE001	HY17M Series Assembly IDE 軟體使用說明書
APD-HY17MIDE010	HY17M26 Series IDE 硬體使用說明書

產品生產相關使用說明書

APD-HY17MIDE0xx	HY17M26 生產線專用燒錄器說明書

4.3. Clock System

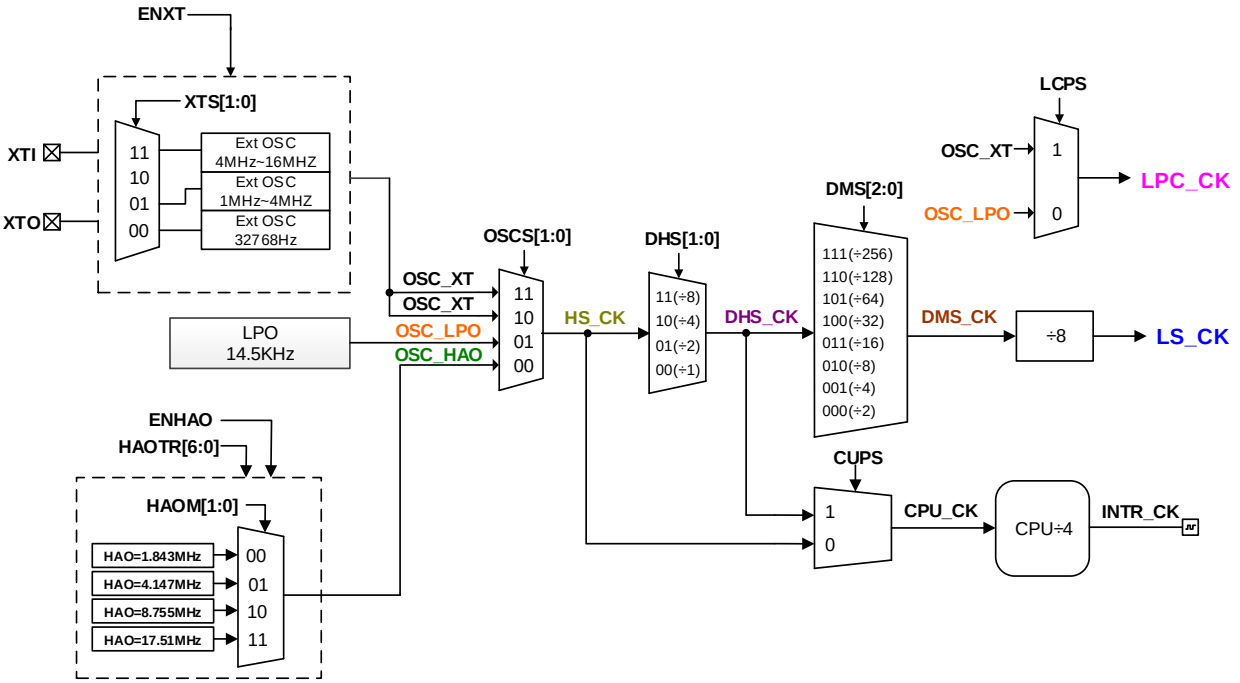


圖 4-2 Clock System(一)

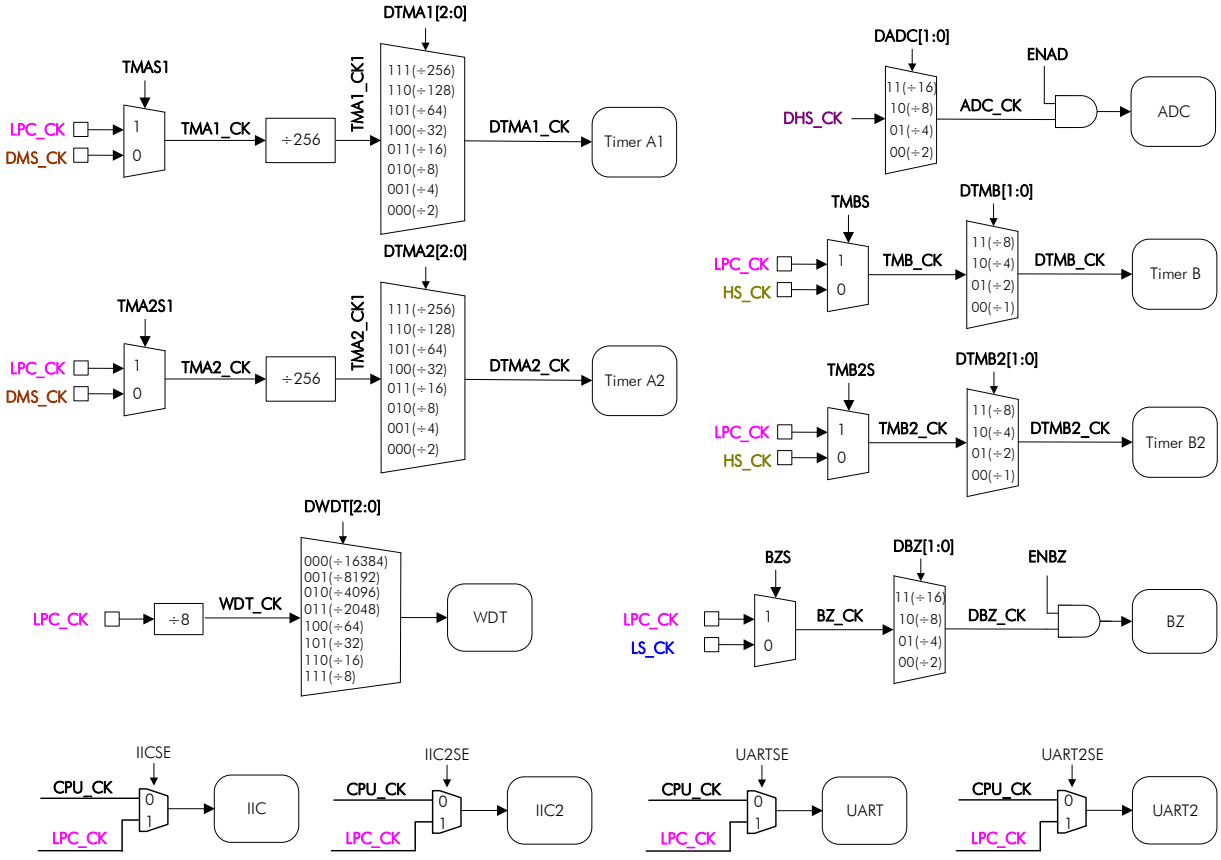


圖 4-3 Clock System(二)

4.4. GPIO PT1~ PT3 System

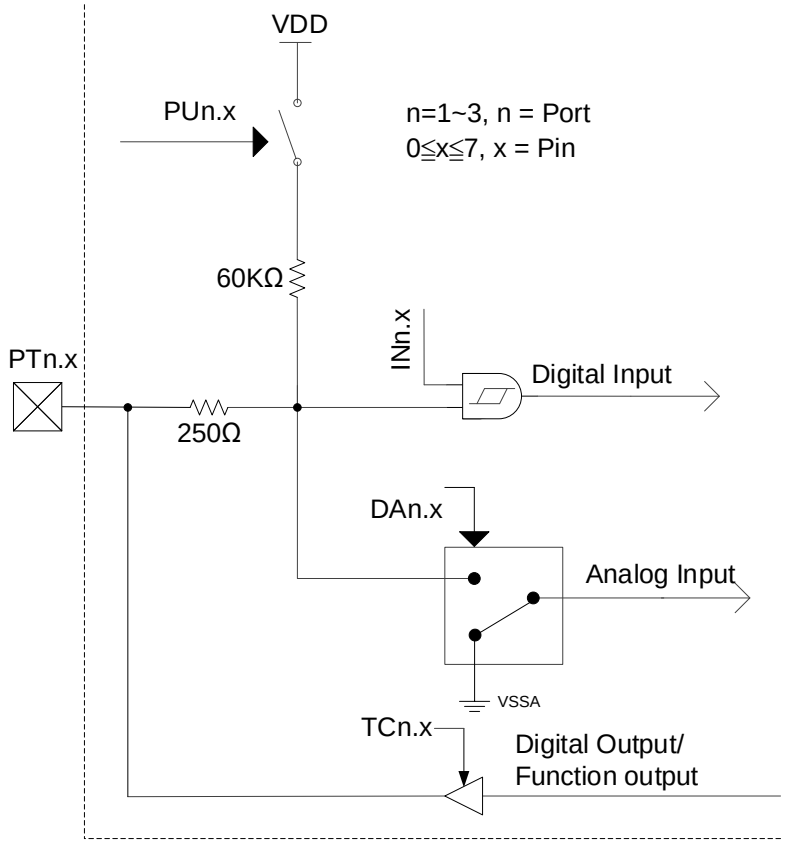


圖 4-4 GPIO PT1~ PT3 System

4.5. Reset System

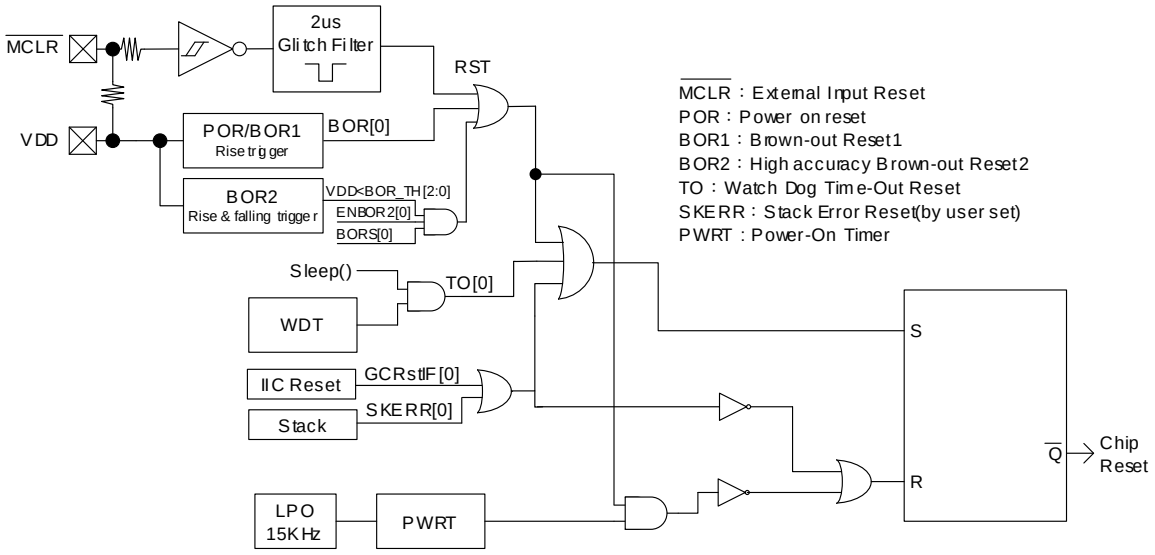


圖 4-5 Reset

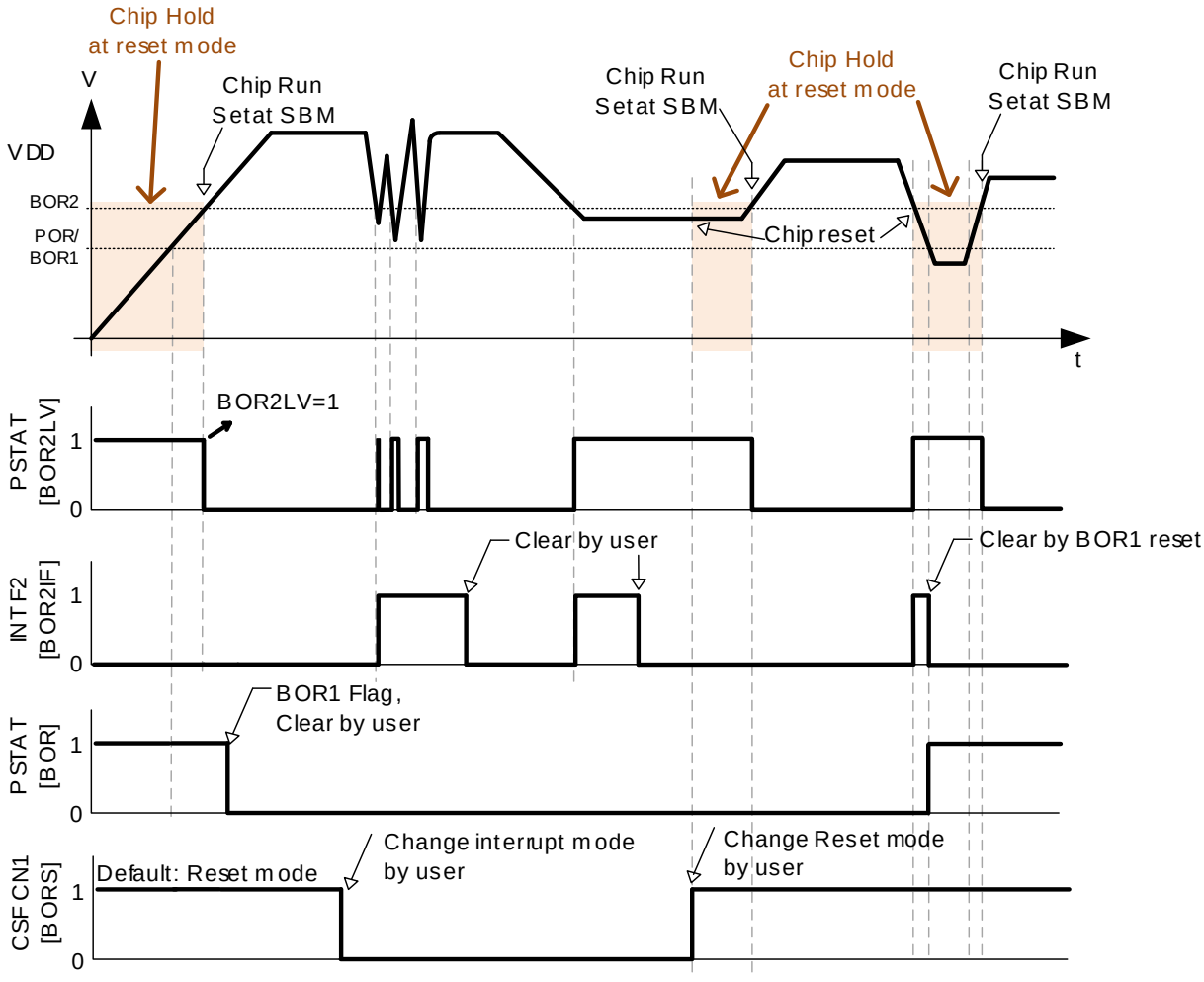


圖 4-6 BOR1 and BOR2 Chart

4.6. Power System

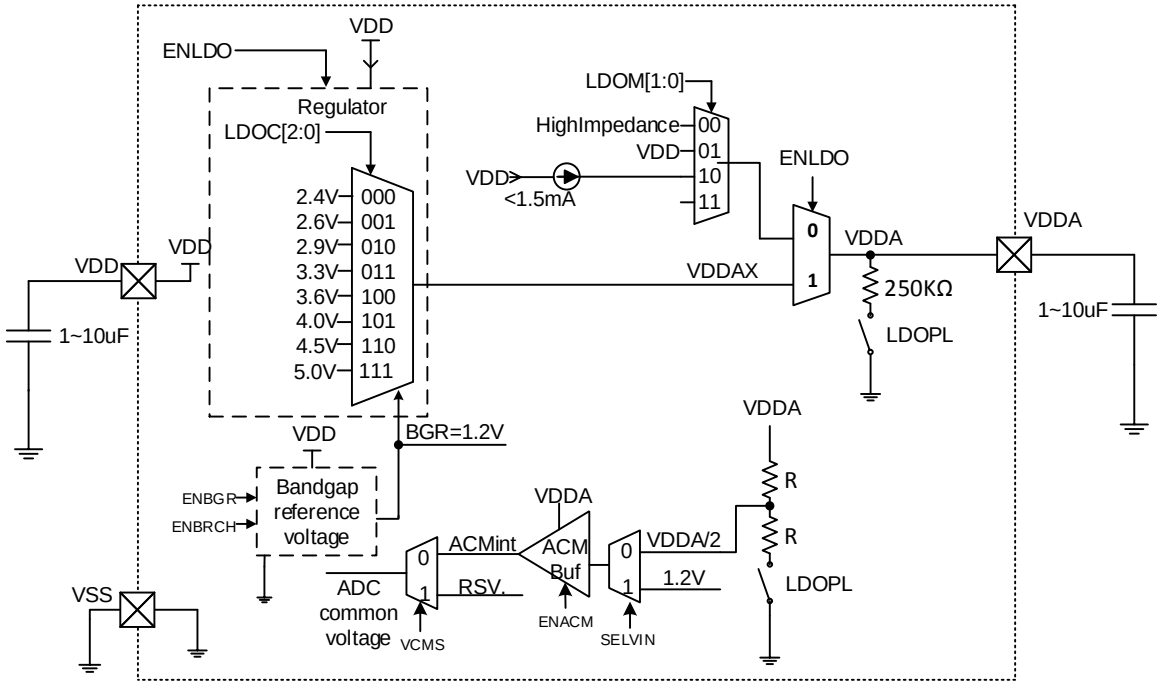
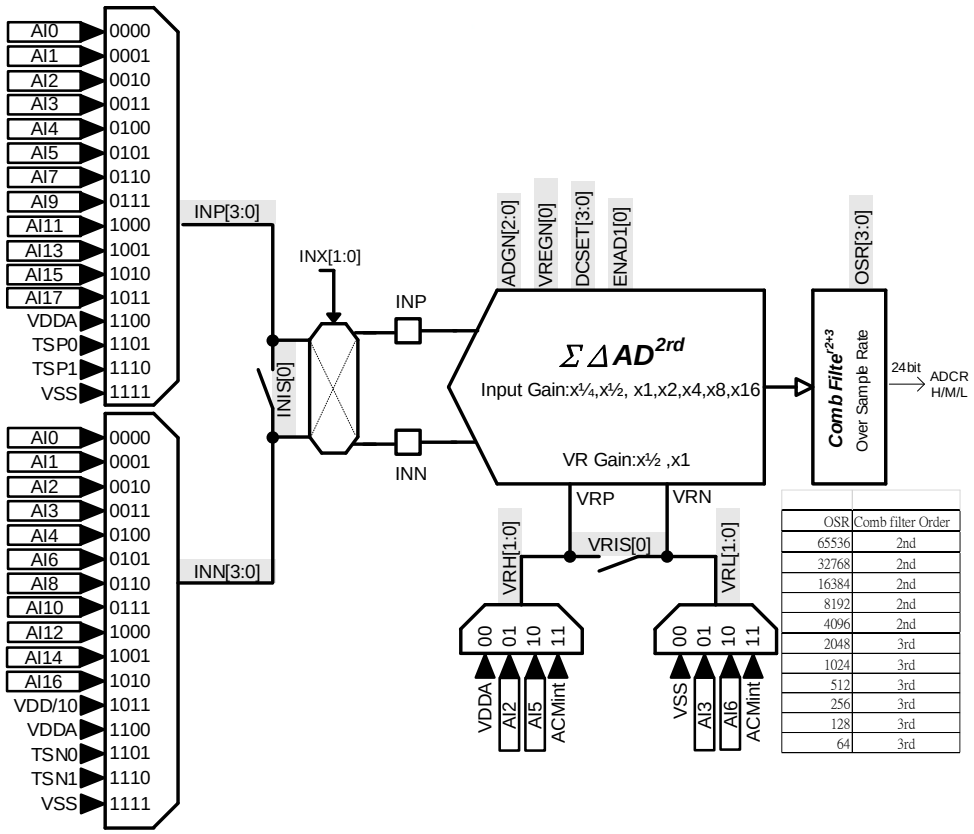


圖 4-7 Power System

4.7. ADC Network



OSR	Comb filter Order
65536	2nd
32768	2nd
16384	2nd
8192	2nd
4096	2nd
2048	3rd
1024	3rd
512	3rd
256	3rd
128	3rd
64	3rd

圖 4-8 ADC Network

4.8. Comparator Network

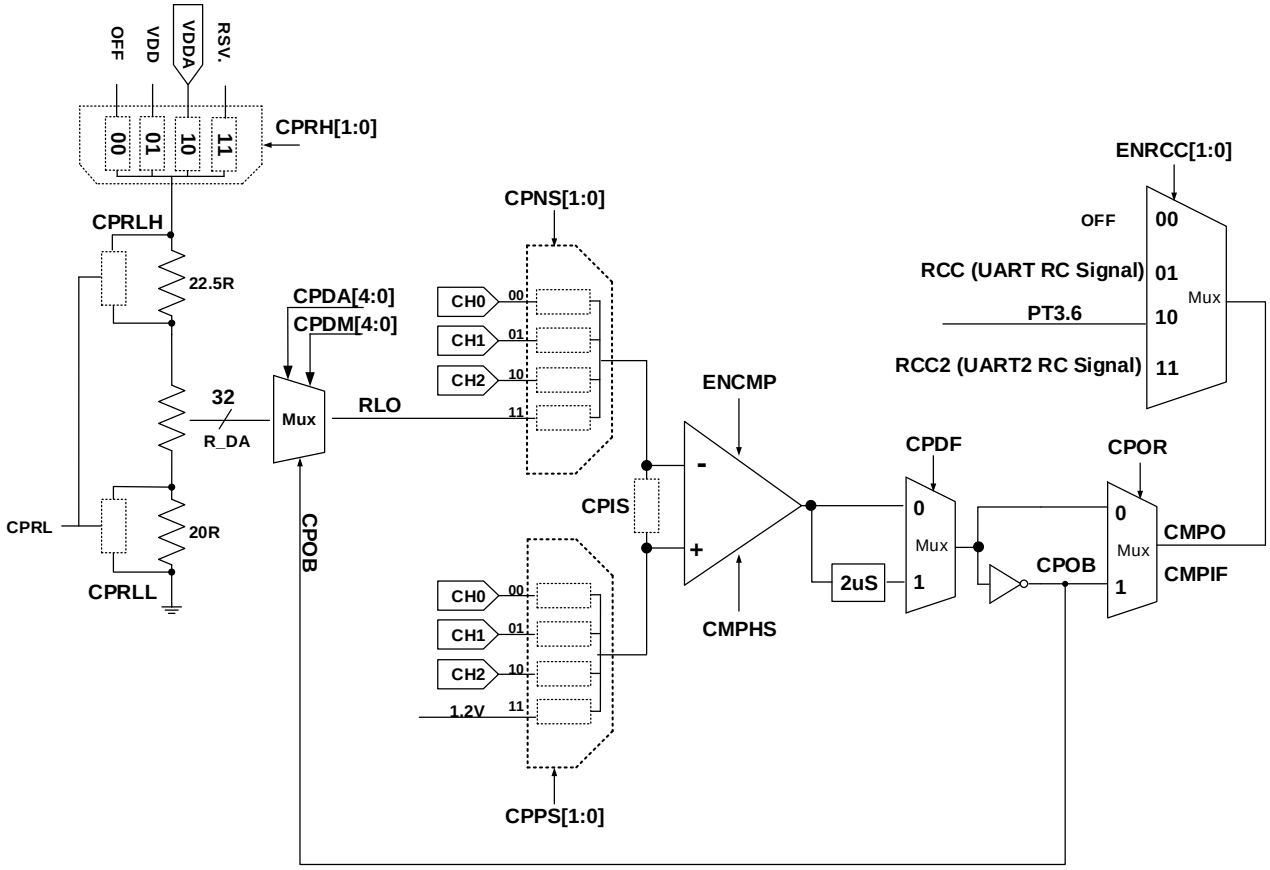
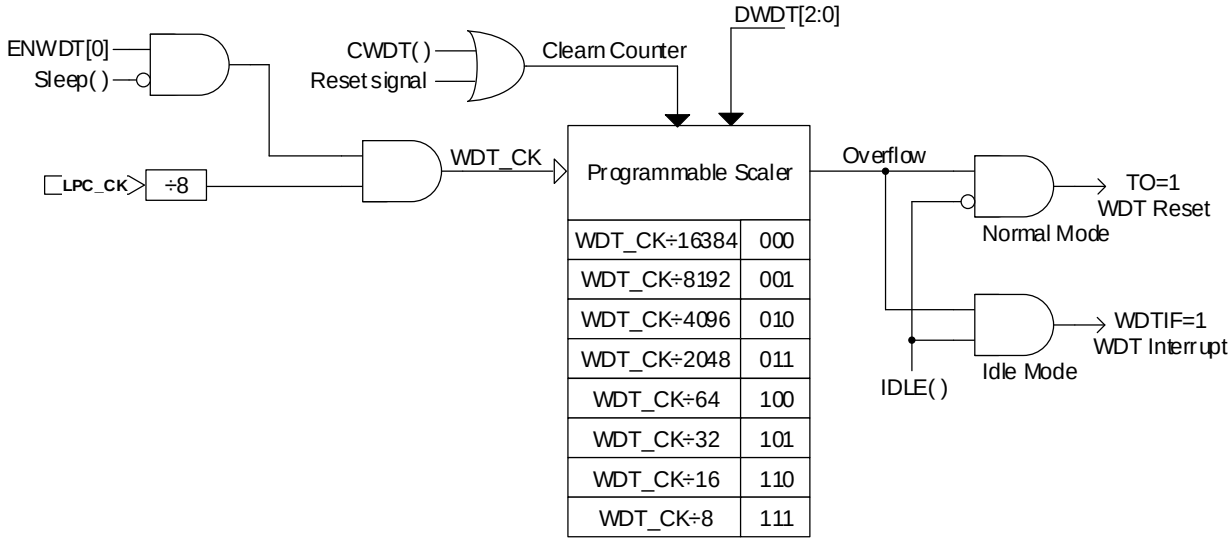


圖 4-9 Comparator Network

4.9. Watch Dog System



WDT_CK÷16384	000
WDT_CK÷8192	001
WDT_CK÷4096	010
WDT_CK÷2048	011
WDT_CK÷64	100
WDT_CK÷32	101
WDT_CK÷16	110
WDT_CK÷8	111

圖 4-10 Watch Dog System

4.10. 8-bit Timer A1 System (TMA1)

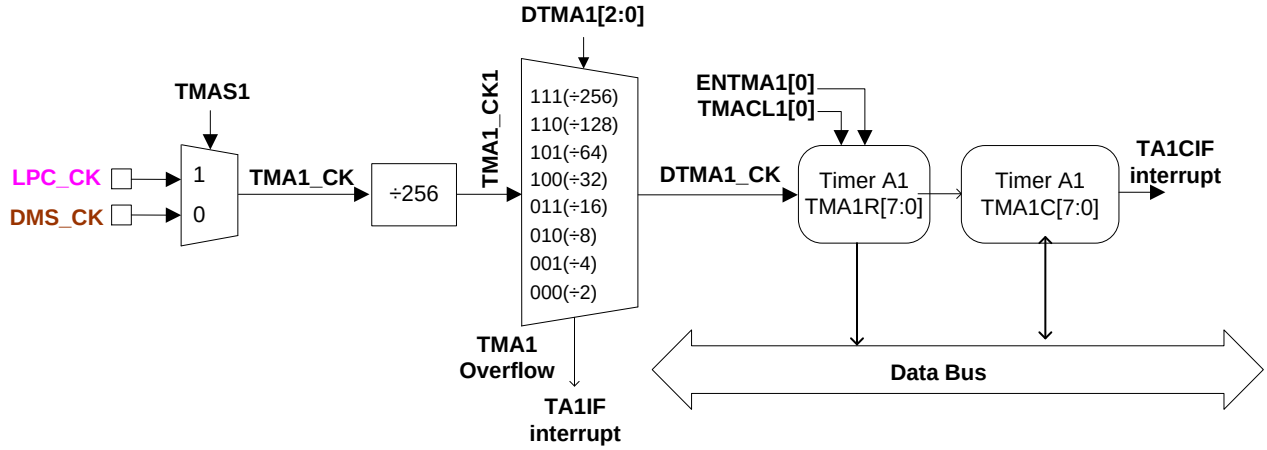


圖 4-11 Timer A1 System

4.11. 8-bit Timer A2 System (TMA2)

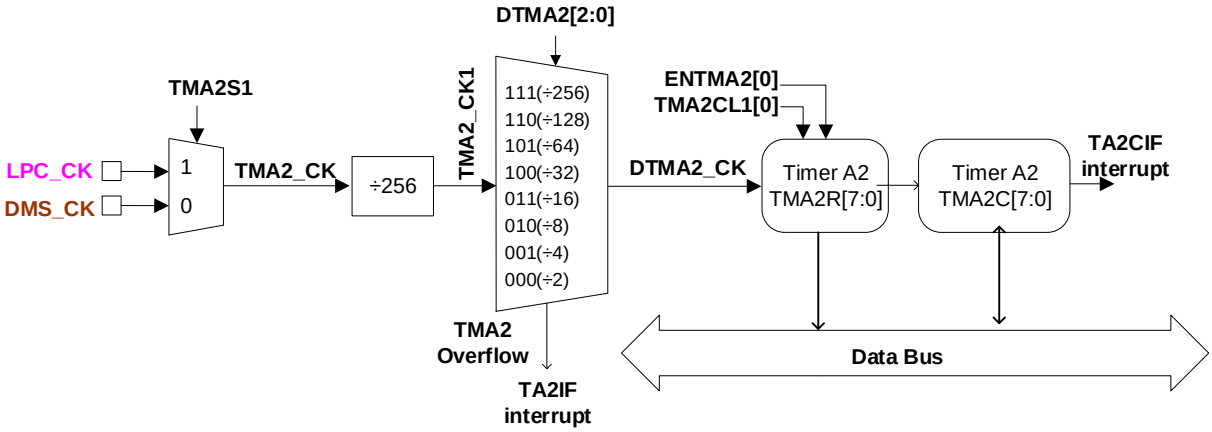


圖 4-12 Timer A2 System

4.12. 16-bit Timer B1 System (TMB1)

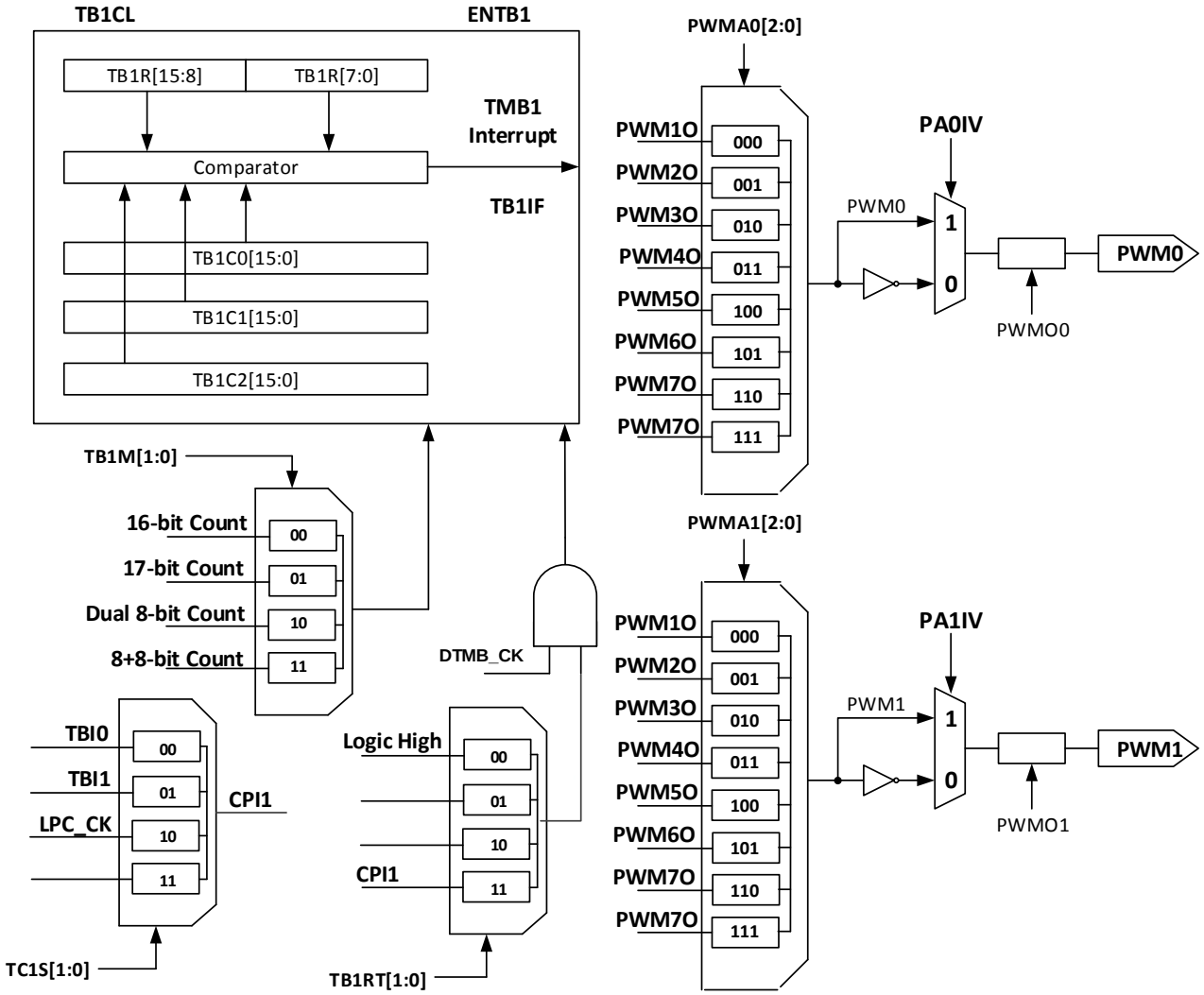


圖 4-13 Timer B1 System

4.13. 16-bit Timer B2 System (TMB2)

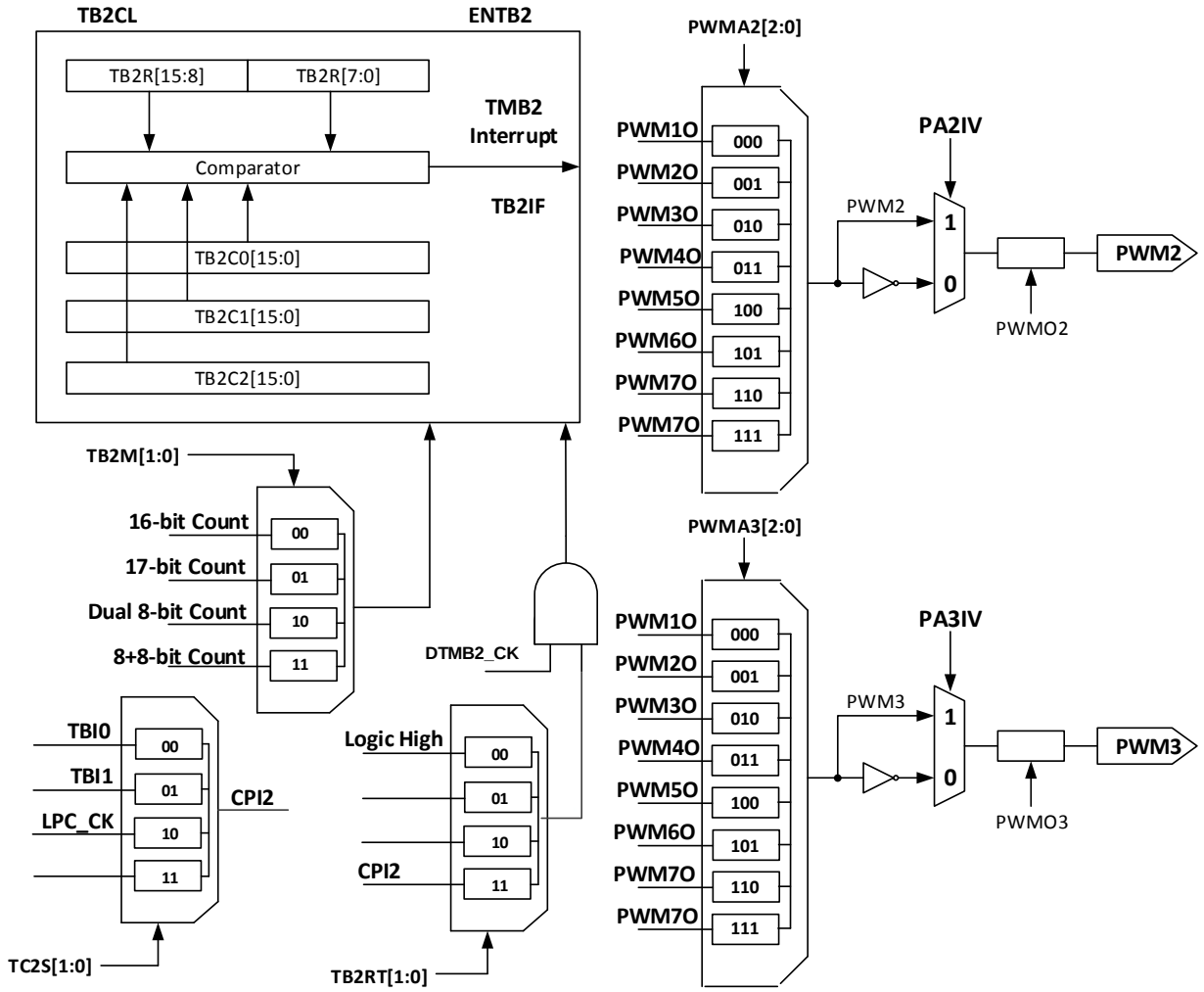


圖 4-14 Timer B2 System

4.14. Timer C1 (TMC1)

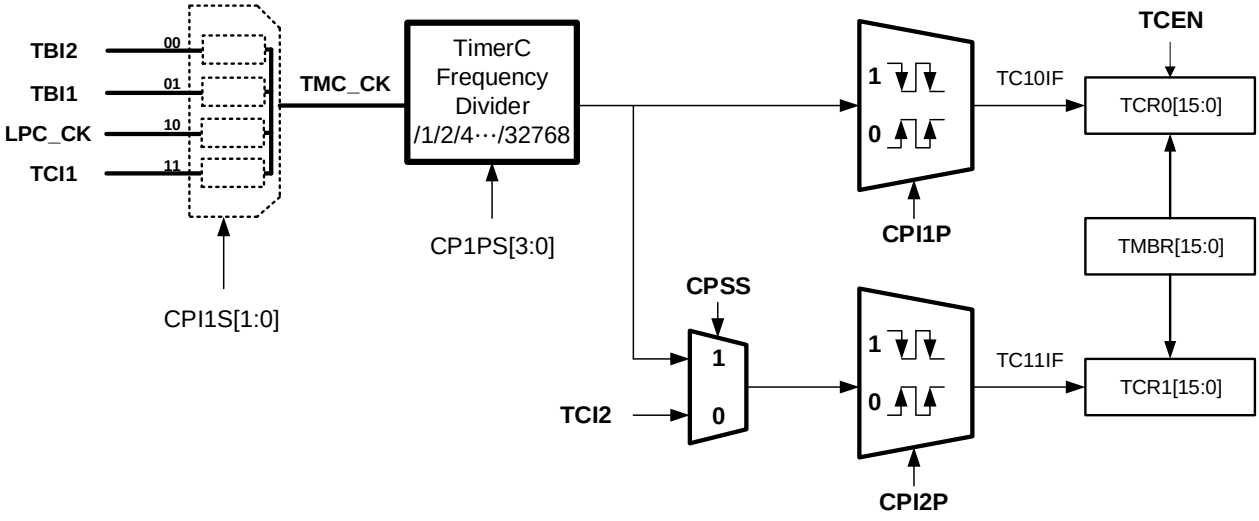


圖 4-15 Timer C1 System

4.15. Timer C2 (TMC2)

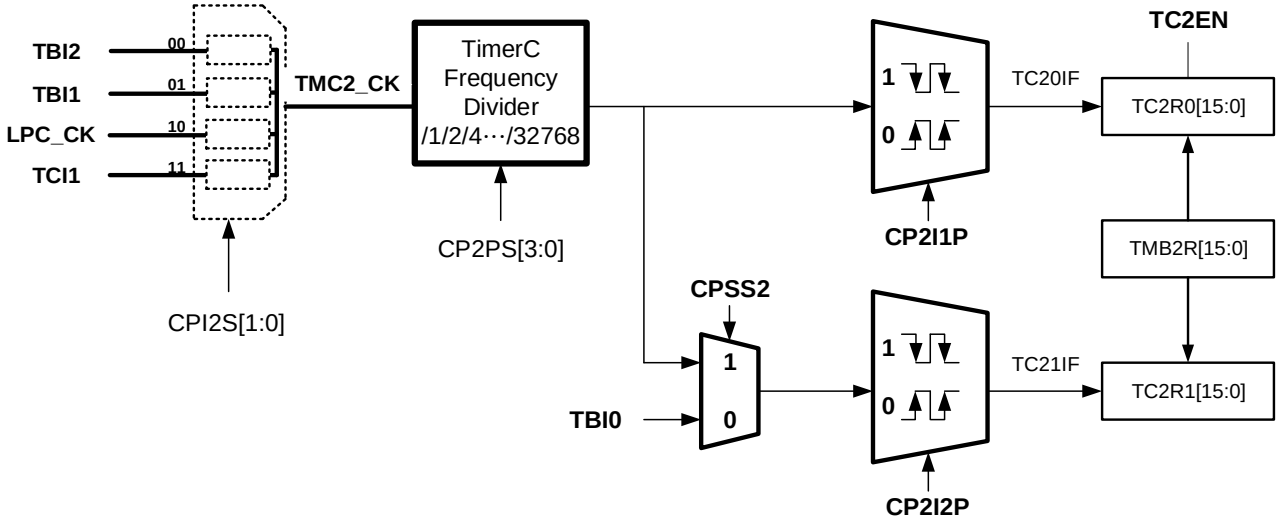


圖 4-16 Timer C2 System

4.16. I²C and I²C2

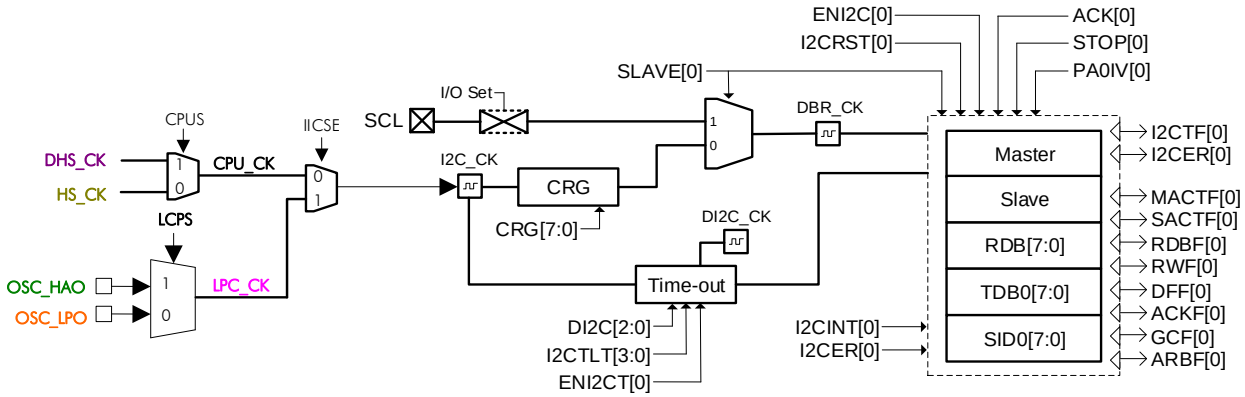


圖 4-17 I²C 方塊圖

4.17. EUART and EUART2

EUART TRANSMIT BLOCK DIAGRAM

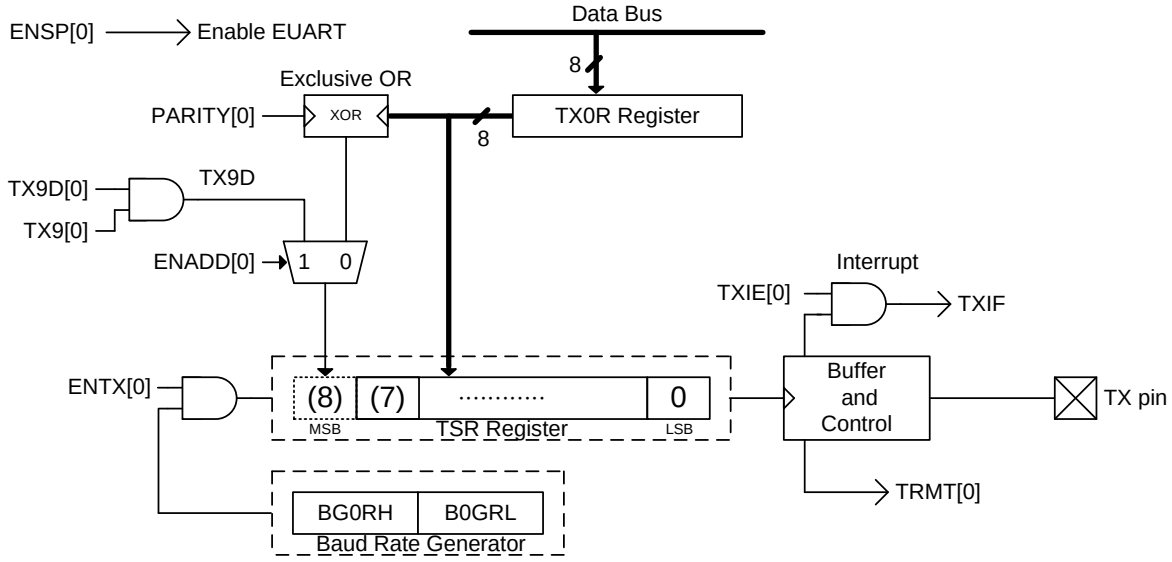
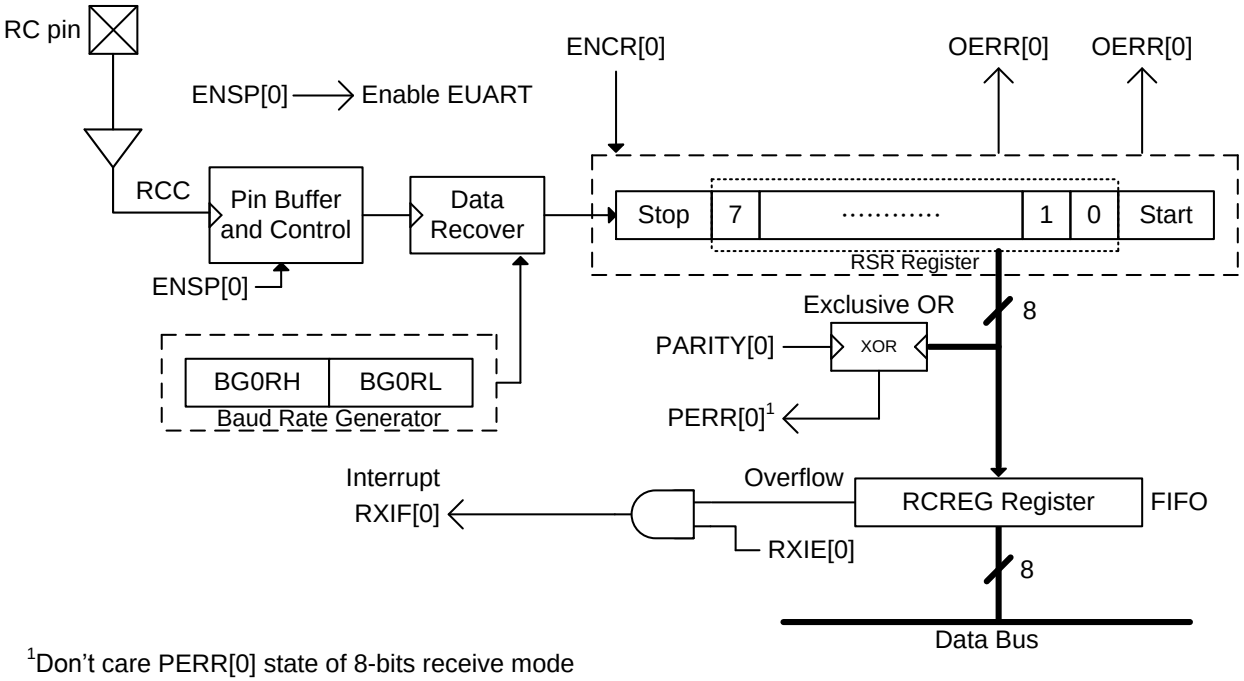


圖 4-18 EUART 傳送方塊圖

EUART 8-BITs RECEIVE BLOCK DIAGRAM



[1]Don't care PERR[0] state of 8-bits receive mode

圖 4-19 EUART 8-bits 接收方塊圖

4.18. SPI

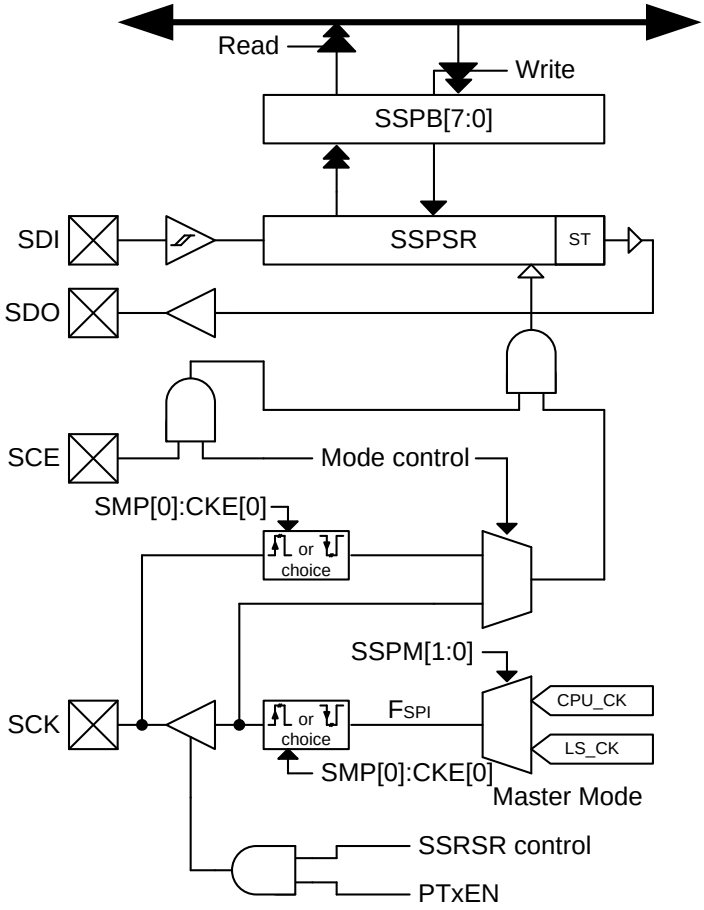


圖 4-20 SPI 方塊圖

5. 暫存器列表

"-"no use,"*"read/write,"w"write,"r"read,"r0"onlyread 0,"r1"onlyread 1,"w0"onlywrite 0,"w1"omlywrite 1
"$"for event status,"."unimplemented bit,"x"unknown,"u"unchanged,"d"depends on condition

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	ARST	IRST	R/W
000h	INDF0	Contents of FSR0 to address data memoryvalue of FSR0 not changed								xxxx xxxx	uuuu uuuu	*,*,*,*,*,*,*,*
001h	POINC0	Contents of FSR0 to address data memoryvalue of FSR0 post-incremented								xxxx xxxx	uuuu uuuu	*,*,*,*,*,*,*,*
002h	PODEC0	Contents of FSR0 to address data memoryvalue of FSR0 post-decremented								xxxx xxxx	uuuu uuuu	*,*,*,*,*,*,*,*
003h	PRINC0	Contents of FSR0 to address data memoryvalue of FSR0 pre-incremented								xxxx xxxx	uuuu uuuu	*,*,*,*,*,*,*,*
004h	PLUSW0	Contents of FSR0 to address data memoryvalue of FSR0 offset by W								xxxx xxxx	uuuu uuuu	*,*,*,*,*,*,*,*
005h	INDF1	Contents of FSR1 to address data memoryvalue of FSR1 not changed								xxxx xxxx	uuuu uuuu	*,*,*,*,*,*,*,*
006h	POINC1	Contents of FSR1 to address data memoryvalue of FSR1 post-incremented								xxxx xxxx	uuuu uuuu	*,*,*,*,*,*,*,*
007h	PODEC1	Contents of FSR1 to address data memoryvalue of FSR1 post-decremented								xxxx xxxx	uuuu uuuu	*,*,*,*,*,*,*,*
008h	PRINC1	Contents of FSR1 to address data memoryvalue of FSR1 pre-incremented								xxxx xxxx	uuuu uuuu	*,*,*,*,*,*,*,*
009h	PLUSW1	Contents of FSR1 to address data memoryvalue of FSR1 offset by W								xxxx xxxx	uuuu uuuu	*,*,*,*,*,*,*,*
00Ah	INDF2	Contents of FSR2 to address data memoryvalue of FSR2 not changed								xxxx xxxx	uuuu uuuu	*,*,*,*,*,*,*,*
00Bh	POINC2	Contents of FSR2 to address data memoryvalue of FSR2 post-incremented								xxxx xxxx	uuuu uuuu	*,*,*,*,*,*,*,*
00Ch	PODEC2	Contents of FSR2 to address data memoryvalue of FSR2 post-decremented								xxxx xxxx	uuuu uuuu	*,*,*,*,*,*,*,*
00Dh	PRINC2	Contents of FSR2 to address data memoryvalue of FSR2 pre-incremented								xxxx xxxx	uuuu uuuu	*,*,*,*,*,*,*,*
00Eh	PLUSW2	Contents of FSR2 to address data memoryvalue of FSR2 offset by W								xxxx xxxx	uuuu uuuu	*,*,*,*,*,*,*,*
00Fh	FSR0H	-	-	-	-	-	-	FSR0[9:8]		xx	.... ..uu	-,-,-,- -,-,*,*
010h	FSR0L	Indirect Data Memory Address Pointer 0 Low Byte,FSR0[7:0]								xxxx xxxx	uuuu uuuu	*,*,*,*,*,*,*,*
011h	FSR1H	-	-	-	-	-	-	FSR1[9:8]		xx	.... ..uu	-,-,-,- -,-,*,*
012h	FSR1L	Indirect Data Memory Address Pointer 0 Low Byte,FSR1[7:0]								xxxx xxxx	uuuu uuuu	*,*,*,*,*,*,*,*
013h	FSR2H	-	-	-	-	-	-	FSR2[9:8]		xx	.... ..uu	-,-,-,- -,-,*,*
014h	FSR2L	Indirect Data Memory Address Pointer 0 Low Byte,FSR2[7:0]								xxxx xxxx	uuuu uuuu	*,*,*,*,*,*,*,*
015h	TOSU	-	-	-	-	-	-	-	-	xxxx xxxx	uuuu uuuu	*,*,*,*,*,*,*,*
016h	TOSH	-	-	-	TOS[12:8]					...x xxxx	...u uuuu	-,-,-,-,*,*,*,*
017h	TOSL	Top-of-Stack Low Byte (TOS<7:0>)								xxxx xxxx	uuuu uuuu	*,*,*,*,*,*,*,*
018h	SKCN	SKFL	SKUN	SKOV	-	SKPRT[3:0]				000. 0000	u$$. $$$$	rw 0,rw 0,rw 0,- *,*,*,*
019h	PCLATU	-	-	-	-	-	-	-	-	xxxx xxxx	uuuu uuuu	*,*,*,*,*,*,*,*
01Ah	PCLATH	-	-	-	PC[12:8]					...0 0000	...0 0000	-,-,-,-,*,*,*,*
01Bh	PCLATL	PC Low Byte for PC<7:0>								0000 0000	0000 0000	*,*,*,*,*,*,*,*
01Ch	TBLPTRU	-	-	-	-	-	-	-	-	xxxx xxxx	uuuu uuuu	*,*,*,*,*,*,*,*
01Dh	TBLPTRH	-	-	-	TBLPTR[12:8]					...x xxxx	...u uuuu	-,-,-,-,*,*,*,*
01Eh	TBLPTRL	Program Memory Table Pointer Low Byte (TBLPTR<7:0>)								xxxx xxxx	uuuu uuuu	*,*,*,*,*,*,*,*
01Fh	TBLDH	Program Memory Table Latch High Byte								xxxx xxxx	uuuu uuuu	*,*,*,*,*,*,*,*
020h	TBLDL	Program Memory Table Latch Low Byte								xxxx xxxx	uuuu uuuu	*,*,*,*,*,*,*,*
021h	PRODH	Product Register of Multiply High Byte								xxxx xxxx	uuuu uuuu	*,*,*,*,*,*,*,*
022h	PRODL	Product Register of Multiply Low Byte								xxxx xxxx	uuuu uuuu	*,*,*,*,*,*,*,*
023h	INTE0	GIE	TA1CIE	ADIE	WDTIE	TB1IE	-	E1IE	E0IE	0000 0.00	0uuu uuuu	*,*,*,*,*,*,*,*
024h	INTE1	TA1IE	SPIIE	TXIE	RCIE	I2CERIE	I2CIE	E3IE	E2IE	0000 0000	uuuu uuuu	*,*,*,*,*,*,*,*
025h	INTE2	TA2IE	TA2CIE	TC11IE	TC10IE	-	CMPIE	TB2IE	BOR2IE	0000 .000	uuuu uuuu	*,*,*,*,*,*,*,*
026h	INTF0	-	TA1CIF	ADIF	WDTIF	TB1IF	-	E1IF	E0IF	.000 0.00	.uuu uuuu	*,*,*,*,*,*,*,*
027h	INTF1	TA1IF	SPIIF	TXIF	RCIF	I2CERIF	I2CIF	E3IF	E2IF	0000 0000	uuuu uuuu	*,*,*,*,r,r,*,*
028h	INTF2	TA2IF	TA2CIF	TC1IF	TC0IF	-	CMPIF	TB2IF	BOR2IF	0000 .000	uuuu uuuu	*,*,*,*,*,*,*,*
029h	WREG	Working Register								xxxx xxxx	uuuu uuuu	*,*,*,*,*,*,*,*
02Ah	BSRCN	-	-	-	-	-	-	-	BSR[0]	x	....u	-,-,-,- -,-,-,*
02Bh	MSTAT	-	-	-	C	DC	N	OV	Z	...x xxxx	...u uuuu	-,-,-,-*,*,*,*
02Ch	PSTAT	BOR	PD	TO	IDL	RST	SKERR	BOR2LV	GCRstIF	$000 $000	uu$u u$uu	rw0,rw0,rw0,rw0 rw0,rw0,r,rw0
02Eh	INTE3	-	-	TX2IE	RC2IE	TC21IE	TC20IE	I2CER2IE	I2C2IE	00 0000	uuuu uuuu	*,*,*,*,*,*,*,*
02Fh	INTF3	-	GC2RstIF	TX2IF	RC2IF	TC21IF	TC20IF	I2CER2IF	I2C2IF	.000 0000	uuuu uuuu	*,rw 0,*,*,*,*,r,r
030h	PWRCN	ENBGR	LDOC[2:0]			LDOM[1:0]		ENLDO	CSFON	1000 0000	uuuu uu0u	*,*,*,*,*,*,*,*
031h	OSCCN0	OSCS[1:0]		DHS[1:0]		DMS[2:0]			CUPS	0000 0000	uuuu uuuu	*,*,*,*,*,*,*,*
032h	OSCCN1	CCOPT	LCPS	DADC[1:0]		DTMB[1:0]		TMBS	-	0000 000.	uuuu uuu.	*,*,*,*,*,*,*,-
033h	OSCCN2	IDLEM1	IDLEM0	ENXT	XTS[1:0]		HAOM[1:0]		ENHAO	0000 0001	uuuu uuu1	*,*,*,*,*,*,*,*
034h	OSCCN3	-	-	-		DTMB2[1:0]		TMB2S	-	.... 000.	.... uuu.	*,*,*,*,*,*,*,*
035h	CSFCN0	SKRST	HAOTR[6:0]							.1..	....	-,-,-,- -,-,-,-
036h	CSFCN1	MCLR	-	ENINXCH	BOR_TH[2:0]			BORS	ENBOR2	0.00 0011	0.uu uuuu	*,-,*,*,*,*,*,*
037h	CSFCN2	-	-							00..	00uu uuuu	*,*,*,*,*,*,*,*

表 5-1 資料記憶體列表

"-"no use,"*"read/write,"w"write,"r"read,"r0"only read 0,"r1"only read 1,"w0"only write 0,"w1"omly write 1

"$"for event status,"."unimplemented bit,"x"unknown,"u"unchanged,"d"depends on condition

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	ARST	IRST	R/W
038h	WDTCN	ENBZ	BZS	BZ[1:0]		ENWDT	DWDT[2:0]			0000 0000	uuuu $000	-,*,** rw 1,*,**
039h	AD1H	ADC1 conversion high byte data register								0000 0000	uuuu uuuu	r,r,r,r r,r,r,r
03Ah	AD1M	ADC1 conversion middle byte data register								0000 0000	uuuu uuuu	r,r,r,r r,r,r,r
03Bh	AD1L	ADC1 conversion low byte data register								0000 0000	uuuu uuuu	r,r,r,r r,r,r,r
03Ch	AD1HH	ADC1 conversion high byte data register								0000 0000	uuuu uuuu	*,*,*,*,*,*,*,*
03Dh	AD1MM	ADC1 conversion middle byte data register								0000 0000	uuuu uuuu	*,*,*,*,*,*,*,*
03Eh	AD1LL	ADC1 conversion low byte data register								0000 0000	uuuu uuuu	*,*,*,*,*,*,*,*
03Fh	AD1CN0	ENAD1	-			OSR[3:0]			CMFR	0000 0000	uuuu uuuu	*,*,*,*,*,*,*,*
040h	AD1CN1	-	-	VREGN	-	-	ADGN[2:0]			000. .000	uuuu uuuu	*,*,*,*,*,*,*,*
041h	AD1CN2			-	SELVIN	DCSET[3:0]				..00 0000	uuuu uuuu	*,*,*,*,*,*,*,*
042h	AD1CN3	INP[3:0]				INN[3:0]				0000 0000	uuuu uuuu	*,*,*,*,*,*,*,*
043h	AD1CN4	VRH[1:0]		VRL[1:0]		INX[1:0]		VRIS	INIS	0000 0000	uuuu uuuu	*,*,*,*,*,*,*,*
044h	AD1CN5	ENACM	-	VCMS	LDOPL	-	-	ENTPS	TPSCH	0.00 .000	uuuu uuuu	*,*,*,*,*,*,*,*
045h	LVDCN	DAFM	ENCH	-	-	-	-	-	-	00..	uu..	*,*,*,*,*,*,*,*
046h	MCCN0	ENRCC[1:0]		CMPO	CPIS	CPOR	CPDF	CMPHS	ENCMP	0000 0000	uuuu uuuu	*,*,r,*,*,*,*,*
047h	MCCN1	CPRL	VRSEL	CPRH[1:0]		CPPS[1:0]		CPNS[1:0]		0000 0000	uuuu uuuu	*,*,*,*,*,*,*,*
048h	MCCN2				CPDA[4:0]					0000 0000	uuuu uuuu	*,*,*,*,*,*,*,*
049h	MCCN3				CPDM[4:0]					0000 0000	uuuu uuuu	*,*,*,*,*,*,*,*
04Ah	-	-		-	-	-	-		-	0000 .000	uuuu .uuu	*,*,*,-,*,**
04Bh	TMA1CN	ENTMA1	TMACL1	TMAS1	DTMA1[2:0]			-		0000 0000	u0uu uuuu	*,rw 1,*,*,*,*,*
04Ch	TMA1R	TMA1 counter Register								0000 0000	uuuu uuuu	rw0,rw0,rw0,rw0 rw0,rw0,rw0,rw0
04Dh	TMA1C	TMA1C counter Register								0000 0000	uuuu uuuu	rw0,rw0,rw0,rw0 rw0,rw0,rw0,rw0
04Eh	TMA2CN	ENTMA2	TMA2CL1	TMA2S1	DTMA2[2:0]			-	-	0000 0000	u0uu uuuu	*,rw 1,*,*,*,*,*
04Fh	TMA2R	TMA2 counter Register								0000 0000	uuuu uuuu	rw0,rw0,rw0,rw0 rw0,rw0,rw0,rw0
050h	TMA2C	TMA2C counter Register								0000 0000	uuuu uuuu	rw0,rw0,rw0,rw0 rw0,rw0,rw0,rw0
051h	TB1Flag	-	PWM7A	PWM6A	PWM5A	PWM4A	PWM3A	PWM2A	PWM1A	..00 0000	..uu uuuu	-,r,r,r r,r,r,r
052h	TB1CN0	ENTB1	TB1M[1:0]		TB1RT[1:0]		TB1CL	PWMO1	PWMO0	0000 0000	uuuu u0uu	*,*,*,*,*,rw 1,*,*
053h	TB1CN1	PA1IV	PWMA1[2:0]			PA0IV	PWMA0[2:0]			0000 0000	uuuu uuuu	*,*,*,*,*,*,*,*
054h	TB1RH	TimerB1 counter Register [15:8]								xxxx xxxx	uuuu uuuu	r,r,r,r r,r,r,r
055h	TB1RL	TimerB1 counter Register [7:0]								xxxx xxxx	uuuu uuuu	r,r,r,r r,r,r,r
056h	TB1C0H	TimerB1 counter Condition Register [15:8]								xxxx xxxx	uuuu uuuu	*,*,*,*,*,*,*,*
057h	TB1C0L	TimerB1 counter Condition Register [7:0]								xxxx xxxx	uuuu uuuu	*,*,*,*,*,*,*,*
058h	TB1C1H	TimerB1 counter Condition Register [15:8]								xxxx xxxx	uuuu uuuu	*,*,*,*,*,*,*,*
059h	TB1C1L	TimerB1 counter Condition Register [7:0]								xxxx xxxx	uuuu uuuu	*,*,*,*,*,*,*,*
05Ah	TB1C2H	TimerB1 counter Condition Register [15:8]								xxxx xxxx	uuuu uuuu	*,*,*,*,*,*,*,*
05Bh	TB1C2L	TimerB1 counter Condition Register [7:0]								xxxx xxxx	uuuu uuuu	*,*,*,*,*,*,*,*
05Ch	TC1CN0		TC1S[1:0]				CPI2P	CPI1P	TCEN	0000 0000	uuuu uuuu	uuuu uuuu
05Dh	TC1CN1	-	CPSS	CPI1S[1:0]		CP1PS[3:0]				0000 0000	uuuu uuuu	uuuu uuuu
05Eh	TC1R0H	Timer C1 Capture 0 High Byte Data Register								xxxx xxxx	uuuu uuuu	uuuu uuuu
05Fh	TC1R0L	Timer C1 Capture 0 Low Byte Data Register								xxxx xxxx	uuuu uuuu	uuuu uuuu
060h	TC1R1H	Timer C1 Capture 1 High Byte Data Register								xxxx xxxx	uuuu uuuu	uuuu uuuu
061h	TC1R1L	Timer C1 Capture 1 Low Byte Data Register								xxxx xxxx	uuuu uuuu	uuuu uuuu
062h	TB2Flag	-	PWM7A	PWM6A	PWM5A	PWM4A	PWM3A	PWM2A	PWM1A	..00 0000	..uu uuuu	-,r,r,r r,r,r,r
063h	TB2CN0	ENTB2	TB2M[1:0]		TB2RT[1:0]		TB2CL	PWMO3	PWMO2	0000 0000	uuuu u0uu	*,*,*,*,*,rw 1,*,*
064h	TB2CN1	PA3IV	PWMA3[2:0]			PA2IV	PWMA2[2:0]			0000 0000	uuuu uuuu	*,*,*,*,*,*,*,*
065h	TB2RH	TimerB2 counter Register [15:8]								xxxx xxxx	uuuu uuuu	r,r,r,r r,r,r,r
066h	TB2RL	TimerB2 counter Register [7:0]								xxxx xxxx	uuuu uuuu	r,r,r,r r,r,r,r
067h	TB2C0H	TimerB2 counter Condition Register [15:8]								xxxx xxxx	uuuu uuuu	*,*,*,*,*,*,*,*
068h	TB2C0L	TimerB2 counter Condition Register [7:0]								xxxx xxxx	uuuu uuuu	*,*,*,*,*,*,*,*
069h	TB2C1H	TimerB2 counter Condition Register [15:8]								xxxx xxxx	uuuu uuuu	*,*,*,*,*,*,*,*
06Ah	TB2C1L	TimerB2 counter Condition Register [7:0]								xxxx xxxx	uuuu uuuu	*,*,*,*,*,*,*,*
06Bh	TB2C2H	TimerB2 counter Condition Register [15:8]								xxxx xxxx	uuuu uuuu	*,*,*,*,*,*,*,*
06Ch	TB2C2L	TimerB2 counter Condition Register [7:0]								xxxx xxxx	uuuu uuuu	*,*,*,*,*,*,*,*
06Dh	TC2CN0		TC2S[1:0]				CP2I2P	CP2I1P	TC2EN	0000 0000	uuuu uuuu	uuuu uuuu
06Eh	TC2CN1	-	CPSS2	CPI2S[1:0]		CP2PS[3:0]				0000 0000	uuuu uuuu	uuuu uuuu
06Fh	TC2R0H	Timer C2 Capture 0 High Byte Data Register								xxxx xxxx	uuuu uuuu	uuuu uuuu
070h	TC2R0L	Timer C2 Capture 0 Low Byte Data Register								xxxx xxxx	uuuu uuuu	uuuu uuuu
071h	TC2R1H	Timer C2 Capture 1 High Byte Data Register								xxxx xxxx	uuuu uuuu	uuuu uuuu
072h	TC2R1L	Timer C2 Capture 1 Low Byte Data Register								xxxx xxxx	uuuu uuuu	uuuu uuuu

表 5-2 資料記憶體列表

"-"no use,"*"read/write,"w"write,"r"read,"r0"onlyread 0,"r1"onlyread 1,"w0"onlywrite 0,"w1"omlywrite 1

"$"for event status,"."unimplemented bit,"x"unknown,"u"unchanged,"d"depends on condition

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	ARST	IRST	R/W
073h	UR0CN	ENSP	ENTX	TX9	TX9D	PARITY	-	-	WUE	0000 0..0	uuuu u..u	*,*,*,*,-,-,*
074h	UR0STA	-	RC9D	PERR	FERR	OERR	RCIDL	TRMT	ABDOVF	.000 0010	.uuu uuuu	-,r,r,r r,r,r,rw 0
075h	BA0CN	UARTSE	-	-	-	ENCR	RC9	ENADD	ENABD	0... 0000	u... uuuu	*,-,-,- *,*,*,*
076h	BG0RH	-	-	-	Baud Rate Generator Register High Byte					...x xxxx	...u uuuu	-,-,-,*,*,*,*
077h	BG0RL	Baud Rate Generator Register Low Byte								xxxx xxxx	uuuu uuuu	*,*,*,*,*,*,*,*
078h	TX0R	UART Transmit Register								xxxx xxxx	uuuu uuuu	*,*,*,*,*,*,*,*
079h	RC0REG	UART Receive Register								xxxx xxxx	uuuu uuuu	r,r,r,r r,r,r,r
180h	BIECN	WR1Flag	-	BIEER	-	-	BIEWR1	BIEWR	BIERD	..0. .000	uu0u u000	-,-,*,- -*,*,*
181h	BIEARH	-	-	-	-	BIE Address Register as BIEAH[7:0]				xxxx xxxx	uuuu uuuu	*,*,*,*,*,*,*,*
182h	BIEARL	BIE Address Register as BIEAL[7:0]								xxxx xxxx	uuuu uuuu	*,*,*,*,*,*,*,*
183h	BIEDRH	BIE High Byte Data Register								xxxx xxxx	uuuu uuuu	*,*,*,*,*,*,*,*
184h	BIEDRL	BIE Low Byte Data Register								xxxx xxxx	uuuu uuuu	*,*,*,*,*,*,*,*
185h	BIEKEY	BIE KEY Data Register								0000 0000	0000 0000	*,*,*,*,*,*,*,*
186h	BIE1CN	PIFBEN1	-	BIE1ER	-	-	-	BIE1WR	BIE1RD	x.00 $000	u.00 $uuu	r,-,*,* r,*,*,*
187h	BIE1ARH	ENBIE1	-	1	1	1	1	1	1	0.xx xxxx	u.uu uuuu	*,-,*,*,*,*,*,*
188h	BIE1ARL	BIE1 Address Register as BIE1AL[7:0]								xxxx xxxx	uuuu uuuu	*,*,*,*,*,*,*,*
189h	BIE1DRH	BIE1 High Byte Data Register								xxxx xxxx	uuuu uuuu	*,*,*,*,*,*,*,*
18Ah	BIE1DRL	BIE1 Low Byte Data Register								xxxx xxxx	uuuu uuuu	*,*,*,*,*,*,*,*
190h	PT1	-	PT1.6	PT1.5	PT1.4	PT1.3	PT1.2	PT1.1	PT1.0	.xxx xxxx	.xxx xxxx	*,*,*,*,*,*,*,*
191h	PT1IN	-	IN1.6	IN1.5	IN1.4	IN1.3	IN1.2	IN1.1	IN1.0	.000 0000	uuuu uuuu	*,*,*,*,*,*,*,*
192h	TRISC1	-	TC1.6	TC1.5	TC1.4	TC1.3	TC1.2	TC1.1	TC1.0	.000 0000	uuuu uuuu	*,*,*,*,*,*,*,*
193h	PT1DA	-	-	-	-	DA1.3	DA1.2	DA1.1	DA1.0	.000 0000	uuuu uuuu	*,*,*,*,*,*,*,*
194h	PT1PU	-	PU1.6	PU1.5	PU1.4	PU1.3	PU1.2	PU1.1	PU1.0	.000 0000	uuuu uuuu	*,*,*,*,*,*,*,*
195h	PT1M1	INTEG3[1:0]		INTEG2[1:0]		INTEG1[1:0]		INTEG0[1:0]		0000 0000	uuuu uuuu	*,*,*,*,*,*,*,*
196h	PT1INT	-	INTG1.6	INTG1.5	INTG1.4	-	-	-	-	.000 0000	uuuu uuuu	*,*,*,*,*,*,*,*
197h	PT1INTE	-	INTE1.6	INTE1.5	INTE1.4	-	-	-	-	.000 0000	uuuu uuuu	*,*,*,*,*,*,*,*
198h	PT1INTF	-	INTF1.6	INTF1.5	INTF1.4	-	-	-	-	.000 0000	uuuu uuuu	*,*,*,*,*,*,*,*
199h	PT2	PT2.7	PT2.6	PT2.5	PT2.4	PT2.3	PT2.2	PT2.1	PT2.0	xxxx xxxx	xxxx xxxx	*,*,*,*,*,*,*,*
19Ah	PT2IN	IN2.7	IN2.6	IN2.5	IN2.4	IN2.3	IN2.2	IN2.1	IN2.0	0000 0000	uuuu uuuu	*,*,*,*,*,*,*,*
19Bh	TRISC2	TC2.7	TC2.6	TC2.5	TC2.4	TC2.3	TC2.2	TC2.1	TC2.0	0000 0000	uuuu uuuu	*,*,*,*,*,*,*,*
19Ch	PT2DA	DA2.7	DA2.6	DA2.5	DA2.4	DA2.3	-	-	-	0000 0000	uuuu uuuu	*,*,*,*,*,*,*,*
19Dh	PT2PU	PU2.7	PU2.6	PU2.5	PU2.4	PU2.3	PU2.2	PU2.1	PU2.0	0000 0000	uuuu uuuu	*,*,*,*,*,*,*,*
19Eh	PT2INT	INTG2.7	INTG2.6	INTG2.5	INTG2.4	INTG2.3	INTG2.2	INTG2.1	INTG2.0	0000 0000	uuuu uuuu	*,*,*,*,*,*,*,*
19Fh	PT2INTE	INTE2.7	INTE2.6	INTE2.5	INTE2.4	INTE2.3	INTE2.2	INTE2.1	INTE2.0	0000 0000	uuuu uuuu	*,*,*,*,*,*,*,*
1A0h	PT2INTF	INTF2.7	INTF2.6	INTF2.5	INTF2.4	INTF2.3	INTF2.2	INTF2.1	INTF2.0	0000 0000	uuuu uuuu	*,*,*,*,*,*,*,*
1A1h	PT3	PT3.7	PT3.6	PT3.5	PT3.4	PT3.3	PT3.2	PT3.1	PT3.0	xxxx xxxx	xxxx xxxx	*,*,*,*,*,*,*,*
1A2h	PT3IN	IN3.7	IN3.6	IN3.5	IN3.4	IN3.3	IN3.2	IN3.1	IN3.0	0000 0000	uuuu uuuu	*,*,*,*,*,*,*,*
1A3h	TRISC3	TC3.7	TC3.6	TC3.5	TC3.4	TC3.3	TC3.2	TC3.1	TC3.0	0000 0000	uuuu uuuu	*,*,*,*,*,*,*,*
1A4h	PT3DA	DA3.7	DA3.6	DA3.5	DA3.4	DA3.3	DA3.2	DA3.1	-	0000 0000	uu.. ..uu	*,*,-,- -,-,*,*
1A5h	PT3PU	PU3.7	PU3.6	PU3.5	PU3.4	PU3.3	PU3.2	PU3.1	PU3.0	0000 0000	uuuu uuuu	*,*,*,*,*,*,*,*
1A6h	PT3INT	INTG3.7	INTG3.6	INTG3.5	INTG3.4	INTG3.3	INTG3.2	INTG3.1	INTG3.0	0000 0000	uuuu uuuu	*,*,*,*,*,*,*,*
1A7h	PT3INTE	INTE3.7	INTE3.6	INTE3.5	INTE3.4	INTE3.3	INTE3.2	INTE3.1	INTE3.0	0000 0000	uuuu uuuu	*,*,*,*,*,*,*,*
1A8h	PT3INTF	INTF3.7	INTF3.6	INTF3.5	INTF3.4	INTF3.3	INTF3.2	INTF3.1	INTF3.0	0000 0000	uuuu uuuu	*,*,*,*,*,*,*,*
1A9h	GPort0	GTBI2[1:0]		GTBI1[2:0]		GTBI0[2:0]				0000 0000	uuuu uuuu	*,*,*,*,*,*,*,*
1AAh	GPort1	GBuz[2:0]			-	GTCI2[1:0]		GTCI1[1:0]		0000 0000	uuuu uuuu	*,*,*,*,*,*,*,*
1ABh	GPort2	-	GPWM1[2:0]			-	GPWM0[2:0]			0000 0000	uuuu uuuu	*,*,*,*,*,*,*,*
1ACh	GPort3	-	GPWM3[2:0]			-	GPWM2[2:0]			0000 0000	uuuu uuuu	*,*,*,*,*,*,*,*
1ADh	GPort4	GSCL2[2:0]			GSCL[2:0]			GSPI[1:0]		0000 0000	uuuu uuuu	*,*,*,*,*,*,*,*
1AEh	GPort5	-	GTX2[2:0]			-	GTX[2:0]			0000 0000	uuuu uuuu	*,*,*,*,*,*,*,*
1AFh	CFG0	IICSE	-	-	-	GCRst	EN2CT	EN2C		0. .000	u. .uuu	*,-,-,- -,*,*,*
1B0h	ACT0	SLAVE	-	-	I2CER	START	STOP	I2CINT	ACK	0..0 0000	u..u uuuu	*,*,*,*,*,*,*,*
1B1h	STA0	MACTF	SACTF	RDBF	RWF	DFF	ACKF	GCF	ARBF	0001 0000	uuuu uuuu	*,*,*,*,*,*,*,*
1B2h	CRG0	CRG[7:0]								0000 0000	uuuu uuuu	*,*,*,*,*,*,*,*
1B3h	TOC0	I2CTF	DI2C[2:0]			I2CTLT[3:0]				0000 0000	uuuu uuuu	*,*,*,*,*,*,*,*
1B4h	RDB0	RDB0[7:1]							RDB0[0]	xxxx xxxx	uuuu uuuu	*,*,*,*,*,*,*,*
1B5h	TDB0	TDB0[7:1]							TDB0[0]	xxxx xxxx	uuuu uuuu	*,*,*,*,*,*,*,*
1B6h	SID0	SID0[7:1],The corresponding address of the 7-bit mode							SID0V[0]	0000 0000	uuuu uuuu	*,*,*,*,*,*,*,*

表 5-3 資料記憶體列表

"-"no use,"*"read/write,"w"write,"r"read,"r0"only read 0,"r1"only read 1,"w0"only write 0,"w1"only write 1

"$"for event status,"."unimplemented bit,"x"unknown,"u"unchanged,"d"depends on condition

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	ARST	IRST	R/W
1B7h	CFG2	IICSE	-	-	-	-	GCRst	ENI2CT	ENI2C	0. .000	u. .uuu	*,-,-,- -,*,*,*
1B8h	ACT2	SLAVE	-	-	I2CER	START	STOP	I2CINT	ACK	0..0 0000	u..u uuuu	*,*,*,*,*,*,*,*
1B9h	STA2	MACTF	SACTF	RDBF	RWF	DFF	ACKF	GCF	ARBF	0001 0000	uuuu uuuu	*,*,*,*,*,*,*,*
1BAh	CRG2	CRG[7:0]								0000 0000	uuuu uuuu	*,*,*,*,*,*,*,*
1BBh	TOC2	I2CTF	DI2C[2:0]			I2CTLT[3:0]				0000 0000	uuuu uuuu	*,*,*,*,*,*,*,*
1BCh	RDB2	RDB2[7:1]							RDB2[0]	xxxx xxxx	uuuu uuuu	*,*,*,*,*,*,*,*
1BDh	TDB2	TDB2[7:1]							TDB2[0]	xxxx xxxx	uuuu uuuu	*,*,*,*,*,*,*,*
1BEh	SID2	SID2[7:1],The corresponding address of the 7-bit mode							SID0V[0]	0000 0000	uuuu uuuu	*,*,*,*,*,*,*,*
1BFh	SSPCN0	ENSSP	CKP	CKE	SMP	-	-	SSPM[1:0]		0000 ..00	uuuu ..uu	*,*,*,*-,-,**
1C0h	SSPSTA0	SSPBY	SSPOV	-	-	-	-	-	BF	00.. ...0	uu.. ...u	*,*,-,- -,-,-,*
1C1h	SSPBUF0	SSP Receive/Transmit Buffer Register								xxxx xxxx	uuuu uuuu	*,*,*,*,*,*,*,*
1C2h	UR2CN	ENSP	ENTX	TX9	TX9D	PARITY	-	-	WUE	0000 0..0	uuuu u..u	*,*,*,*,*-,-,*
1C3h	UR2STA	-	RC9D	PERR	FERR	OERR	RCIDL	TRMT	ABDOVF	.000 0010	.uuu uuuu	-,r,r,r r,r,r,rw 0
1C4h	BA2CN	UART2SE	-	-	-	ENCR	RC9	ENADD	ENABD	0... 0000	u... uuuu	*,-,-,- *,*,*'
1C5h	BG2RH	-	-	-	UART2 Baud Rate Register High Byte					...x xxxx	...u uuuu	-,-,-,-,*,*,*,*
1C6h	BG2RL	UART2 Baud Rate Generator Register Low Byte								xxxx xxxx	uuuu uuuu	*,*,*,*,*,*,*,*
1C7h	TX2R	UART2 Transmit Register								xxxx xxxx	uuuu uuuu	*,*,*,*,*,*,*,*
1C8h	RC2REG	UART2 Receive Register								xxxx xxxx	uuuu uuuu	r,r,r,r r,r,r,r
1C9h	FWRST	FWRST data register[7:0]								0000 0000	uuuu uuuu	*,*,*,*,*,*,*,*
1CAh	-	-	-	-	-		-	-	-	0000 0000	0000 0000	r,r,r,r *,*,*,*
1CBh	-	-						-		0000 0000	0000 0000	*,*,*,*,*,*,*,*
1CCh	-	-								0000 0000	0000 0000	*,*,*,*,*,*,*,*
1CDh	-							-		xxxx xxxx	xxxx xxxx	r,r,r,r r,r,r,r
1CEh	-	-								xxxx xxxx	xxxx xxxx	r,r,r,r r,r,r,r
1CFh	-		-							xxxx xxxx	xxxx xxxx	r,r,r,r r,r,r,r
1D0h	-	-					-			0000 0000	0000 0000	*,*,*,*,*,*,*,*
080h ~ 0FFh		SRAM as 128Byte								uuuu uuuu	uuuu uuuu	*,*,*,*,*,*,*,*
100h ~ 17Fh		SRAM as 128Byte								uuuu uuuu	uuuu uuuu	*,*,*,*,*,*,*,*
200h ~ 2FFh		SRAM as 256Byte								uuuu uuuu	uuuu uuuu	*,*,*,*,*,*,*,*
300h ~ 37Fh		BIE2 Data Buffer (128Byte)								uuuu uuuu	uuuu uuuu	*,*,*,*,*,*,*,*

表 5-4 資料記憶體列表

6. 電氣特性

Absolute Maximum Ratings :

Absolute maximum ratings over operating free-air temperature (unless otherwise noted)

Voltage applied at V_{DD} to V_{SS} . . . . −0.2 V to 6.0 V

Voltage applied to any pin . . . . −0.2 V to V_{DD} + 0.3 V

Diode current at any device terminal . . . . ±2 mA

Storage temperature, ... −55℃ to 125℃

(Operation Mode) . . . . −40℃ to 85℃

Total power dissipation. 0.5w

Maximum output current sink by any I/O pin. 20mA

6.1. Recommended operating conditions

T_A = -40℃ ~ 85℃,unless otherwise noted

Sym.	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V_{DD}	Supply Voltage	All digital peripherals and CPU V_{DD} = 1.9V~5.5V, Frequency<=9.6MHz, V_{DD} = 3.6V~5.5V, Frequency<=16MHz,	1.9		5.5	V
V_{DDA}	Supply Voltage	Analog peripherals	2.4		5.5	
V_{SS}	Supply Voltage		0		0	

6.2. Internal RC Oscillator

T_A = 25℃,VDD = 3.0V,unless otherwise noted

Sym.	Parameter	Test Conditions		Min.	Typ.	Max.	Unit
HAO	High Speed Oscillator frequency, After writer Trim.	ENHAO[0]=1b, HAOM[1:0]=00b	VDD=3V/5V, T_A = 25℃	-1%	1.843	+1%	MHz
			VDD=3V/5V, T_A = -40℃~ 85℃	-3%	1.843	+3%	
			VDD=2.2V~5.5V, T_A = 25℃	-3%	1.843	+3%	
			VDD=2.2V~5.5V, T_A = -40℃~ 85℃	-6%	1.843	+6%	
		ENHAO[0]=1b, HAOM[1:0]=01b	VDD=3V/5V, T_A = 25℃	-1%	4.147	+1%	MHz
			VDD=3V/5V, T_A = -40℃~ 85℃	-3%	4.147	+3%	
			VDD=2.2V~5.5V, T_A = 25℃	-3%	4.147	+3%	
			VDD=2.2V~5.5V, T_A = -40℃~ 85℃	-6%	4.147	+6%	
		ENHAO[0]=1b, HAOM[1:0]=10b	VDD=3V/5V, T_A = 25℃	-1%	8.755	+1%	MHz
			VDD=3V/5V, T_A = -40℃~ 85℃	-3%	8.755	+3%	
			VDD=2.2V~5.5V, T_A = 25℃	-4%	8.755	+4%	
			VDD=2.2V~5.5V, T_A = -40℃~ 85℃	-8%	8.755	+8%	
		ENHAO[0]=1b, HAOM[1:0]=11b	VDD=3.6V/5V, T_A = 25℃	-1%	17.51	+1%	MHz
			VDD=3.6V/5V, T_A = -40℃~ 85℃	-3%	17.51	+3%	
			VDD=3.6V~5.5V, T_A = 25℃	-2%	17.51	+2%	
			VDD=3.6V~5.5V, T_A = -40℃~ 85℃	-5%	17.51	+5%	

LPO	Low Power Oscillator	VDD=2.2V~5.5V, T_A = 25℃	-20%	14.5	+20%	KHz

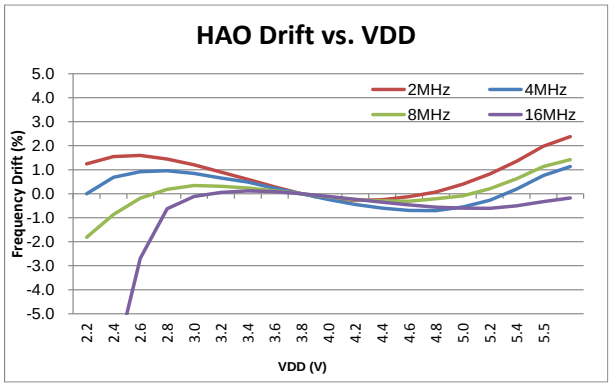


Figure 6.2-1 HAO vs. VDD

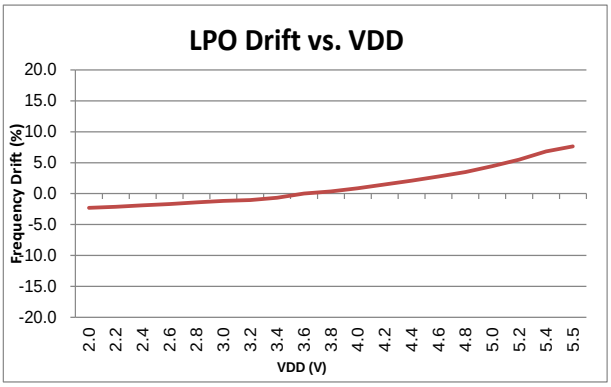


Figure 6.2-2 LPO vs. VDD

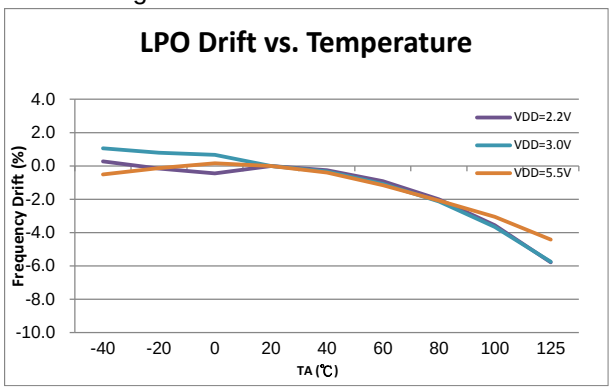


Figure 6.2-3 LPO vs. Temperature

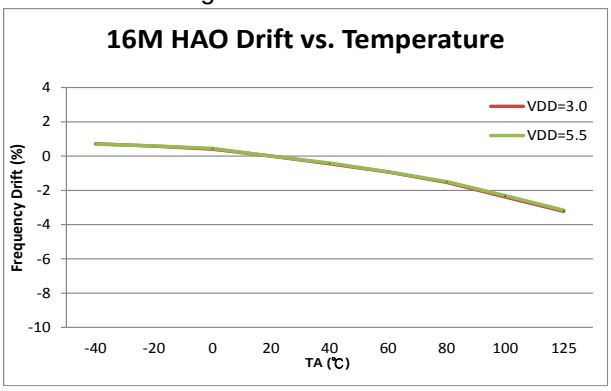


Figure 6.2-4 HAO(17.51MHz) vs. Temperature

6.3. Supply current into VDD excluding peripherals current

T_A = 25℃,V_{DD} = 3.0V,OSC_LPO = 14KHz, BOR2 OFF, OSC_CY = off, unless otherwise noted

Sym.	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
I_{AM1}	Active mode 1	OSC_HAO = 17.51MHz, CPU_CK = 17.51MHz		1700	2500	uA
I_{AM5}	Active mode 5	OSC_HAO = 4.147MHz, CPU_CK = OSC_HAO		785	1200	uA
I_{LP1}	Low Power 1	OSC_HAO=off, CPU_CK = LPO		490	735	uA
I_{LP2}	Low Power 2	OSC_HAO=off, CPU_CK = LPO, Idle state		0.5	2	uA
I_{LP3}	Low Power 3	OSC_HAO=off, CPU_CK = off, Sleep state		0.1	1	uA

OSC_CY：External Oscillator frequency.
OSC_HAO：Internal High Accuracy Oscillator frequency.
CPU_CK：CPU core work frequency.

T_A = 25℃,V_{DD} = 5.5V,OSC_LPO = 14KHz, BOR2 OFF, OSC_CY = off, unless otherwise noted

Sym.	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
I_{AM1}	Active mode 1	OSC_HAO = 17.51MHz, CPU_CK = 17.51MHz		2850	4200	uA
I_{AM5}	Active mode 5	OSC_HAO = 4.147MHz, CPU_CK = OSC_HAO		1100	1650	uA
I_{LP1}	Low Power 1	OSC_HAO = off, CPU_CK = LPO		510	765	uA
I_{LP2}	Low Power 2	OSC_HAO=off, CPU_CK = LPO, Idle state		1.3	4	uA
I_{LP3}	Low Power 3	OSC_HAO=off, CPU_CK = off, Sleep state		0.3	2	uA

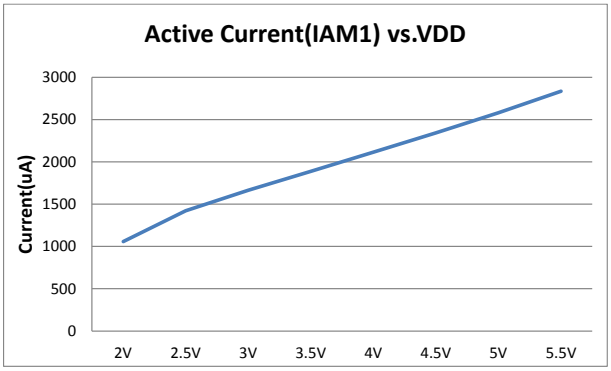


Figure 6.3-1 I_{AM1} vs. VDD

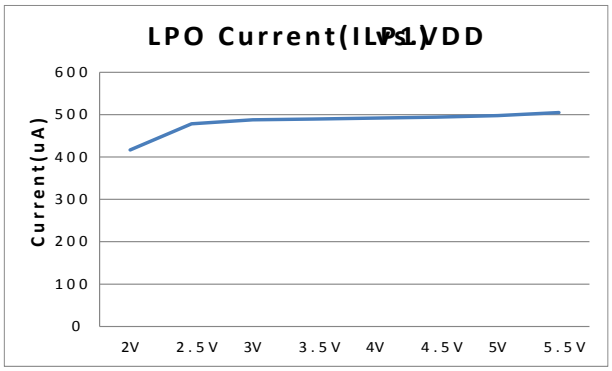


Figure 6.3-2 I_{LP1} vs. VDD

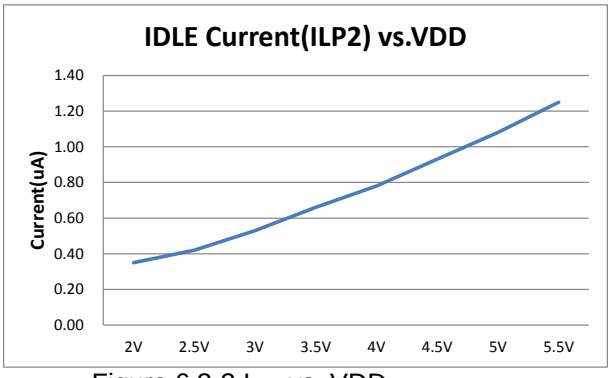


Figure 6.3-3 I_{LP2} vs. VDD

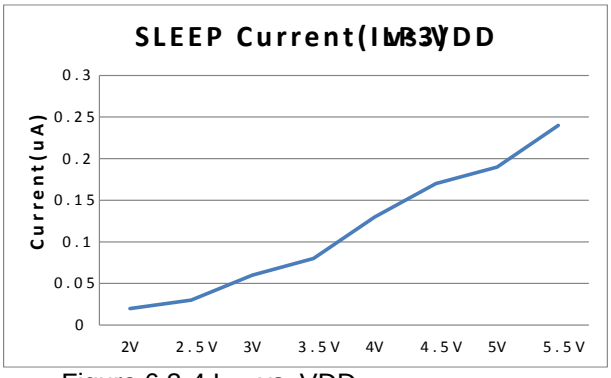


Figure 6.3-4 I_{LP3} vs. VDD

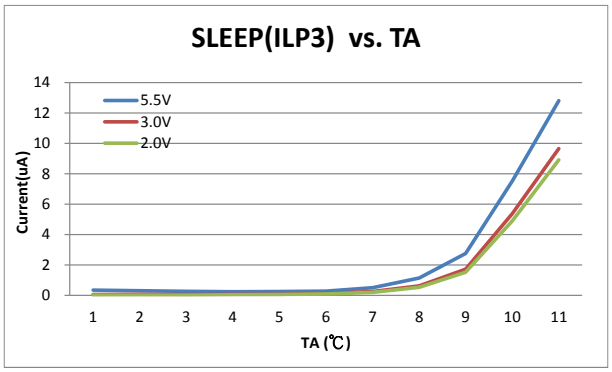


Figure 6.3-5 I_{LP3} vs. Temperature

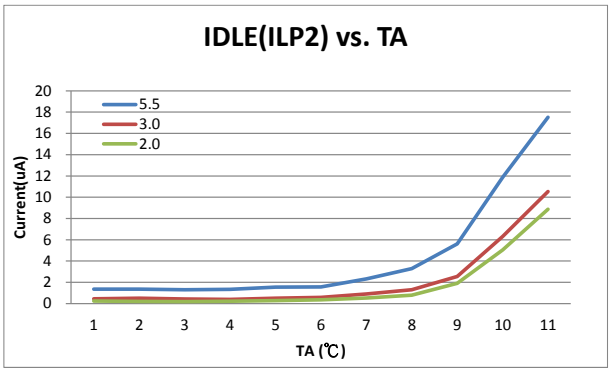


Figure 6.3-6 I_{LP2} vs. Temperature

6.4. Port 1~3

T_A = 25℃,VDD = 3.0V,unless otherwise noted

Sym.	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
Input voltage and Schmitt trigger and leakage current and timing						
V_{IH}	High-Level input voltage				0.7*VDD	V
V_{IL}	Low-Level input voltage		0.3*VDD			
V_{hys}	Input Voltage hysteresis(V_{IH} - V_{IL})			0.3*VDD		V
I_{LKG}	Leakage Current				0.1	uA
R_{PU}	Port pull high resistance			60		kΩ
Output voltage and current and frequency						
V_{OH}	High-level output voltage	VDD=3V, I_{OH}=-10mA,	V_{DD} -0.5			V
		VDD=5V, I_{OH}=-15mA,	V_{DD} -0.5			
V_{OL}	Low-level output voltage	VDD=3V, I_{OL}=10mA			V_{SS} +0.4	
		VDD=5V, I_{OL}=15mA			V_{SS} +0.4	

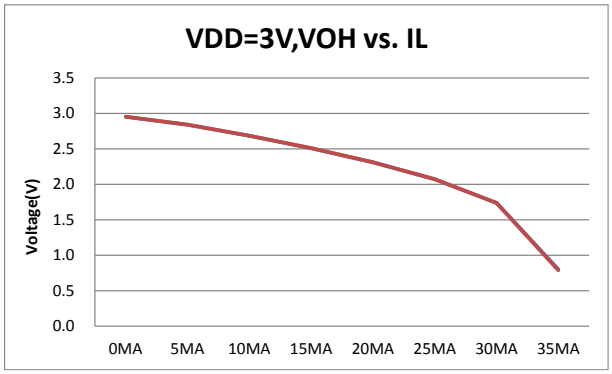


Figure 6.4-1 V_{OH} vs. I_{OH}

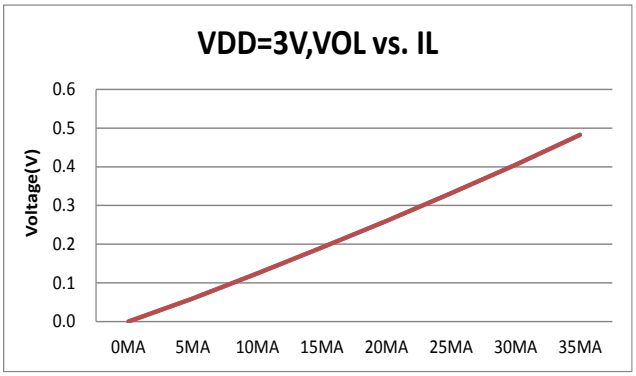


Figure 6.4-2 V_{OL} vs. I_{OL}

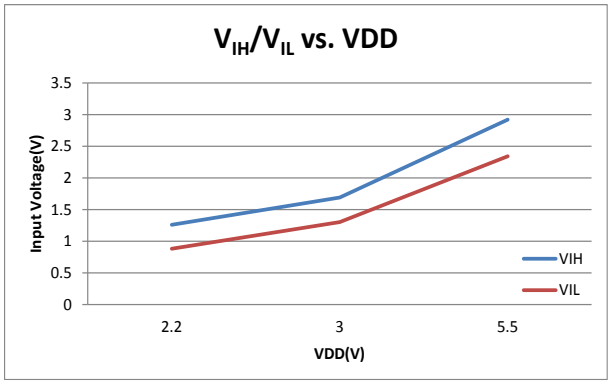


Figure 6.4-3 V_{IH}/V_{IL} vs. VDD

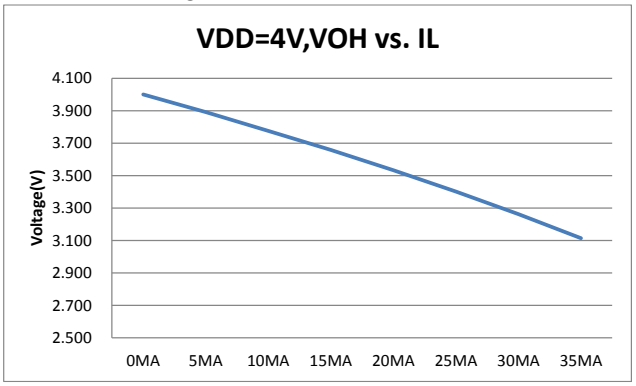


Figure 6.4-4 V_{IH}/V_{IL} vs. VDD

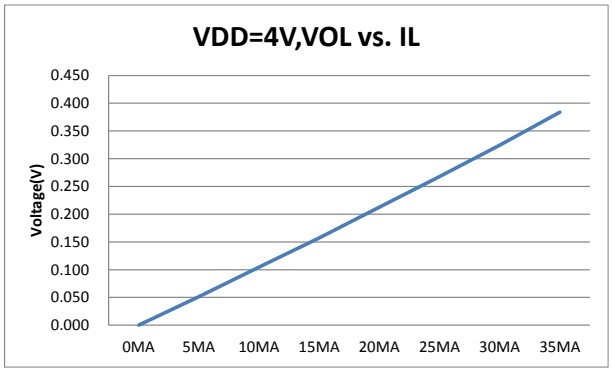


Figure 6.4-5 V_{IH}/V_{IL} vs. VDD

6.5. Reset(Brownout)

T_A = 25℃,VDD = 3.0V,unless otherwise noted

Sym.	Parameter	Test Conditions		Min.	Typ.	Max.	Unit
BOR1	Pulse length needed to accepted reset internally, t_{d-LVR1}			2			uS
	V_{DD} Start Voltage to accepted reset internally (L➔H),V_{HYS1}			1.0	1.35	1.65	V
	BOR1 current, I_{BOR1}				0.1	0.5	uA
	Temperature Drift				15		%
BOR2	Pulse length needed to accepted reset internally, t_{d-LVR2}			2			uS
	V_{DD} Start Voltage to accepted reset internally (L➔H),V_{HYS2}, and BOR_TH[2:0]:		000b	-10%	1.73	+10%	V
			001b	-10%	2.0	+10%	
			010b	-10%	2.22	+10%	
			011b	-10%	2.5	+10%	
			100b	-10%	2.72	+10%	
			101b	-10%	3.0	+10%	
			110b	-10%	3.63	+10%	
			111b	-10%	4.0	+10%	
	V_{DD} Start Voltage to accepted reset internally (H➔L),V_{LVR2}, and BOR_TH[2:0]:		000b	-10%	1.67	+10%	V
			001b	-10%	1.96	+10%	
			010b	-10%	2.17	+10%	
			011b	-10%	2.44	+10%	
			100b	-10%	2.69	+10%	
			101b	-10%	2.96	+10%	
			110b	-10%	3.58	+10%	
			111b	-10%	3.94	+10%	
	Hysteresis, $V_{HYS2-LVR2}$			25	60	90	mV
	BOR2 current, I_{BOR2}				10	15	uA
	Temperature Drift				3	5	%
MCLR	Pulse length needed as MCLR pin to accepted reset internally, t_{d-RST}			2			uS
	Input Voltage to accepted reset voltage				1.1		V
	Reset release voltage				2		V

BOR1/BOR2：Brownout Reset 1/2
LVR：Low Voltage Reset of BOR
MCLR：External Reset pin

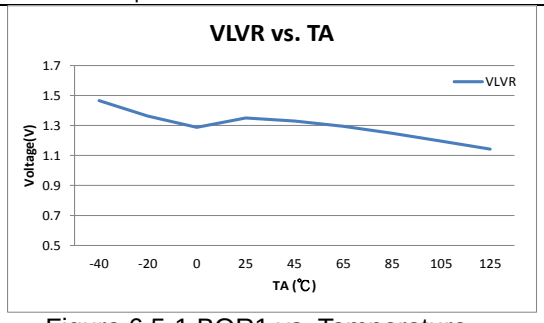


Figure 6.5-1 BOR1 vs. Temperature

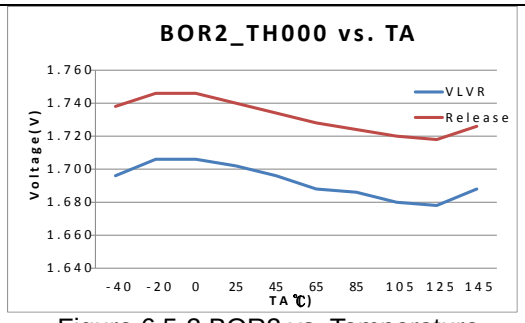


Figure 6.5-2 BOR2 vs. Temperature

6.6. Power System

T_A = 25℃,VDD = 3.0V,unless otherwise noted

Sym.	Parameter	Test Conditions		Min.	Typ.	Max.	Unit
VDDA	VDDA operation current, I_{VDDA}	I_L = 0mA	LDOC[2:0]=000b		20		uA
	Select VDDA output voltage	I_L = 0.1mA, VDD=5.5V	LDOC [2:0]=000b	-5%	2.4	+5%	V
			LDOC [2:0]=001b		2.6		
			LDOC [2:0]=010b		2.9		
			LDOC [2:0]=011b		3.3		
			LDOC [2:0]=100b		3.6		
			LDOC [2:0]=101b		4.0		
			LDOC [2:0]=110b		4.5		
			LDOC [2:0]=111b		5.0		
		I_L = 10mA, VDD=2.6V	LDOC [2:0]=000b	-6%	2.4	+5%	
	Dropout voltage	VDD=2.9V, VDDA=2.9V mode (LDOC [2:0]=010b), IL = 10mA			200		mV
	Temperature drift	LDOC [2:0]=000b I_L = 0.1mA	T_A=-40℃~85℃		50		PPM/℃
	V_{DD} Voltage drift	LDOC [2:0]=000b	V_{DD}=2.2V~5.5V		±0.2		%/V
ACM	operation current, I_{ACM}		ENVCM[0]=1b		50		uA
	Internal ADC common mode voltage, V_{ACM}	ENVCM[0]=1b	VCMS[0]=0b, SELVIN[0]=0b		VDDA/2		
			VCMS[0]=0b, SELVIN[0]=1b		1.2		V
			VCMS[0]=1b,		REFO		
VDDA：Adjust Voltage Regulator ACM：Internal ADC common mode voltage							

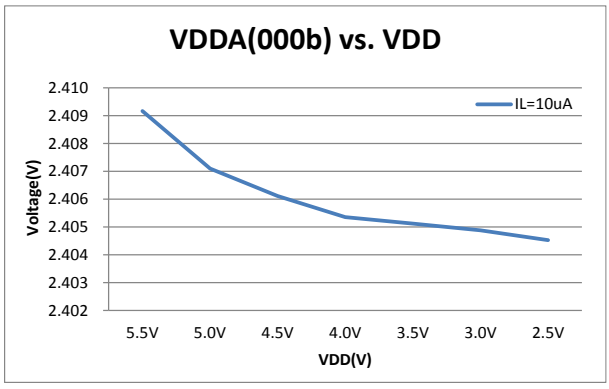


Figure 6.6-1 VDDA(000b) vs. VDD

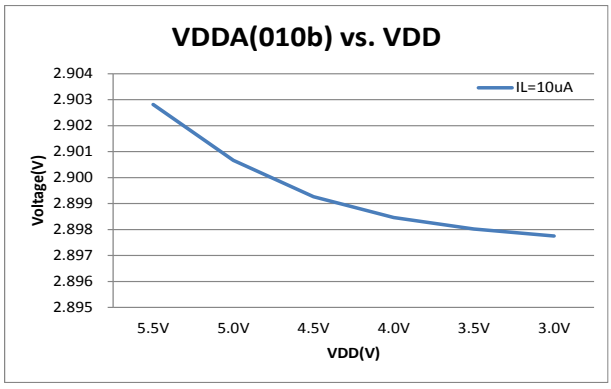


Figure 6.6-2 VDDA(010b) vs. VDD

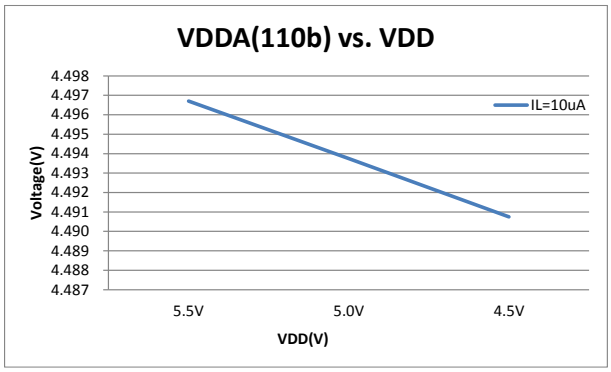


Figure 6.6-3 VDDA(110b) vs. VDD

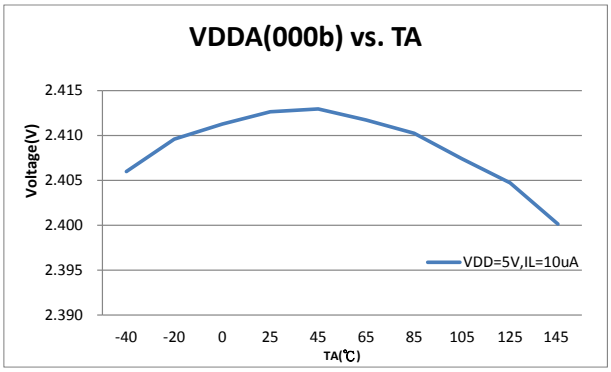


Figure 6.6-4 VDDA(000b) vs. Temperature

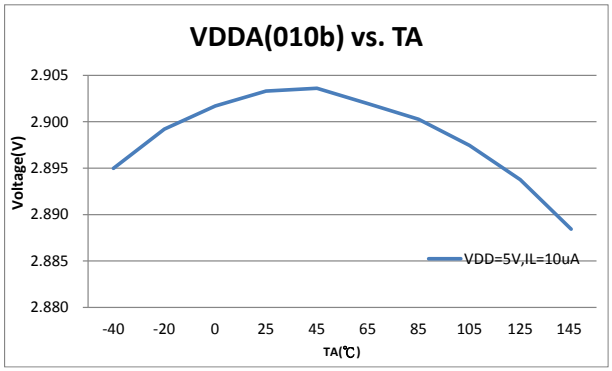


Figure 6.6-5 VDDA(010b) vs. Temperature

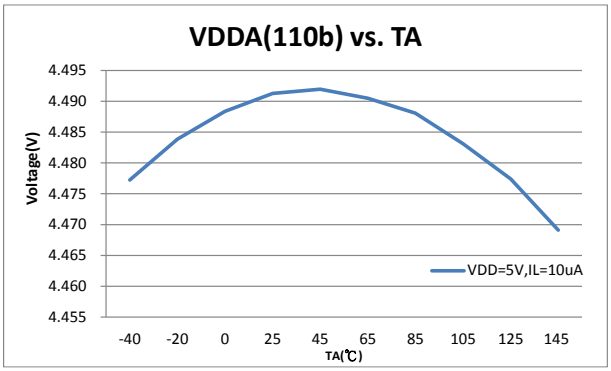


Figure 6.6-6 VDDA(110b) vs. Temperature

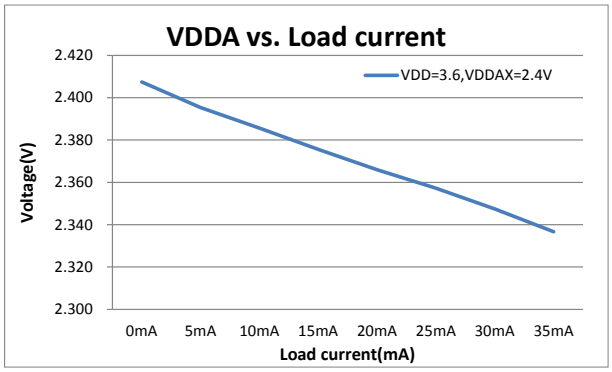


Figure 6.6-7 VDDA vs. Load current

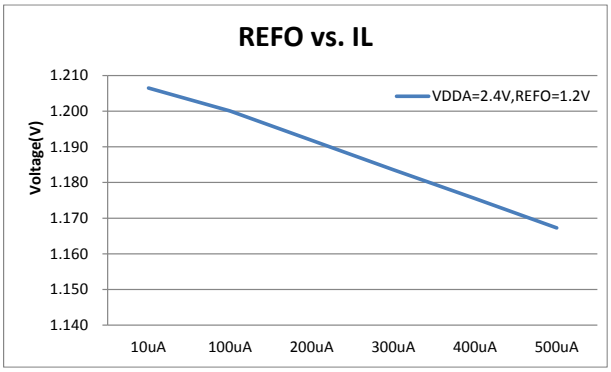


Figure 6.6-8 REFO vs. Load current

6.7. Multi-Comparator

T_A = 25℃,V_{DD} = 3.0V, unless otherwise noted.

Sym.	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
I_{MC}	Operation supply current	ENCMP[0]=1, CMPHS[0]=1b		5		uA
	Low Power Mode	ENCMP[0]=1, CMPHS [0]=0b		1		
V_{IC}	Common-mode input voltage		0		V_{DD}-1	V
V_{OS}	Offset voltage		-5		5	mV
V_{hys}	Input hysteresis		0	0.7	1.5	mV
V_{accy}	Reference Voltage	ENLDO[0]=1b, CPPS[1:0]=11b, VRSEL[0]=1b	1.15	1.2	1.25	V
	Temperature Drift			50		ppm/℃
	VDD Voltage drift			±0.2		%/V
I_R	Multi-node resistor current	CPRL[0]=0b		10		uA
		CPRL[0]=1b		30		
	ENLDO[0]=1b,CPPS[1:0]=11b,CPRH[1:0]=01b,CPRL[0]=0b.	CPDA[4:0]=00011b	-5%	3.89	5%	V
		CPDA[4:0]=00100b		3.73		
		CPDA[4:0]=00101b		3.58		
		CPDA[4:0]=00110b		3.44		
		CPDA[4:0]=00111b		3.31		
		CPDA[4:0]=01000b		3.19		
		CPDA[4:0]=01001b		3.08		
		CPDA[4:0]=01010b		2.98		
		CPDA[4:0]=01011b		2.88		
		CPDA[4:0]=01100b		2.79		
		CPDA[4:0]=01101b		2.71		
		CPDA[4:0]=01110b		2.63		
		CPDA[4:0]=01111b		2.55		
		CPDA[4:0]=10000b		2.48		
		CPDA[4:0]=10001b		2.42		
		CPDA[4:0]=10010b		2.35		
		CPDA[4:0]=10011b		2.29		
		CPDA[4:0]=10100b		2.24		
		CPDA[4:0]=10101b		2.18		
		CPDA[4:0]=10110b		2.13		
		CPDA[4:0]=10111b		2.08		
		CPDA[4:0]=11000b		2.03		
		CPDA[4:0]=11001b		1.99		
		CPDA[4:0]=11010b		1.94		

		CPDA[4:0]=11011b		1.90		
		CPDA[4:0]=11100b		1.86		
		CPDA[4:0]=11101b		1.82		
	CPDA[4:0]=00000b~00010b, and 11110b~11111b (reserved)					

LVD：Low Voltage Detect.

6.8. ΣΔADC, Power Supply and recommended operating conditions

TA = 25℃,VDD = 3.0V, VDDA=2.4V,unless otherwise noted

Sym.	Parameter	Test Conditions		Min.	Typ.	Max.	Unit
$V_{\Sigma\Delta ADC}$	Supply Voltage at VDDA	ENLDO[0]=0		2.4		5.5	V
$f_{\Sigma\Delta ADC}$	Modulator sample frequency, ADC_CK			125	1000	1200	KHz
	Over Sample Ratio, OSR			64		65536	
$I_{\Sigma\Delta ADC}$	Operation supply current	ENAD1 [0]=1	GAIN =16, ADC_CK=1MHz		260		uA

6.9. ΣΔADC, Performance

T_A = 25℃,V_{DD}=3.3V,VDDA=2.4V,V_{VR}=(VDDA-VSS)/2,GAIN=1,fΣΔADC=1000KHz,unless otherwise noted

Sym.	Parameter	Test Conditions		Min.	Typ.	Max.	Unit
INL	Integral Nonlinearity(INL)	VDDA=2.4V,V_{VR}= VDDA/2, ΔSI=±450mV			±0.003	±0.01	%FSR
	No Missing Codes[3]	ADC_CK=1000KHz,OSR[3:0]=0000b		23			Bits
$G_{\Sigma\Delta ADC}$	Temperature drift Gain x16	T_A = -40℃~ 85℃			20		ppm/℃
E_{OS}	Offset error of Full Scale Rang input voltage range with Chopper	ΔAI=0V ΔVR=1.2V DCSET[3:0]=0000b *ΔAI is external short Gain Normalized	Gain=2			1	%FSR
	Offset temperature drift with Chopper mode		GAIN=1		0.021		uV/℃
			GAIN=2		0.026		
			GAIN=4		0.03		
			GAIN=16		0.45		
$CM_{\Sigma\Delta ADC}$	Common-mode rejection	V_{CM}=0.7V to 1.7V, V_{VR}= 1.0V	V_{SI}=0V, GAIN=1		90		dB
			V_{SI}=0V, GAIN=16		75		dB
PSRR	DC power supply rejection	VDDA=3.0V,ΔVDDA =±100mV, V_{VR}=1.0V, V_{SI}=1.2V,V_{SI-}=1.2V,	GAIN=1	75			dB
			GAIN=16				dB

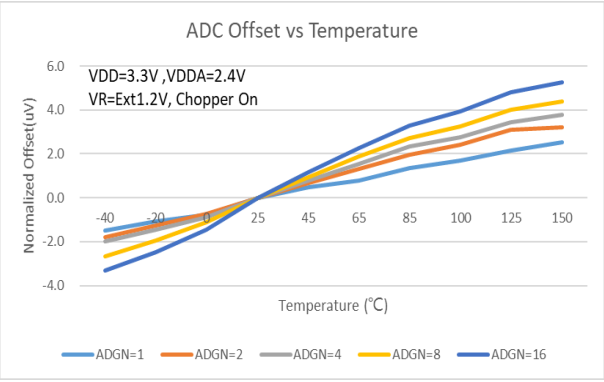


Figure 6.11-1 ADC Offset drift with Temperature

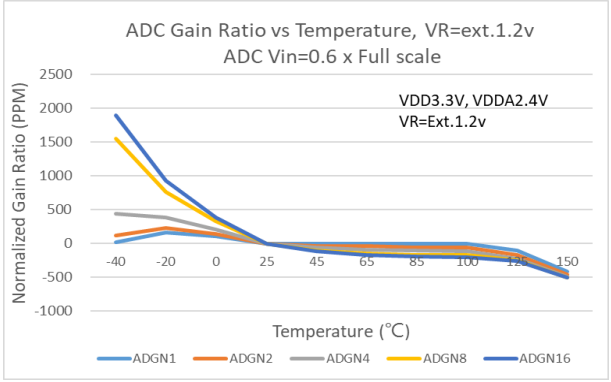


Figure 6.11-2 ADC Gain drift with Temperature

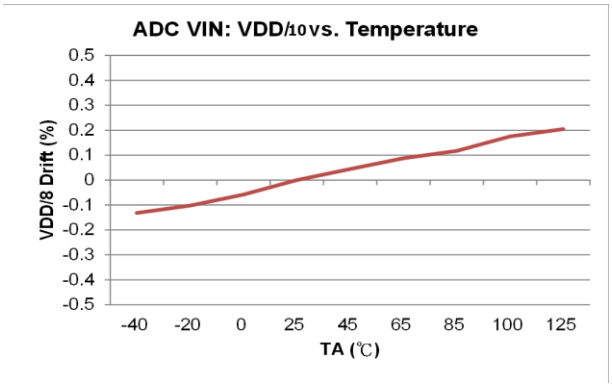


Figure 6.11-3 VDD/10 drift with Temperature

6.10. ΣΔADC Noise Performance

HY17M26 針對ΣΔADC 提供了重要的輸入雜訊規格。下表列出典型的雜訊規格表與 Gain, Output rate, 及差動最大輸入電壓等關係。測試條件設定在外部輸入訊號短路到 VDDA/2 電位下，取樣 1024 筆資料。

ENOB(RMS) with OSR/GAIN at A/D Clock=1MHz, VDDA=2.4V, VREF=V12, Chopper Off													
OSR					**64**	**128**	**256**	**512**	**1024**	**2048**	**4096**	**8196**	**16384**	**32768**	**65536**
Output rate(Hz)					**15625**	**7813**	**3906**	**1953**	**977**	**488**	**244**	**122**	**61**	**31**	**15**
Gain	**=**	**PGAGN**	**x**	**ADGN**											
0.25	**=**	**off**	**x**	**0.25**	14.47	16.21	16.89	16.48	17.62	18.62	18.97	19.43	20.01	20.45	20.71
0.5	**=**	**off**	**x**	**0.5**	14.39	16.17	16.84	16.55	17.85	18.36	18.92	19.39	19.83	20.28	20.66
1	**=**	**off**	**x**	**1**	14.16	16.13	16.8	16.67	18.01	18.2	18.72	19.2	19.69	20.08	20.36
2	**=**	**off**	**x**	**2**	13.83	15.91	16.49	16.45	17.5	17.99	18.32	18.77	19.39	19.91	20.17
4	**=**	**off**	**x**	**4**	13.19	15.68	16.27	16.55	17.21	17.8	18.06	18.36	19.05	19.42	19.59
8	**=**	**off**	**x**	**8**	13.99	15.4	15.96	16.16	16.89	17.25	17.24	17.65	18.57	19.02	19.44
16	**=**	**off**	**x**	**16**	11.96	14.91	15.44	15.27	16.12	16.41	16.27	16.59	17.76	18.68	18.77
RMS Noise(uV) with OSR/GAIN at A/D Clock=1MHz, VDDA=2.4V, VREF=V12, Chopper Off															
OSR					**64**	**128**	**256**	**512**	**1024**	**2048**	**4096**	**8196**	**16384**	**32768**	**65536**
Output rate(Hz)					**15625**	**7813**	**3906**	**1953**	**977**	**488**	**244**	**122**	**61**	**31**	**15**
Gain	**=**	**PGAGN**	**x**	**ADGN**											
0.25	**=**	**off**	**x**	**0.25**	423.20	126.66	78.98	104.91	47.63	23.85	18.74	13.59	9.12	6.71	5.61
0.5	**=**	**off**	**x**	**0.5**	224.02	65.01	40.84	49.96	20.25	14.30	9.66	6.98	5.14	3.78	2.90
1	**=**	**off**	**x**	**1**	130.78	33.53	20.97	23.02	9.10	7.99	5.58	3.99	2.83	2.17	1.78
2	**=**	**off**	**x**	**2**	82.66	19.56	13.00	13.39	6.47	4.60	3.68	2.68	1.75	1.22	1.01
4	**=**	**off**	**x**	**4**	64.21	11.45	7.58	6.25	3.95	2.63	2.19	1.78	1.11	0.85	0.76
8	**=**	**off**	**x**	**8**	18.44	6.96	4.70	4.09	2.47	1.93	1.94	1.46	0.77	0.56	0.42
16	**=**	**off**	**x**	**16**	37.63	4.89	3.38	3.78	2.11	1.72	1.90	1.52	0.68	0.36	0.34

Table 6.12-1(a) ΣΔADC ENOB and RMS Noise Table

ENOB(RMS) with OSR/GAIN at A/D Clock=1MHz, VDDA=2.4V, VREF=V12, Chopper On													
OSR					**64**	**128**	**256**	**512**	**1024**	**2048**	**4096**	**8196**	**16384**	**32768**	**65536**
Output rate(Hz)					**5208**	**2604**	**1302**	**651**	**326**	**163**	**122**	**61**	**31**	**15**	**8**
Gain	**=**	**PGAGN**	**x**	**ADGN**											
0.25	**=**	**off**	**x**	**0.25**	15.58	17.05	17.64	18.13	18.61	19.3	19.63	20.15	20.63	21.06	21.59
0.5	**=**	**off**	**x**	**0.5**	15.62	16.81	17.64	18.06	18.67	19.16	19.52	19.92	20.43	20.86	21.45
1	**=**	**off**	**x**	**1**	15.45	16.69	17.56	17.99	18.5	18.92	19.27	19.82	20.29	20.81	21.22
2	**=**	**off**	**x**	**2**	15.43	16.3	17.25	17.63	18.21	18.53	18.8	19.29	20.05	20.5	20.89
4	**=**	**off**	**x**	**4**	15.34	16.18	16.9	17.43	17.8	18.15	18.27	18.91	19.84	20.08	20.47
8	**=**	**off**	**x**	**8**	15.07	15.48	16.52	16.8	17.3	17.45	17.55	18.05	19.26	19.75	20.12
16	**=**	**off**	**x**	**16**	14.91	14.53	15.89	16.18	16.43	16.4	16.35	16.87	18.71	19.17	19.58
ENOB(RMS) with OSR/GAIN at A/D Clock=1MHz, VDDA=2.4V, VREF=V12, Chopper On													
OSR					**64**	**128**	**256**	**512**	**1024**	**2048**	**4096**	**8196**	**16384**	**32768**	**65536**
Output rate(Hz)					**5208**	**2604**	**1302**	**651**	**326**	**163**	**122**	**61**	**31**	**15**	**8**
Gain	**=**	**PGAGN**	**x**	**ADGN**											
0.25	**=**	**off**	**x**	**0.25**	195.81	70.91	46.96	33.52	24.07	14.90	11.87	8.25	5.93	4.38	3.05
0.5	**=**	**off**	**x**	**0.5**	95.23	41.74	23.56	17.53	11.50	8.19	6.37	4.85	3.39	2.53	1.67
1	**=**	**off**	**x**	**1**	53.79	22.65	12.44	9.24	6.47	4.86	3.79	2.59	1.87	1.31	0.98
2	**=**	**off**	**x**	**2**	27.26	14.83	7.67	5.91	3.95	3.17	2.64	1.88	1.11	0.81	0.62
4	**=**	**off**	**x**	**4**	14.51	8.09	4.91	3.39	2.64	2.06	1.90	1.22	0.64	0.54	0.41
8	**=**	**off**	**x**	**8**	8.75	6.58	3.20	2.62	1.86	1.68	1.57	1.11	0.48	0.34	0.26
16	**=**	**off**	**x**	**16**	4.88	6.32	2.47	2.03	1.70	1.74	1.79	1.26	0.35	0.25	0.19

Table 6.12-1(b) ΣΔADC ENOB and RMS Noise Table

The RMS Noise are referred to the input. The Effective Number of Bits (ENOB(RMS Bit)) is defined as:

$$\text{ENOB(RMS)} = \ln\left(\frac{\text{FSR}}{\text{RMS Noise}}\right) \Big/ \ln(2)$$

$$\text{RMS Noise} = \left(2 \times \text{VREF} \times \sqrt{\sum_{k=1}^{1024} (\text{ADO}[k] - \text{Average})^2}\right) \Big/ 2^{23}$$

$$\text{Where FSR (Full - Scale Range)} = 2 \times \text{VREF/Gain.}$$

$$\text{Average} = \frac{\sum_{k=1}^{1024} (\text{ADO}[k])}{1024}$$

6.11. ΣΔADC ,Temperature Sensor

T_A = 25℃,V_{DD} = 3.0V, VDDA=2.4V,unless otherwise noted

Sym.	Parameter	Test Conditions	Min.	Typ.	Max.	unit
TC_S	Sensor temperature drift			173		uV/℃
KT	Absolute Temperature Scale 0°K			-277		℃
TC_{ERR}	One point calibrate error temperature	Calibration at 25℃ of -40℃~85℃		±2		℃

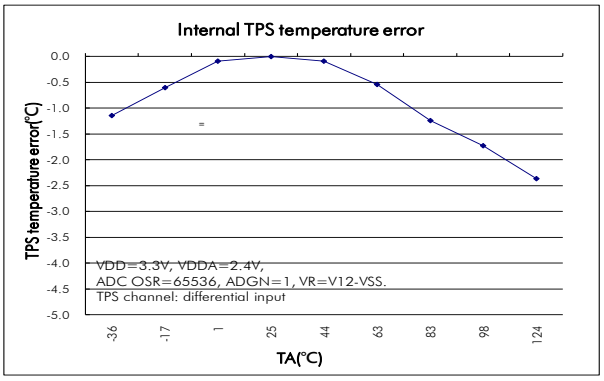


Figure 6.13-1 Internal Temperature Sensor (TPS) temperature error

6.12. MTP Memory

TA = -40℃~85℃, VDD=3V, unless otherwise noted

Sym.	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
Main MTP Program Memory/ Build-In EPROM Data Memory						
V_{DD}	Read/Write/Program/Erase Memory Operation supply Voltage		2.75		5.5	V
I_{BIEE}	Read/Write/Program/Erase Memory Operation supply current				22	mA
T_{DART}	Data retention time		10			Years
C_{MAIN}	Endurance cycles at main MTP block		100			Cycles
C_{EPROM}	Endurance cycles at EPROM block		100			Cycles

7. 訂貨資訊

下單品名 1	封裝型式	引腳數	封裝型式		程式碼	出貨包裝	個裝	材料	MSL3
			描述方式		編號 2	形式	數量	組成	
HY17M26-NS32	QFN	32	N	S32	000	Tape & Reel	5000	Green[4]	MSL-3
HY17M26-ES28	SSOP	28	E	S28	000	Tube	50	Green[4]	MSL-3
HY17M26-ES28	SSOP	28	E	S28	000	Tape & Reel	3000	Green[4]	MSL-3
HY17M26-E016	SSOP	16	E	016	000	Tube	100	Green[4]	MSL-3
HY17M26-E016	SSOP	16	E	016	000	Tape & Reel	2500	Green[4]	MSL-3

[1] **產品名稱 品名封裝型式描述方式 裝型程式碼編號（空白片 / 標準品 / 代客燒錄碼）**

例如：您的需求是 HY17M26 不帶程式碼的空白片且需要的產品是封裝片 QFN32 出貨，則下單品名為 HY17M26-NS32，並請特別註明出貨包裝形式為 Tape & Reel

例如：您的 HY17M26 代客燒錄服務申請的程式碼編號為 009，而需求的產品是封裝片 QFN32 出貨，則下單品名為 HY17M26-NS32-009，並請特別註明出貨包裝形式為 Tape & Reel

例如：您的需求是 HY17M26 不帶程式碼的空白片且需要的產品是封裝片 SSOP28 出貨，則下單品名為 HY17M26-ES28，且需以 Tape & Reel 出貨，則除下單品名外，請特別註明出貨包裝形式為 Tape & Reel

例如：您的 HY17M26 代客燒錄服務申請的程式碼編號為 009，而需求的產品是封裝片 SSOP28 出貨，則下單品名為 HY17M26-ES28-009，且需以 Tape & Reel 出貨，則除下單品名外，請特別註明出貨包裝形式為 Tape & Reel

例如：您的需求是 HY17M26 不帶程式碼的空白片且需要的產品是封裝片 SSOP16 出貨，則下單品名為 HY17M26-E016，且需以 Tube 出貨，則除下單品名外，請特別註明出貨包裝形式為 Tube

例如：您的 HY17M26 代客燒錄服務申請的程式碼編號為 007，而需求的產品是封裝片 SSOP16 出貨，則下單品名為 HY17M26-E016-007，且需以 Tube 出貨，則除下單品名外，請特別註明出貨包裝形式為 Tube

[2] 程式碼編號

“001” ~ “999” 為標準品或代客燒錄申請的程式碼編號，而空白晶片不帶此碼。

[3] MSL:

濕度敏感性等級係依據 IPC/JEDEC J-STD-020 的規範加以試驗分級，並參考 IPC/JEDEC J-STD-033 的標準處理、包裝、運輸與使用。

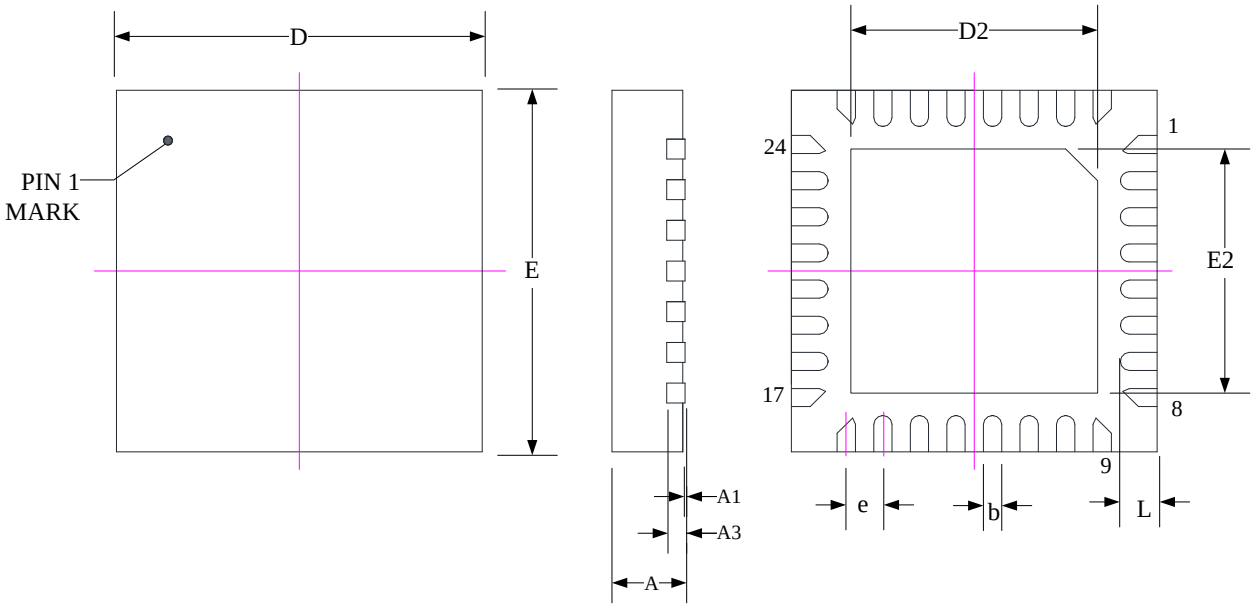
[4] Green (RoHS & no Cl/Br):

HYCON 產品皆為 Green Product，符合 RoHS 指令，REACH 高關注物質(SVHC)以及無鹵素規定 (Br<900ppm or Cl<900ppm or (Br+Cl)<1500ppm)。

8. 封裝型式資訊

8.1. QFN32(NS32)

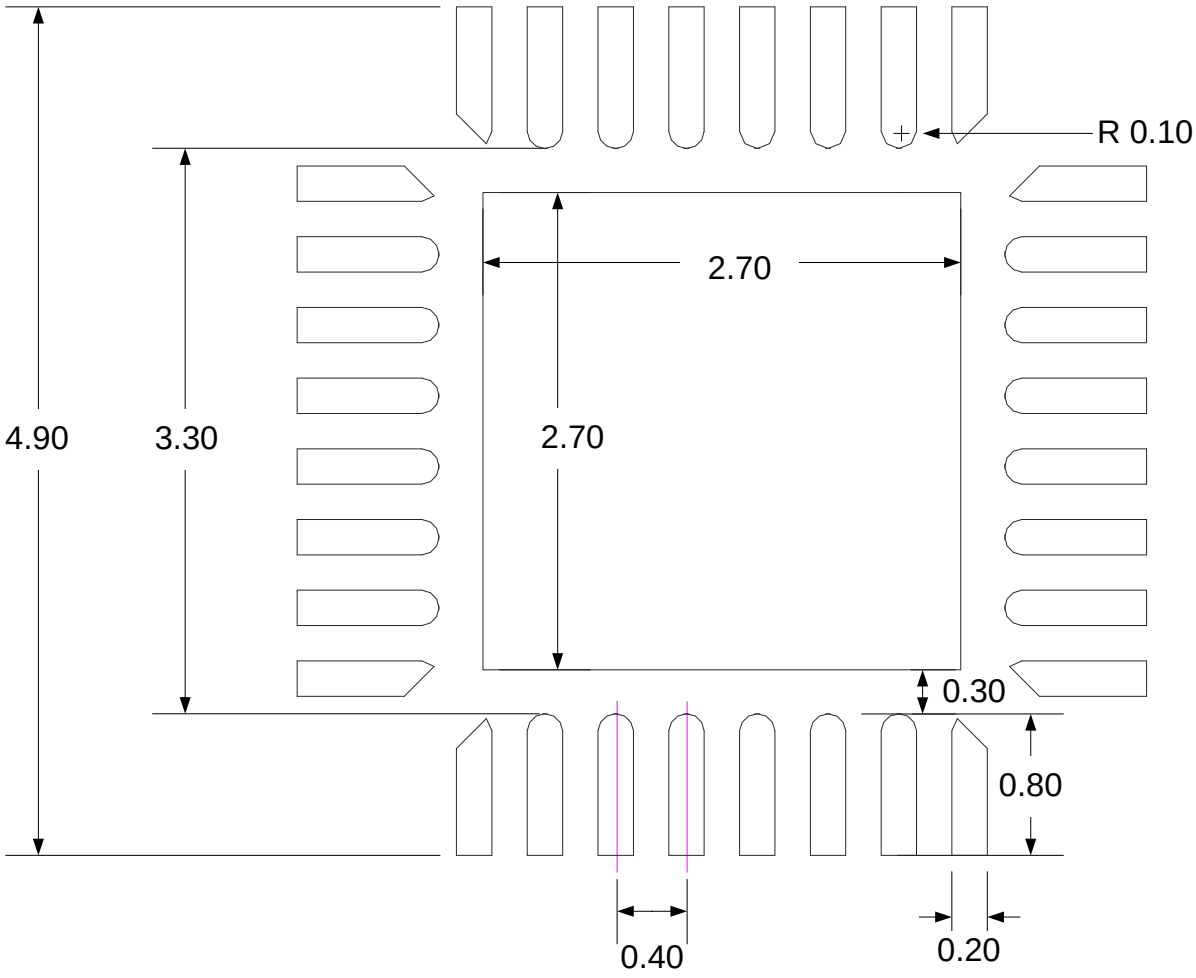
8.1.1. Package Dimensions QFN32(4x4x0.55)



SYMBOLS	MIN	NOM	MAX
A	0.50	0.55	0.60
A1	0.00	0.02	0.05
A3	0.15 REF.		
b	0.15	0.20	0.25
D	3.90	4.00	4.10
E	3.90	4.00	4.10
D2	2.65	2.70	2.75
E2	2.65	2.70	2.75
L	0.25	0.30	0.35
e	0.40 BASIC		

Note:
1. All dimensions refer to JEDEC OUTLINE MO-220.
2. Do not include Mold Flash or Protrusions.
3. Unit: mm.
4. https://www.hycontek.com/hy_mcu/QFN_DFN_PCB.pdf

8.1.2. Land Pattern Design Recommendations

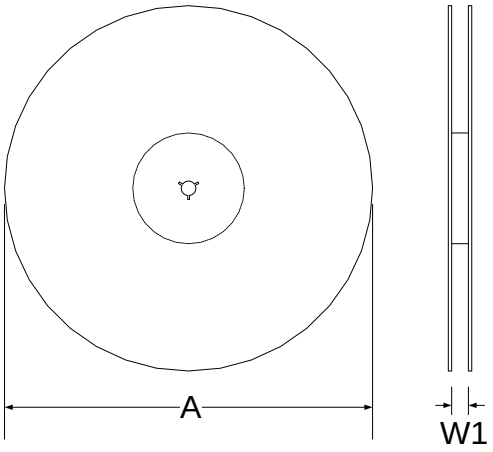


Note:
1. Publication IPC-7351 is recommended for alternate designs.
2. http://www.hycontek.com/hy_mcu/QFN_DFN_PCB.pdf
3. Unit: mm.

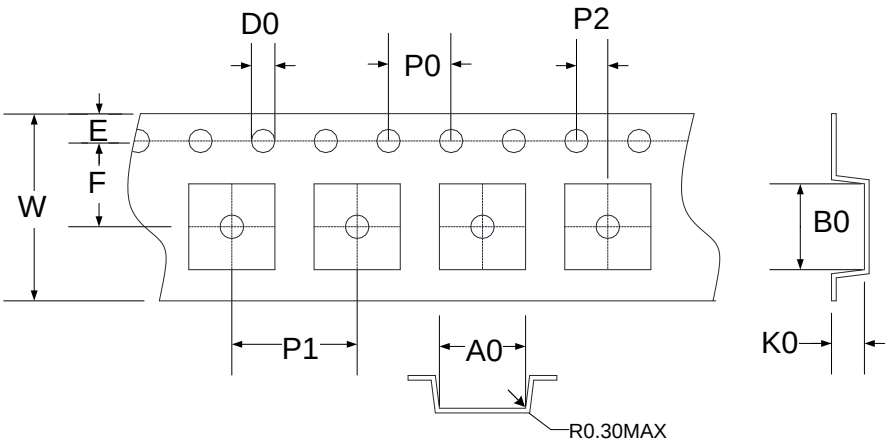
8.1.3. Tape & Reel Information

8.1.3.1. Reel Dimensions

Unit: mm



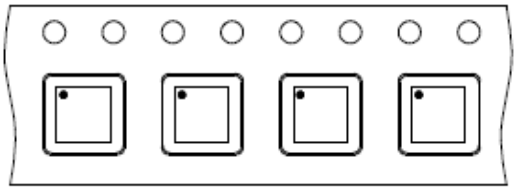
8.1.3.2. Carrier Tape Dimensions



SYMBOLS	Reel Dimensions		Carrier Tape Dimensions									
	A	W1	A0	B0	K0	P0	P1	P2	E	F	D0	W
Spec.	330	12.5	4.35	4.35	1.10	4.00	8.00	2.00	1.75	5.50	1.50	12.00
Tolerance	+6/-3	+1.5/-0	±0.10	±0.10	±0.10	±0.10	±0.10	±0.05	±0.10	±0.05	+0.1/-0	±0.30

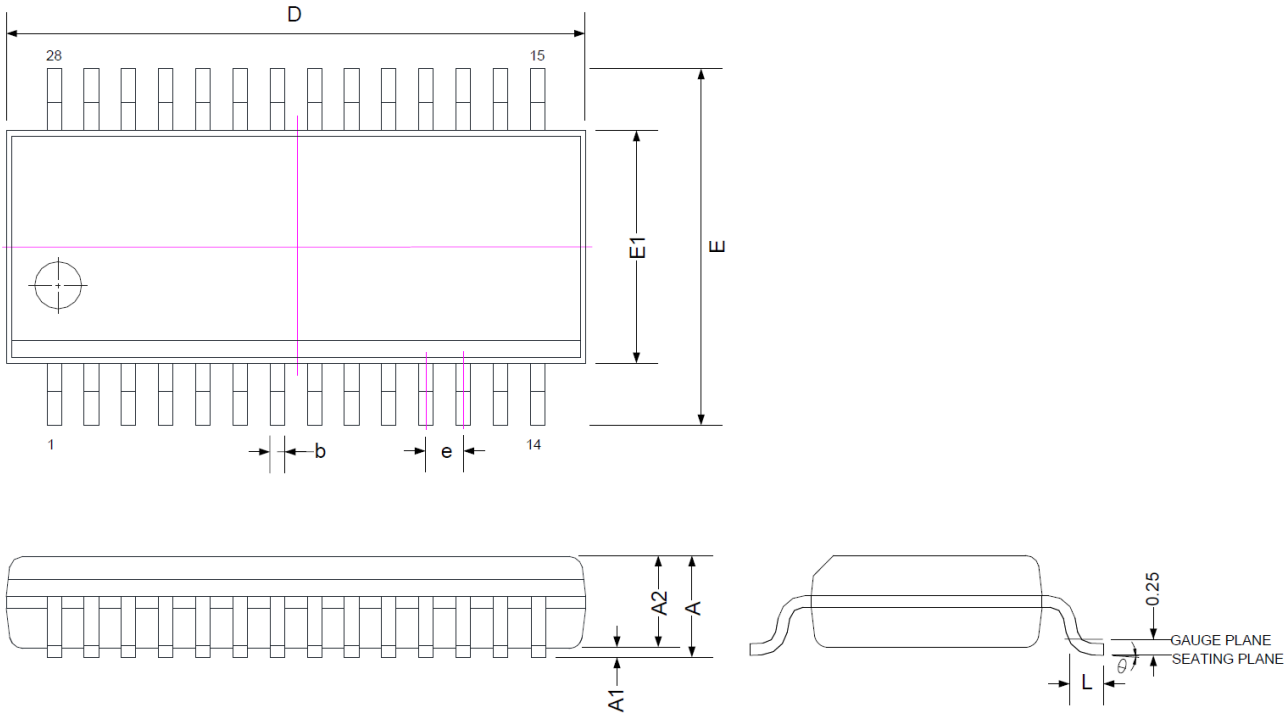
Note: 10 Sprocket hole pitch cumulative tolerance is ±0.20mm.

8.1.3.3. Pin1 direction



8.2. SSOP28(ES28)

8.2.1. Package Dimensions SSOP28(150mil)

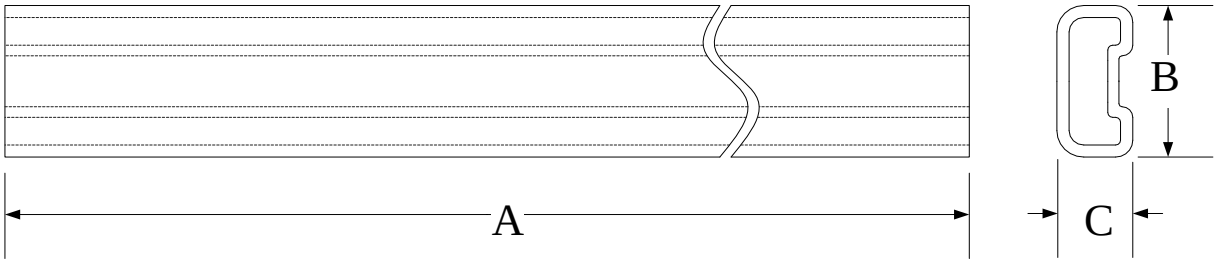


SYMBOLS	MIN	NOM	MAX
A	1.34	1.63	1.75
A1	0.10	0.15	0.25
A2	-	-	1.50
b	0.20	-	0.30
c	0.18	-	0.25
D	9.80	9.91	10.01
E1	3.81	3.91	3.99
E	5.79	5.99	6.20
L	0.41	0.64	1.27
e	0.635 BASIC		
θ°	0	-	8

Note:
1. All dimensions refer to JEDEC OUTLINE MO-137.
2. Do not include Mold Flash or Protrusions.
3. Unit: mm.

8.2.2. Tube Dimensions SSOP28(150mil)

Unit : mm

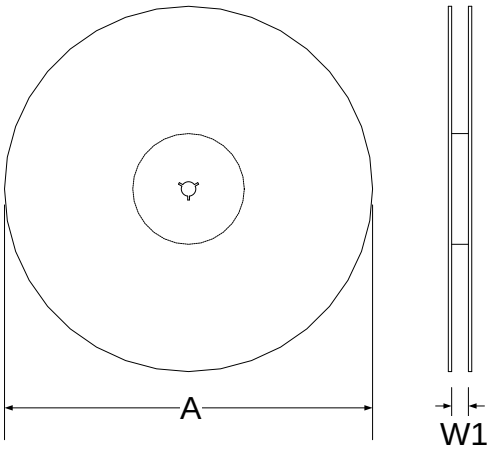


SYMBOLS	A	B	C
Spec.	529.6±1.0	8.001±0.127	3.937±0.127

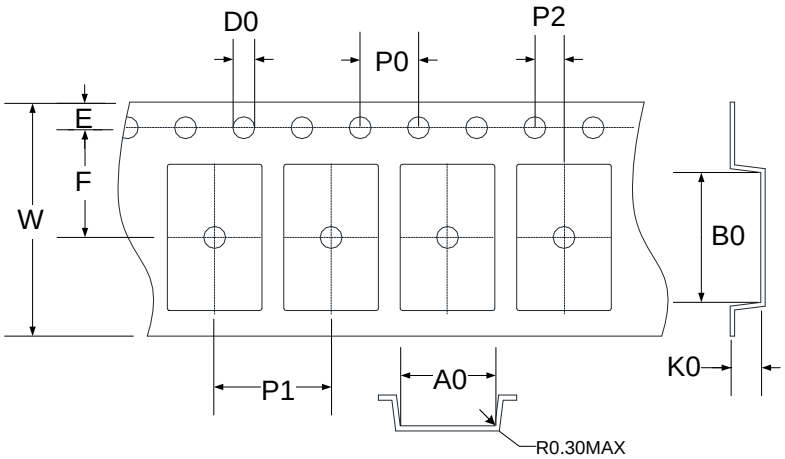
8.2.3. Tape & Reel Information

8.2.3.1. Reel Dimensions

Unit: mm



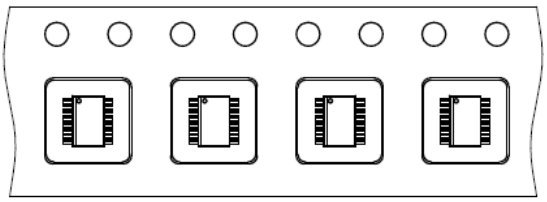
8.2.3.2. Carrier Tape Dimensions



SYMBOLS	Reel Dimensions		Carrier Tape Dimensions									
	A	W1	A0	B0	K0	P0	P1	P2	E	F	D0	W
Spec.	330	16.5	6.50	10.30	2.10	4.00	8.00	2.00	1.75	7.50	1.50	16.00
Tolerance	+6/-3	+1.5/-0	±0.10	±0.10	±0.10	±0.10	±0.10	±0.05	±0.10	±0.10	+0.1/-0	±0.30

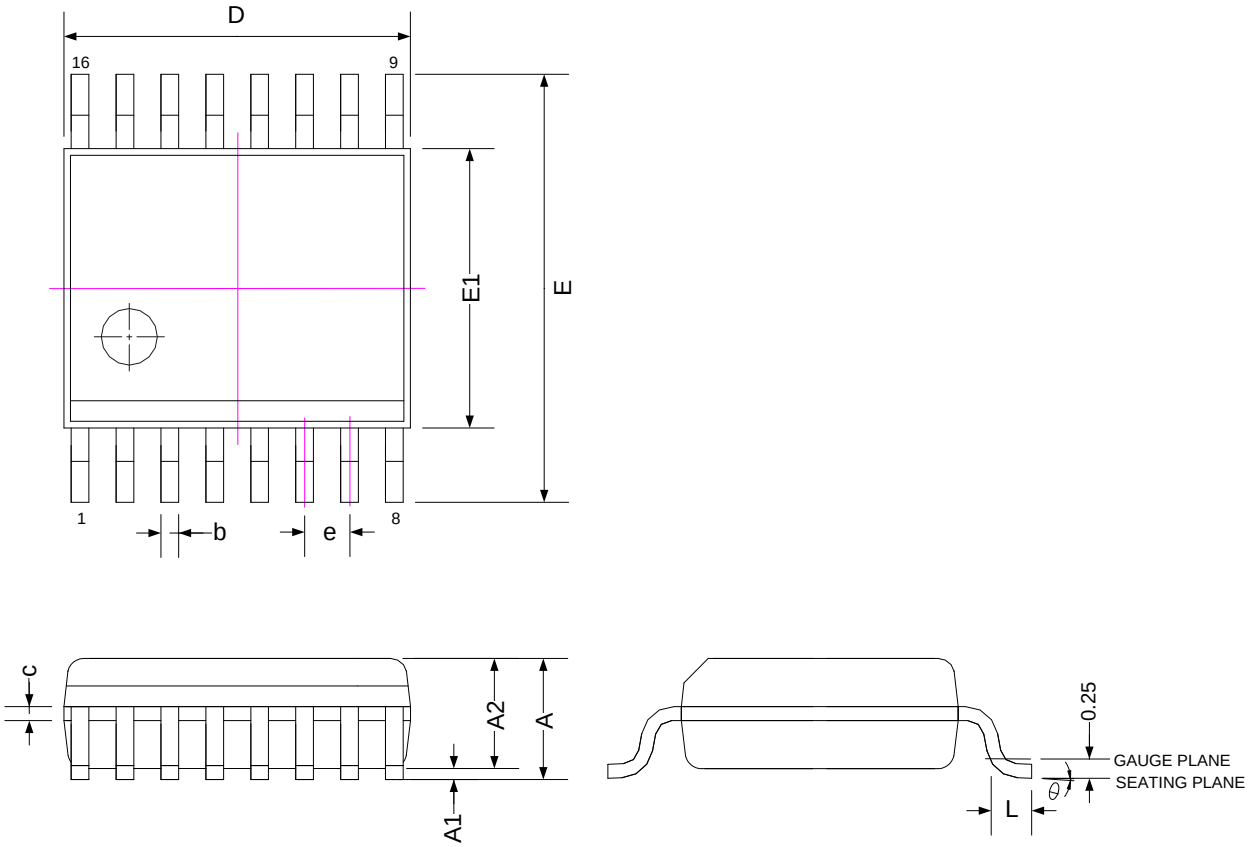
Note: 10 Sprocket hole pitch cumulative tolerance is ±0.20mm.

8.2.3.3. Pin1 direction



8.3. SSOP16(E016)

8.3.1. Package Dimensions SSOP16(150mil)



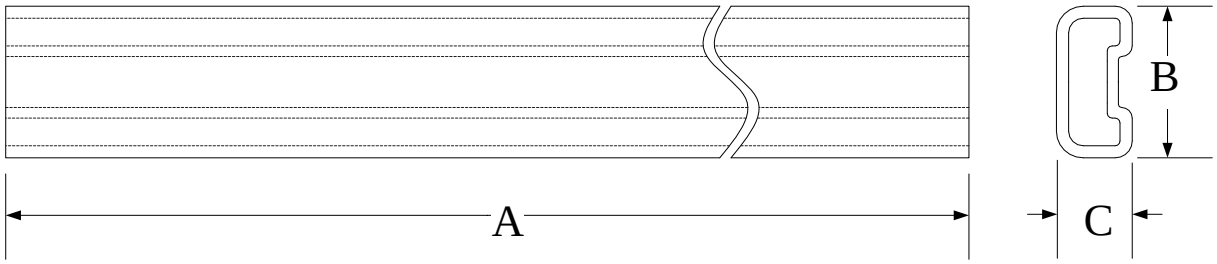
SYMBOLS	MIN	NOM	MAX
A	-	-	1.75
A1	0.10	0.15	0.25
A2	-	-	1.50
b	0.20	-	0.30
c	0.18	-	0.25
D	4.80	4.90	5.00
E1	3.81	3.91	3.99
E	5.79	5.99	6.20
L	0.41	-	1.27
e	0.635 BASIC		
θ°	0	-	8

Note:

1. All dimensions refer to JEDEC OUTLINE MO-137.
2. Do not include Mold Flash or Protrusions.
3. Unit: mm.

8.3.2. Tube Dimensions SSOP16(150mil)

Unit : mm



Type 1:

SYMBOLS	A	B	C
Spec.	521.0±1.0	7.747±0.15	3.810±0.15

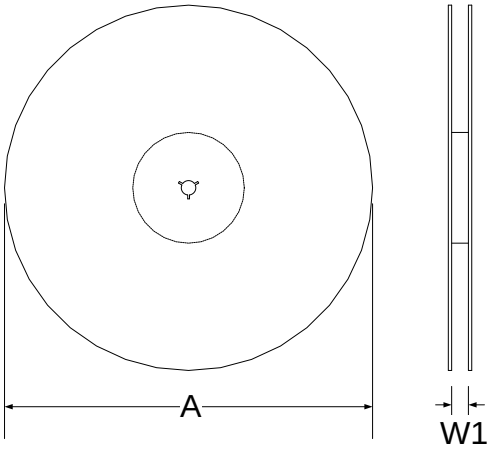
Type 2:

SYMBOLS	A	B	C
Spec.	521.0±1.0	7.874 REF.	3.810 REF.

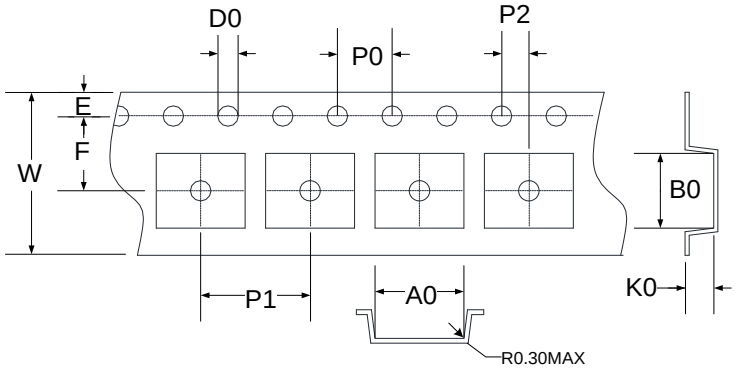
8.3.3. Tape & Reel Information

8.3.3.1. Reel Dimensions-Type1

Unit: mm



8.3.3.2. Carrier Tape Dimensions

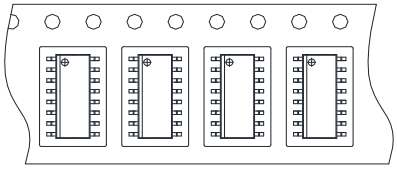


SYMBOLS	Reel Dimensions		Carrier Tape Dimensions									
	A	W1	A0	B0	K0	P0	P1	P2	E	F	D0	W
Spec.	330	12.5	6.90	5.40	2.00	4.00	8.00	2.00	1.75	5.50	1.50	12.00
Tolerance	+6/-3	+1.5/-0	±0.10	±0.10	±0.10	±0.10	±0.10	±0.05	±0.10	±0.05	+0.1/-0	±0.30

Note: 10 Sprocket hole pitch cumulative tolerance is ±0.20mm.

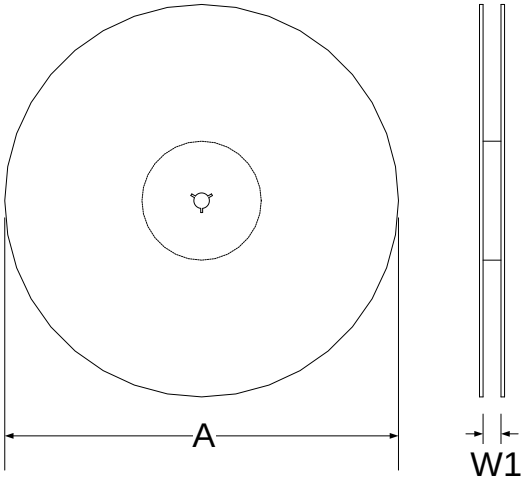
Unit : mm

8.3.3.3. Pin1 direction

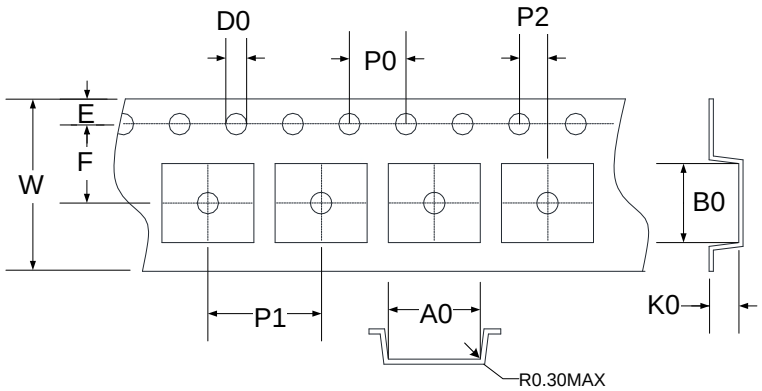


8.3.3.4. Reel Dimensions-Type2

Unit: mm



8.3.3.5. Carrier Tape Dimensions

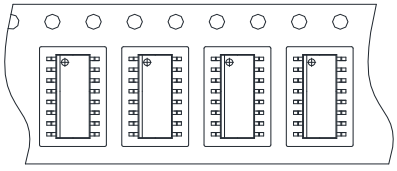


SYMBOLS	Reel Dimensions		Carrier Tape Dimensions									
	A	W1	A0	B0	K0	P0	P1	P2	E	F	D0	W
Spec.	330	12.5	6.50	5.20	2.10	4.00	8.00	2.00	1.75	5.50	1.50	12.00
Tolerance	+6/-3	+1.5/-0	±0.10	±0.10	±0.10	±0.10	±0.10	±0.05	±0.10	±0.05	+0.1/-0	±0.30

Note: 10 Sprocket hole pitch cumulative tolerance is ±0.20mm.

Unit : mm

8.3.3.6. Pin1 direction



9. 修訂記錄

以下描述本文件差異較大的地方，而標點符號與字形的改變不在此描述範圍。

文件版次	頁次	日期	摘要
V01	All	2021/09/27	初版發行
V02	All	2022/04/08	1. 更新 QFN32 產品包裝之個裝數量，移除 Die 出貨資訊 2. 更新 QFN32 產品的 Package Dimensions 為 4x4x0.55 3. LPO 中心值規格從 15kHz 修正為 14.5kHz(+/-20%) 4. MCLR 的 Reset release voltage 從 1.6V 修正為 2V 5. BOR2 規格上下限範圍修正為+/-10% 6. 暫存器總列表修正.
V03	6 7 39 50	2022/09/28	1.修改功能列表 2.QFN32 引腳 20 修正為 ECK0，引腳 21 修正為 EDIO0 3.V_{OH} 最小值修改為 VDD-0.5V 4.修改 6.12 章節名稱與內容
V04	All	2023/01/31	1. 修改 MTP/Build-In EPROM 的燒錄次數 修改前 MTP 燒錄次數 1K 次, 修改後 MTP 燒錄次數 100 次, 修改前 Build-In EPROM 燒錄次數 1K 次, 修改後 Build-In EPROM 燒錄次數 100 次. 2. 修改 BOR1 的 current Typ.數值為 0.1uA