HYCON TECHNOLOGY

HY16F3981

規格書

高精密混合信號處理控制器

4X32 ~ 6X30 LCD Driver

32-bit 低功耗微控制器

21-bit ENOB ΣΔADC

64KB Flash ROM

目錄

注意：

1、本說明書中的內容，隨著產品的改進，有可能不經過預告而更改。請客戶及時到本公司網站下載更新 http://www.hycontek.com

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8、本規格書中內容，未經本公司許可，嚴禁用於其他目的之轉載或複製。

1. 特性

數位量

- 32-bit 1T Andes Core E801 內核
- 支援 C 開發環境指令集
- 數位工作電壓 2.2V to 3.6V.
- 工作溫度-40 to 85℃
- 低功耗:
  - 運行模式: 0.6mA@CPU_CK:2MHz/2
  - 待機模式:5uA@LSRC=35KHz
  - 休眠模式:Typ.2.5uA
- 64KB Flash ROM、8KB SRAM
  - Write/Erase 的週期次數為 ：20,000 次
  - Write/Read/Erase 的操作電壓為 ：2.7V~3.6V
- 16-bit Timer A, Timer B(x2), Timer C
- 16-bit PWM 控制器及訊號捕抓功能
- 硬體實現 32-bit SPI/UART(x2)/I2C 通訊介面
- 硬體實現時鐘 RTC 萬年曆功能
- 4x32 ~ 6x30 LCD 液晶驅動器：
  1/3、1/4、1/5、1/6 Duty 及 1/3 Bias 選擇
  支援 R Type 驅動方式
  內建昇壓穩壓線路，提供 4 段 VLCD 偏壓 3.3V, 3.0V, 2.8V, or 2.6V 可透過效正函數提供 5 段 VLCD 偏壓
- 多個可編程複用型 I/O：
  數個通用型數位輸出入埠
  數個可選擇 LCD 埠或數位輸出入埠

類比量

- 類比工作電壓為 2.4V to 3.6V
- 內建低雜訊 24-bit Σ ADC：
  ADC 支援 x1~ x8 訊號放大，內建儀表放大器 IA, x4~ x32 訊號放大,最大輸入放大倍率高達 256
  輸入參考訊號可解析至 0.1uVrms(Gain=256)
  最高轉換率可達 15Ksps
- 外部高速震盪器頻率達 16MHz
- 外部低速震盪器 32768Hz
- 內建 RC 高速震盪器頻率高達 16MHz
- 內建 RC 低速震盪器頻率低至 35KHz
- 電源模塊：
  內建四段可調整穩壓電源(VDDA)
  1.2V 帶隙參考電壓(REFO)
- 軌對軌運算放大器 OPAMP：
  CMOS 輸入, 1MHz 增益帶寬
  可設計為比較器
- 12-BIT 可編程數位電阻器：
  可編程電阻分壓計
  電阻保證單調性
  搭配 OPAMP 可設計為 12-BIT DAC
- 低電壓比較器：
  低電壓檢測電路
  支援外部電壓輸入比較

Part No.	24-b ΣΔADC	Flash (byte)	SRAM (byte)	R2R OPAMP	DAC	Temp. Sensor	RTC	I/O	PWM	Serial Interface	LCD	ISP Mode	Pin
HY16F3981-L064	(7+2)-CH	64K	8K	1	12bits	Y	1	16+36	4-CH	2*UART 32bits SPI I2C	4x32 6x30	Y	LQFP64
HY16F3981-E028	(7+2)-CH	64K	8K	1	12bits	Y	1	17	4-CH	2*UART 32bits SPI I2C	-	Y	SSOP28

2. 管腳名稱定義

2.1 HY16F3981 系列管腳圖

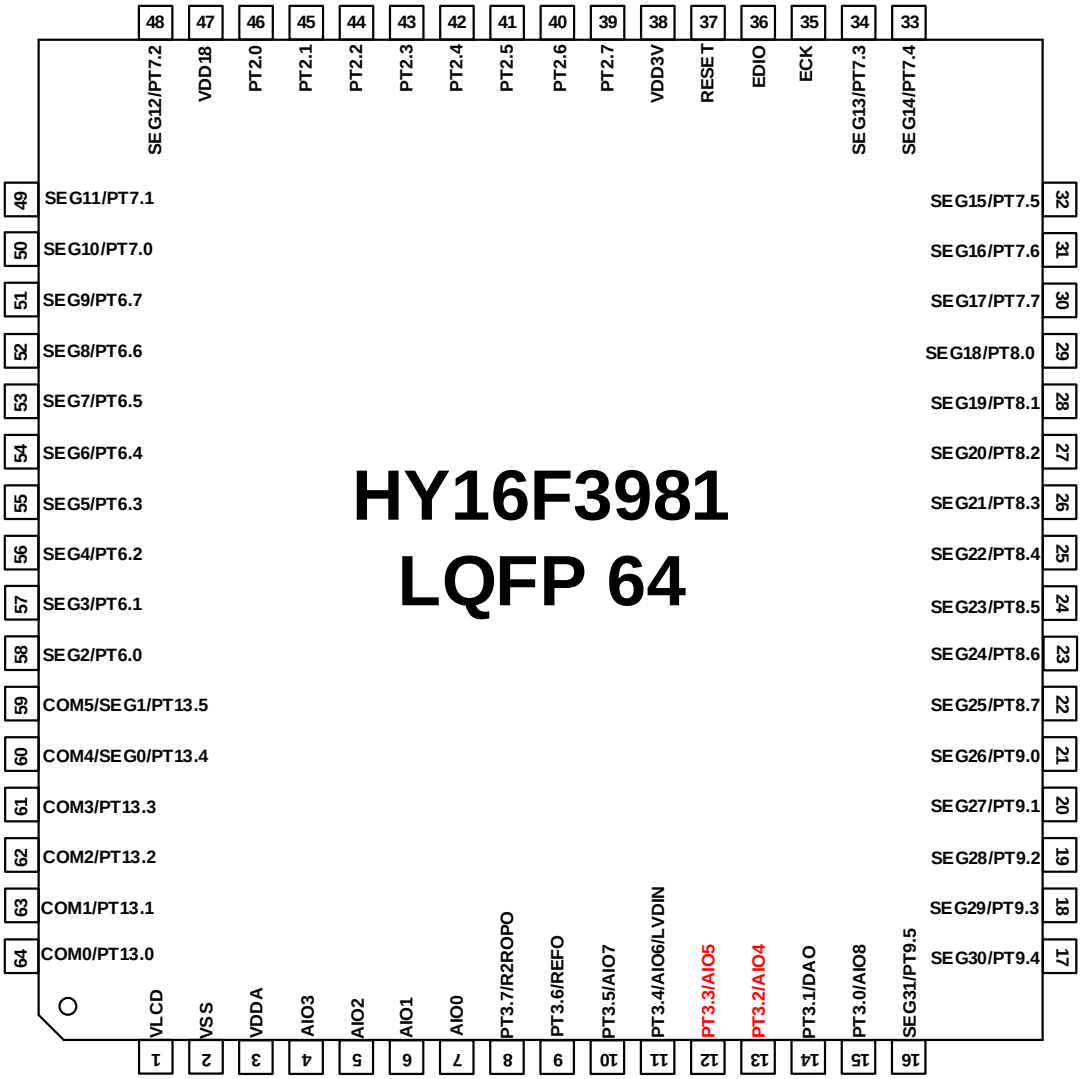


圖 2-1-1 HY16F3981 LQFP64 管腳圖

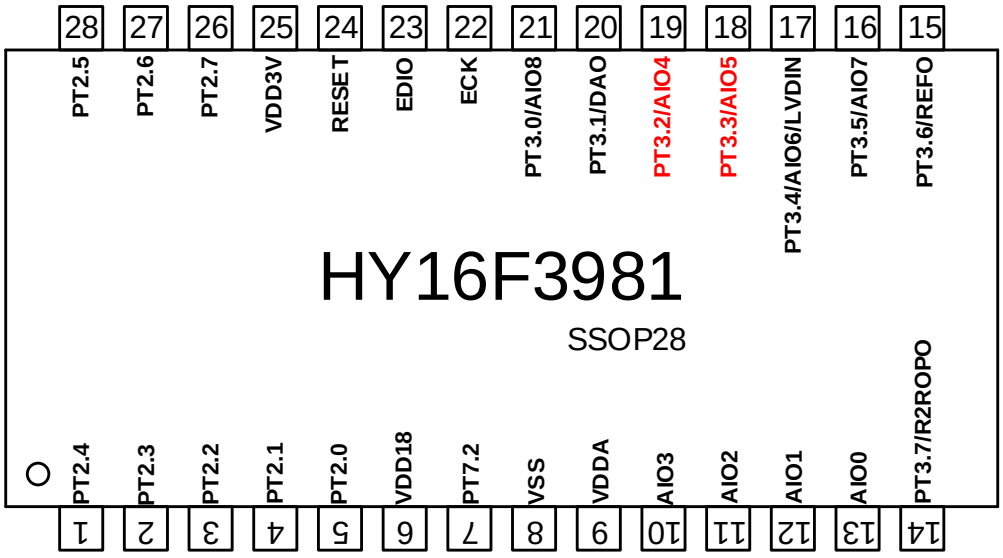


圖 2-1-2 HY16F3981 SSOP28 管腳圖

2.2 引腳功能描述

2.2.1 HY16F3981 引腳定義

類型定義：I = 數位輸入;O = 數位輸出;OD = 開漏輸出;AI = 類比輸入;AO = 類比輸出;P = 電源連接端.

引腳	HY16F3981-L064	HY16F3981-E028	類型	名稱	描述
VLCD	1	-	PIO	VLCD	LCD 穩壓電源輸出/LCD 電源輸入, 10uF Cap to VSS.
VSS	2	8	PI	VSS	接地端引腳
VDDA	3	9	PIO	VDDA	類比電源電壓/LDO 穩壓輸出端/類比電源電壓輸入端 1uF~10uF Cap to VSS.
AIO3	4	10	AI	AIO3	ADC 類比輸入引腳 AIO3
AIO2	5	11	AI	AIO2	ADC 類比輸入引腳 AIO2
AIO1	6	12	AI	AIO1	ADC 類比輸入引腳 AIO1
AIO0	7	13	AI	AIO0	ADC 類比輸入引腳 AIO0
PT3.7	8	14	IO AO I	PT3.7 R2ROPO INT3.7	通用數位輸入/輸出引腳 Rail-to-rail 運算放大器類比輸出引腳 R2ROPO 外部中斷源 INT3.7 輸入引腳
PT3.6	9	15	IO PIO I	PT3.6 REFO INT3.6	通用數位輸入/輸出引腳 類比參考電壓 1.2V 輸出引腳, 0.1uF Cap to VSS. 外部中斷源 INT3.6 輸入引腳
PT3.5	10	16	IO AI I	PT3.5 AIO7 INT3.5	通用數位輸入/輸出引腳 ADC 類比輸入引腳 AIO7 外部中斷源 INT3.5 輸入引腳
PT3.4	11	17	IO AI I AI	PT3.4 AIO6 INT3.4 LVDIN	通用數位輸入/輸出引腳 ADC 類比輸入引腳 AIO6 外部中斷源 INT3.4 輸入引腳 低電壓比較器外部輸入引腳 LVDIN
PT3.3	12	18	IO AI I	PT3.3 AIO5 INT3.3	通用數位輸入/輸出引腳 ADC 類比輸入引腳 AIO5 外部中斷源 INT3.3 輸入引腳
PT3.2	13	19	IO AI I	PT3.2 AIO4 INT3.2	通用數位輸入/輸出引腳 ADC 類比輸入引腳 AIO4 外部中斷源 INT3.2 輸入引腳
PT3.1	14	20	IO DO AO I	PT3.1 OPO2 DAO INT3.1	通用數位輸入/輸出引腳 運算放大器數位輸出引腳 OPO2 12-BIT Resistance Ladders 輸出引腳 外部中斷源 INT3.1 輸入引腳

引腳	HY16F3981-L064	HY16F3981-E028	類型	名稱	描述
PT3.0	15	21	IO	PT3.0	通用數位輸入/輸出引腳
			DO	OPO1	運算放大器數位輸出引腳 OPO1
			AI	AIO8	類比輸入引腳 AIO8
			I	INT3.0	外部中斷源 INT3.0 輸入引腳
SEG31	16	-	IO	PT9.5	通用數位輸入/輸出引腳
			AO	SEG31	LCD Segment 輸出
			O	PWM1_8	TimerB, PWM1_8 輸出引腳
			I	RX_8	EUART 通訊接收線引腳 RX_8
SEG30	17	-	IO	PT9.4	通用數位輸入/輸出引腳
			AO	SEG30	LCD Segment 輸出
			O	PWM0_8	TimerB, PWM0_8 輸出引腳
			O	TX_8	EUART 通訊發送線引腳 TX_8
SEG29	18	-	IO	PT9.3	通用數位輸入/輸出引腳
			AO	SEG29	LCD Segment 輸出
			O	PWM3_7	TimerB2, PWM3_7 輸出引腳
			O	MOSI_7	SPI 通訊數據線引腳 MOSI_7(主機輸出，從機輸入)
			I	RX2_7	EUART2 通訊接收線引腳 RX2_7
SEG28	19	-	IO	PT9.2	通用數位輸入/輸出引腳
			AO	SEG28	LCD Segment 輸出
			O	PWM2_7	TimerB2, PWM2_7 輸出引腳
			O	MISO_7	SPI 通訊數據線引腳 MISO_7(主機輸入，從機輸出)
			O	TX2_7	EUART2 通訊發送線引腳 TX2_7
SEG27	20	-	IO	PT9.1	通用數位輸入/輸出引腳
			AO	SEG27	LCD Segment 輸出
			O	PWM1_7	TimerB, PWM1_7 輸出引腳
			O	CK_7	SPI 通訊時鐘線引腳 CK_7
			I	RX_7	EUART 通訊接收線引腳 RX_7
SEG26	21	-	IO	PT9.0	通用數位輸入/輸出引腳
			AO	SEG26	LCD Segment 輸出
			O	PWM0_7	TimerB, PWM0_7 輸出引腳
			O	CS_7	SPI 通訊使能線引腳 CS_7
			O	TX_7	EUART 通訊發送線引腳 TX_7

引腳	HY16F3981-L064	HY16F3981-E028	類型	名稱	描述
SEG25	22	-	IO	PT8.7	通用數位輸入/輸出引腳
			AO	SEG25	LCD Segment 輸出
			O	PWM3_6	TimerB2, PWM3_6 輸出引腳
			O	MOSI_6	SPI 通訊數據線引腳 MOSI_6(主機輸出，從機輸入)
			I	RX2_6	EUART2 通訊接收線引腳 RX2_6
			I	TCI3_8	TimerB2 輸入源引腳 TCI3_8
SEG24	23	-	IO	PT8.6	通用數位輸入/輸出引腳
			AO	SEG24	LCD Segment 輸出
			O	PWM2_6	TimerB2, PWM2_6 輸出引腳
			O	MISO_6	SPI 通訊數據線引腳 MISO_6(主機輸入，從機輸出)
			O	TX2_6	EUART2 通訊發送線引腳 TX2_6
SEG23	24	-	IO	PT8.5	通用數位輸入/輸出引腳
			AO	SEG23	LCD Segment 輸出
			O	PWM1_6	TimerB, PWM1_6 輸出引腳
			O	CK_6	SPI 通訊時鐘線引腳 CK_6
			I	RX_6	EUART 通訊接收線引腳 RX_6
			I	TCI3_7	TimerB2 輸入源引腳 TCI3_7
SEG22	25	-	IO	PT8.4	通用數位輸入/輸出引腳
			AO	SEG22	LCD Segment 輸出
			O	PWM0_6	TimerB, PWM0_6 輸出引腳
			O	CS_6	SPI 通訊使能線引腳 CS_6
			O	TX_6	EUART 通訊發送線引腳 TX_6
SEG21	26	-	IO	PT8.3	通用數位輸入/輸出引腳
			AO	SEG21	LCD Segment 輸出
			O	PWM3_5	TimerB2, PWM3_5 輸出引腳
			O	MOSI_5	SPI 通訊數據線引腳 MOSI_5(主機輸出，從機輸入)
			I	RX2_5	EUART2 通訊接收線引腳 RX2_5
			I	TCI3_6	TimerB2 輸入源引腳 TCI3_6
SEG20	27	-	IO	PT8.2	通用數位輸入/輸出引腳
			AO	SEG20	LCD Segment 輸出
			O	PWM2_5	TimerB2, PWM2_5 輸出引腳
			O	MISO_5	SPI 通訊數據線引腳 MISO_5(主機輸入，從機輸出)
			O	TX2_5	EUART2 通訊發送線引腳 TX2_5

引腳	HY16F3981-L064	HY16F3981-E028	類型	名稱	描述
SEG19	28		IO	PT8.1	通用數位輸入/輸出引腳
			AO	SEG19	LCD Segment 輸出
			O	PWM1_5	TimerB, PWM1_5 輸出引腳
			O	CK_5	SPI 通訊時鐘線引腳 CK_5
			I	RX_5	EUART 通訊接收線引腳 RX_5
			I	TCI3_5	TimerB2 輸入源引腳 TCI3_5
SEG18	29		IO	PT8.0	通用數位輸入/輸出引腳
			AO	SEG18	LCD Segment 輸出
			O	PWM0_5	TimerB, PWM0_5 輸出引腳
			O	CS_5	SPI 通訊使能線引腳 CS_5
			O	TX_5	EUART 通訊發送線引腳 TX_5
SEG17	30		IO	PT7.7	通用數位輸入/輸出引腳
			AO	SEG17	LCD Segment 輸出
			I	TCI3_4	TimerB2 輸入源引腳 TCI3_4
SEG16	31		IO	PT7.6	通用數位輸入/輸出引腳
			AO	SEG16	LCD Segment 輸出
SEG15	32		IO	PT7.5	通用數位輸入/輸出引腳
			AO	SEG15	LCD Segment 輸出
			I	TCI3_3	TimerB2 輸入源引腳 TCI3_3
SEG14	33		IO	PT7.4	通用數位輸入/輸出引腳
			AO	SEG14	LCD Segment 輸出
SEG13	34		IO	PT7.3	通用數位輸入/輸出引腳
			AO	SEG13	LCD Segment 輸出
			I	TCI3_2	TimerB2 輸入源引腳 TCI3_2
ECK	35	22	DIO	ECK	開發調試通訊口(EDM)時鐘線引腳, 100K Resistance to VSS.
EDIO	36	23	DIO	EDIO	開發調試通訊口(EDM)數據線輸入/輸出引腳, 100K Resistance to VSS.
RESET	37	24	DI	RESET	復位引腳(低電位有效), 100K Resistance to VDD3V, 100nF Cap to VSS.
VDD3V	38	25	PI	VDD3V	晶片工作電源電壓輸入引腳, 10uF Cap to VSS.

引腳	HY16F3981-L064	HY16F3981-E028	類型	名稱	描述
PT2.7	39	26	IO	PT2.7	通用數位輸入/輸出引腳
			XO	HS_XOUT	外部高速晶震 2~16MHZ 輸出引腳
			I	INT2.7	外部中斷源 INT2.7 輸入引腳
			O	PWM3_4	TimerB2, PWM3_4 輸出引腳
			O	MOSI_4	SPI 通訊數據線引腳 MOSI_4(主機輸出，從機輸入)
			I	RX2_4	EUART2 通訊接收線引腳 RX2_4
			I	TCI2_8	捕捉比較器輸入源引腳 TCI2_8
			IO	SDA_8	I2C 通訊數據線引腳 SDA_8
PT2.6	40	27	IO	PT2.6	通用數位輸入/輸出引腳
			XI	HS_XIN	外部高速晶震 2~16MHZ 輸入引腳
			I	INT2.6	外部中斷源 INT2.6 輸入引腳
			O	PWM2_4	TimerB2, PWM2_4 輸出引腳
			I	MISO_4	SPI 通訊數據線引腳 MISO_4(主機輸入，從機輸出)
			O	TX2_4	EUART2 通訊發送線引腳 TX2_4
			I	TCI1_8	捕捉比較器輸入源引腳 TCI1_8
			IO	SCL_8	I2C 通訊時鐘線引腳 SCL_8
PT2.5	41	28	IO	PT2.5	通用數位輸入/輸出引腳
			XI	LS_XIN	外部低速晶震 32768HZ 輸入引腳
			I	INT2.5	外部中斷源 INT2.5 輸入引腳
			O	PWM1_4	TimerB, PWM1_4 輸出引腳
			I	CK_4	SPI 通訊時鐘線引腳 CK_4
			I	RX_4	EUART 通訊接收線引腳 RX_4
			I	TCI2_7	捕捉比較器輸入源引腳 TCI2_7
			IO	SDA_7	I2C 通訊數據線引腳 SDA_7
PT2.4	42	1	IO	PT2.4	通用數位輸入/輸出引腳
			XO	LS_XOUT	外部低速晶震 32768HZ 輸出引腳
			I	INT2.4	外部中斷源 INT2.4 輸入引腳
			O	PWM0_4	TimerB, PWM0_4 輸出引腳
			I	CS_4	SPI 通訊使能引腳 CS_4
			O	TX_4	EUART 通訊發送線引腳 TX_4
			I	TCI1_7	捕捉比較器輸入源引腳 TCI1_7
			IO	SCL_7	I2C 通訊時鐘線引腳 SCL_7

引腳	HY16F3981-L064	HY16F3981-E028	類型	名稱	描述
PT2.3	43	2	IO	PT2.3	通用數位輸入/輸出引腳
			I	INT2.3	外部中斷源 INT2.3 輸入引腳
			O	PWM3_3	TimerB2, PWM3_3 輸出引腳
			O	MOSI_3	SPI 通訊數據線引腳 MOSI_3(主機輸出，從機輸入)
			I	RX2_3	EUART2 通訊接收線引腳 RX2_3
			I	TCI2_6	捕捉比較器輸入源引腳 TCI2_6
			IO	SDA_6	I2C 通訊數據線引腳 SDA_6
PT2.2	44	3	IO	PT2.2	通用數位輸入/輸出引腳
			I	INT2.2	外部中斷源 INT2.2 輸入引腳
			O	PWM2_3	TimerB2, PWM2_3 輸出引腳
			I	MISO_3	SPI 通訊數據線引腳 MISO_3(主機輸入，從機輸出)
			O	TX2_3	EUART2 通訊發送線引腳 TX2_3
			I	TCI1_6	捕捉比較器輸入源引腳 TCI1_6
			IO	SCL_6	I2C 通訊時鐘線引腳 SCL_6
PT2.1	45	4	IO	PT2.1	通用數位輸入/輸出引腳
			I	INT2.1	外部中斷源 INT2.1 輸入引腳
			O	PWM1_3	TimerB, PWM1_3 輸出引腳
			I	CK_3	SPI 通訊時鐘線引腳 CK_3
			I	RX_3	EUART 通訊接收線引腳 RX_3
			I	TCI2_5	捕捉比較器輸入源引腳 TCI2_5
			IO	SDA_5	I2C 通訊數據線引腳 SDA_5
PT2.0	46	5	IO	PT2.0	通用數位輸入/輸出引腳
			I	INT2.0	外部中斷源 INT2.0 輸入引腳
			O	PWM0_3	TimerB, PWM0_3 輸出引腳
			I	CS_3	SPI 通訊使能引腳 CS_3
			O	TX_3	EUART 通訊發送線引腳 TX_3
			I	TCI1_5	捕捉比較器輸入源引腳 TCI1_5
			IO	SCL_5	I2C 通訊時鐘線引腳 SCL_5
VDD18	47	6	PI	VDD18	數位電源電壓引腳，輸出 1.8V, 1uF Cap to VSS
SEG12	48	7	IO	PT7.2	通用數位輸入/輸出引腳
			AO	SEG12	LCD Segment 輸出
SEG11	49	-	IO	PT7.1	通用數位輸入/輸出引腳
			AO	SEG11	LCD Segment 輸出
			I	TCI3_1	TimerB2 輸入源引腳 TCI3_1
SEG10	50	-	IO	PT7.0	通用數位輸入/輸出引腳
			AO	SEG10	LCD Segment 輸出

引腳	HY16F3981-L064	HY16F3981-E028	類型	名稱	描述
SEG9	51	-	IO	PT6.7	通用數位輸入/輸出引腳
			AO	SEG9	LCD Segment 輸出
SEG8	52	-	IO	PT6.6	通用數位輸入/輸出引腳
			AO	SEG8	LCD Segment 輸出
SEG7	53	-	IO	PT6.5	通用數位輸入/輸出引腳
			AO	SEG7	LCD Segment 輸出
SEG6	54	-	IO	PT6.4	通用數位輸入/輸出引腳
			AO	SEG6	LCD Segment 輸出
SEG5	55	-	IO	PT6.3	通用數位輸入/輸出引腳
			AO	SEG5	LCD Segment 輸出
SEG4	56	-	IO	PT6.2	通用數位輸入/輸出引腳
			AO	SEG4	LCD Segment 輸出
SEG3	57	-	IO	PT6.1	通用數位輸入/輸出引腳
			AO	SEG3	LCD Segment 輸出
SEG2	58	-	IO	PT6.0	通用數位輸入/輸出引腳
			AO	SEG2	LCD Segment 輸出
SEG1	59		IO	PT13.5	通用數位輸入/輸出引腳
			AO	SEG1	LCD Segment 輸出
			AO	COM5	LCD Common 輸出
SEG0	60		IO	PT13.4	通用數位輸入/輸出引腳
			AO	SEG0	LCD Segment 輸出
			AO	COM4	LCD Common 輸出
COM3	61		IO	PT13.3	通用數位輸入/輸出引腳
			AO	COM3	LCD Common 輸出
COM2	62		IO	PT13.2	通用數位輸入/輸出引腳
			AO	COM2	LCD Common 輸出
COM1	63		IO	PT13.1	通用數位輸入/輸出引腳
			AO	COM1	LCD Common 輸出
COM0	64		IO	PT13.0	通用數位輸入/輸出引腳
			AO	COM0	LCD Common 輸出

表2-1 HY16F3981 管腳定義及管腳功能描述

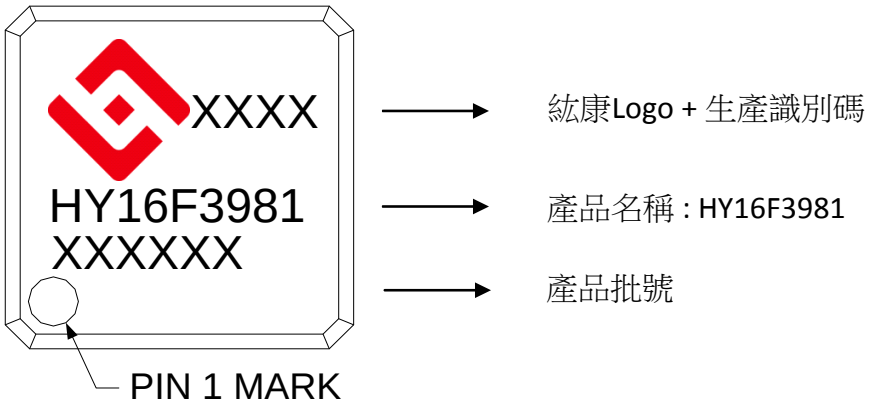
2.2.2 管腳複用功能及複用功能優先級

Function	INT	Timer C Capture	Special Function	SPI	I2C	UART 1/2	AIP	Analog	Timer B/B2 PWM
Output Priority	I/P	I/P	0	1	2	3	4	5	6
PT2.0	INT2.0	TCI1_5		CS_3	SCL_5	Tx_3			PWM0_3
PT2.1	INT2.1	TCI2_5		CK_3	SDA_5	Rx_3			PWM1_3
PT2.2	INT2.2	TCI1_6		MISO_3	SCL_6	Tx2_3			PWM2_3
PT2.3	INT2.3	TCI2_6		MOSI_3	SDA_6	Rx2_3			PWM3_3
PT2.4	INT2.4	TCI1_7	LS_XOUT	CS_4	SCL_7	Tx_4			PWM0_4
PT2.5	INT2.5	TCI2_7	LS_XIN	CK_4	SDA_7	Rx_4			PWM1_4
PT2.6	INT2.6	TCI1_8	HS_XIN	MISO_4	SCL_8	Tx2_4			PWM2_4
PT2.7	INT2.7	TCI2_8	HS_XOUT	MOSI_4	SDA_8	Rx2_4			PWM3_4
PT3.0	INT3.0						OPO1	AIO8	
PT3.1	INT3.1						OPO2	DAO	
PT3.2	INT3.2							AIO4	
PT3.3	INT3.3							AIO5	
PT3.4	INT3.4							AIO6/LVDIN	
PT3.5	INT3.5							AIO7	
PT3.6	INT3.6							REFO	
PT3.7	INT3.7							R2ROPO	
RESET	RESET								
AIO0								AIO0	
AIO1								AIO1	
AIO2								AIO2	
AIO3								AIO3	
PT13.0			COM 0						
PT13.1			COM 1						
PT13.2			COM 2						
PT13.3			COM 3						
PT13.4			COM 4/SEG 0						
PT13.5			COM 5/SEG 1						
PT6.0			SEG 2						
PT6.1			SEG 3						

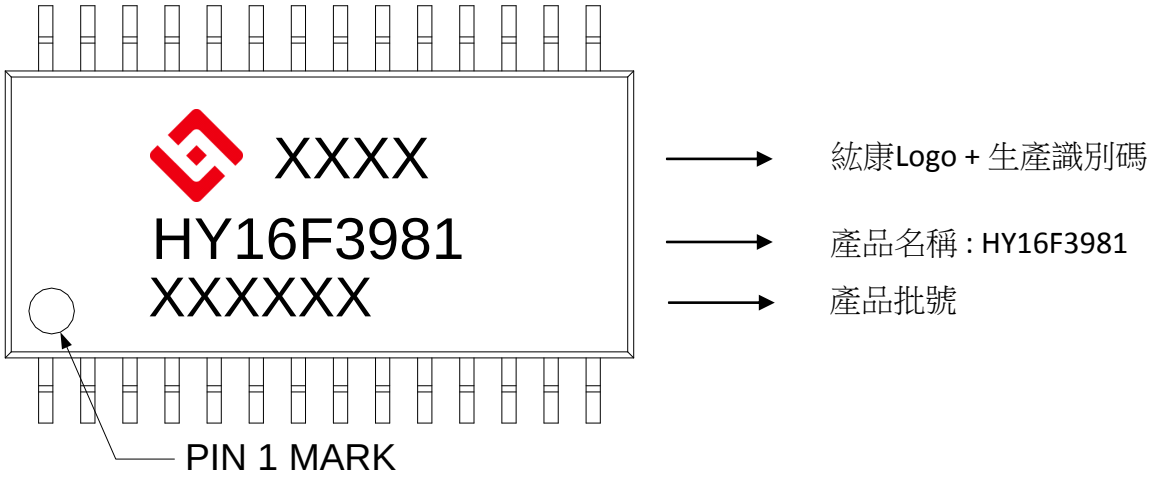
PT6.2			SEG 4						
PT6.3			SEG 5						
PT6.4			SEG 6						
PT6.5			SEG 7						
PT6.6			SEG 8						
PT6.7			SEG 9						
PT7.0			SEG 10						
PT7.1		TCI3_1	SEG 11						
PT7.2			SEG 12						
PT7.3		TCI3_2	SEG 13						
PT7.4			SEG 14						
PT7.5		TCI3_3	SEG 15						
PT7.6			SEG 16						
PT7.7		TCI3_4	SEG 17						
PT8.0			SEG 18	CS_5		Tx_5			PWM0_5
PT8.1		TCI3_5	SEG 19	CK_5		Rx_5			PWM1_5
PT8.2			SEG 20	MISO_5		Tx2_5			PWM2_5
PT8.3		TCI3_6	SEG 21	MOSI_5		Rx2_5			PWM3_5
PT8.4			SEG 22	CS_6		Tx_6			PWM0_6
PT8.5		TCI3_7	SEG 23	CK_6		Rx_6			PWM1_6
PT8.6			SEG 24	MISO_6		Tx2_6			PWM2_6
PT8.7		TCI3_8	SEG 25	MOSI_6		Rx2_6			PWM3_6
PT9.0			SEG 26	CS_7		Tx_7			PWM0_7
PT9.1			SEG 27	CK_7		Rx_7			PWM1_7
PT9.2			SEG 28	MISO_7		Tx2_7			PWM2_7
PT9.3			SEG 29	MOSI_7		Rx2_7			PWM3_7
PT9.4			SEG 30			Tx_8			PWM0_8
PT9.5			SEG 31			Rx_8			PWM1_8

2.3 封裝片標記信息

2.3.1 LQFP 封裝片標記信息



2.3.2 SSOP28 封裝片標記信息



3. 應用電路

3.1 紅外線感測應用電路(LQFP64 支援 LCD)

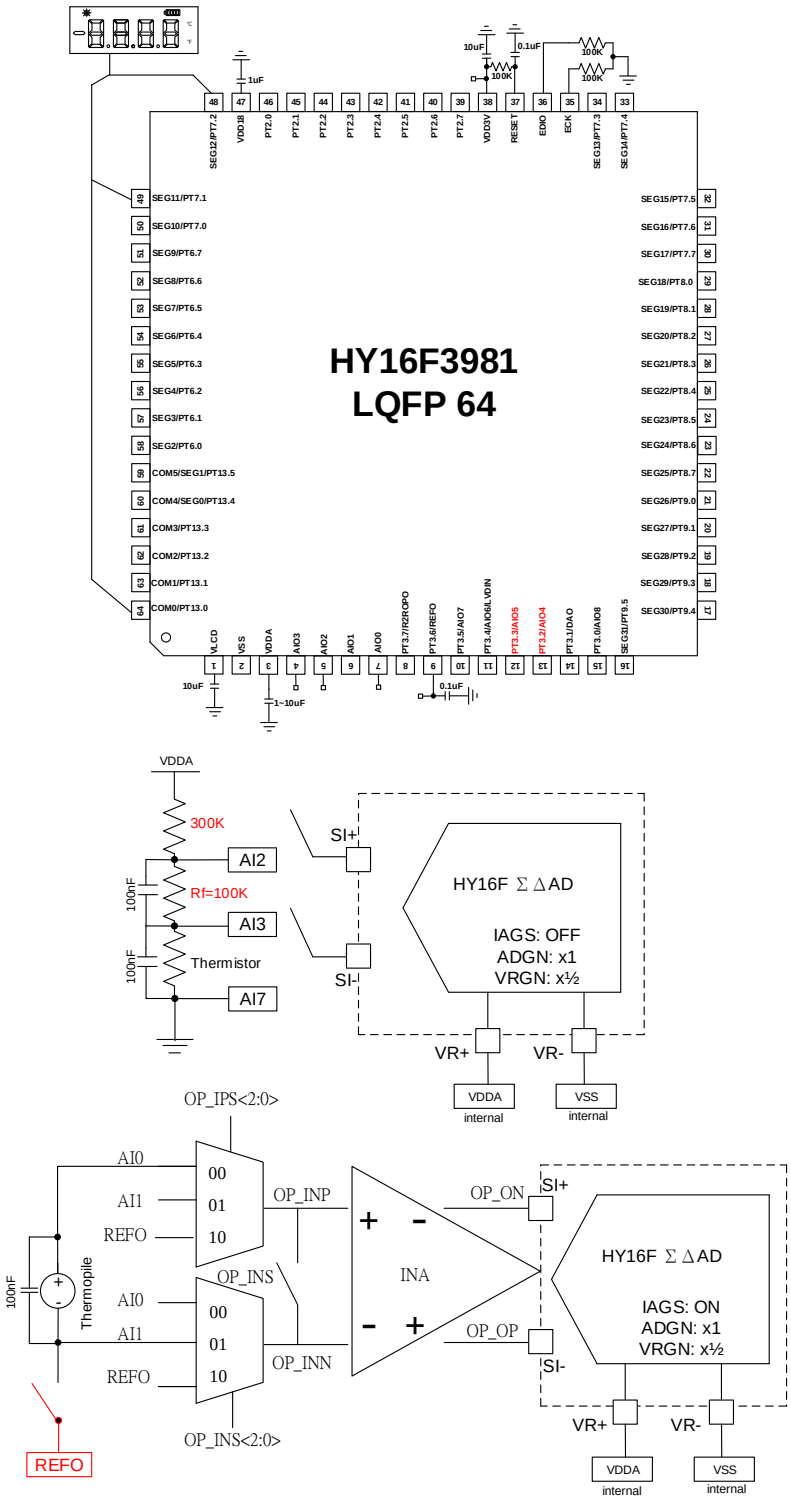


圖3-1 紅外線感測應用電路(LQFP64支援LCD)

3.2 紅外線感測應用電路(SSOP28 無支援 LCD)

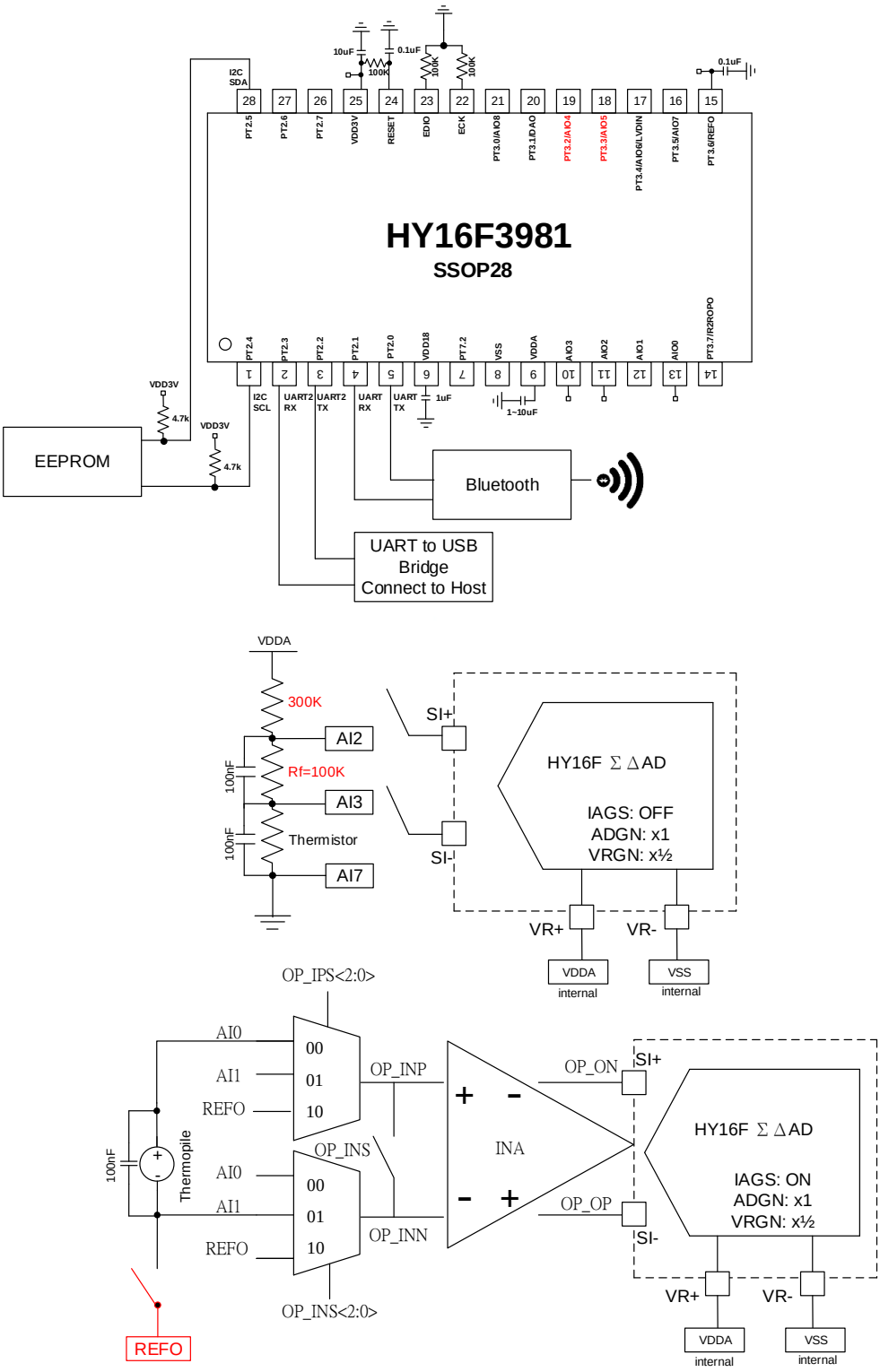


圖3-2 紅外線感測應用電路(SSOP28無支援LCD)

3.3 血壓計傳感器應用電路(LQFP64 支援 LCD)

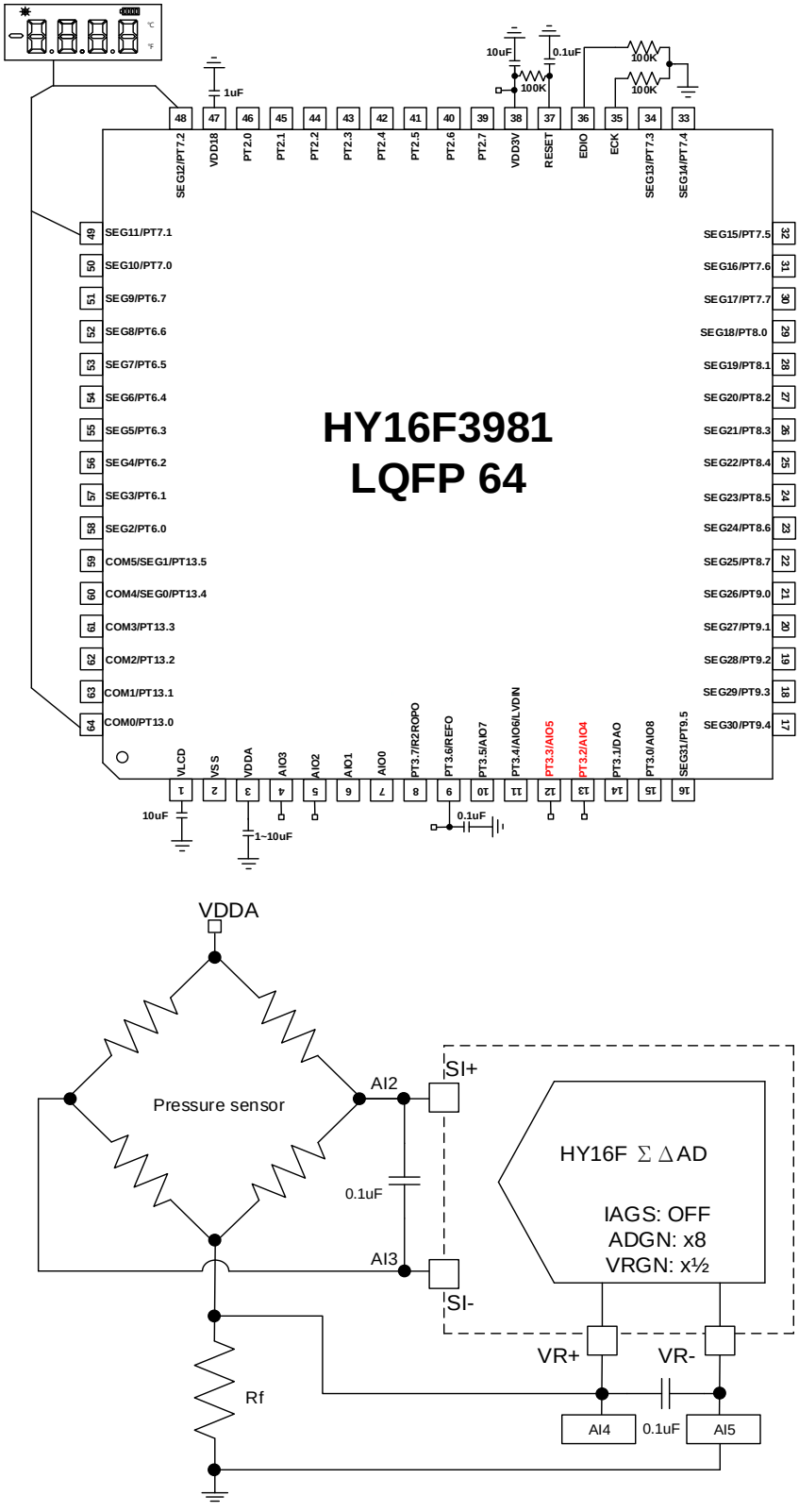


圖 3-3 血壓計傳感器應用電路(LQFP64支援LCD)

3.4 血壓計傳感器應用電路(SSOP28 無支援 LCD)

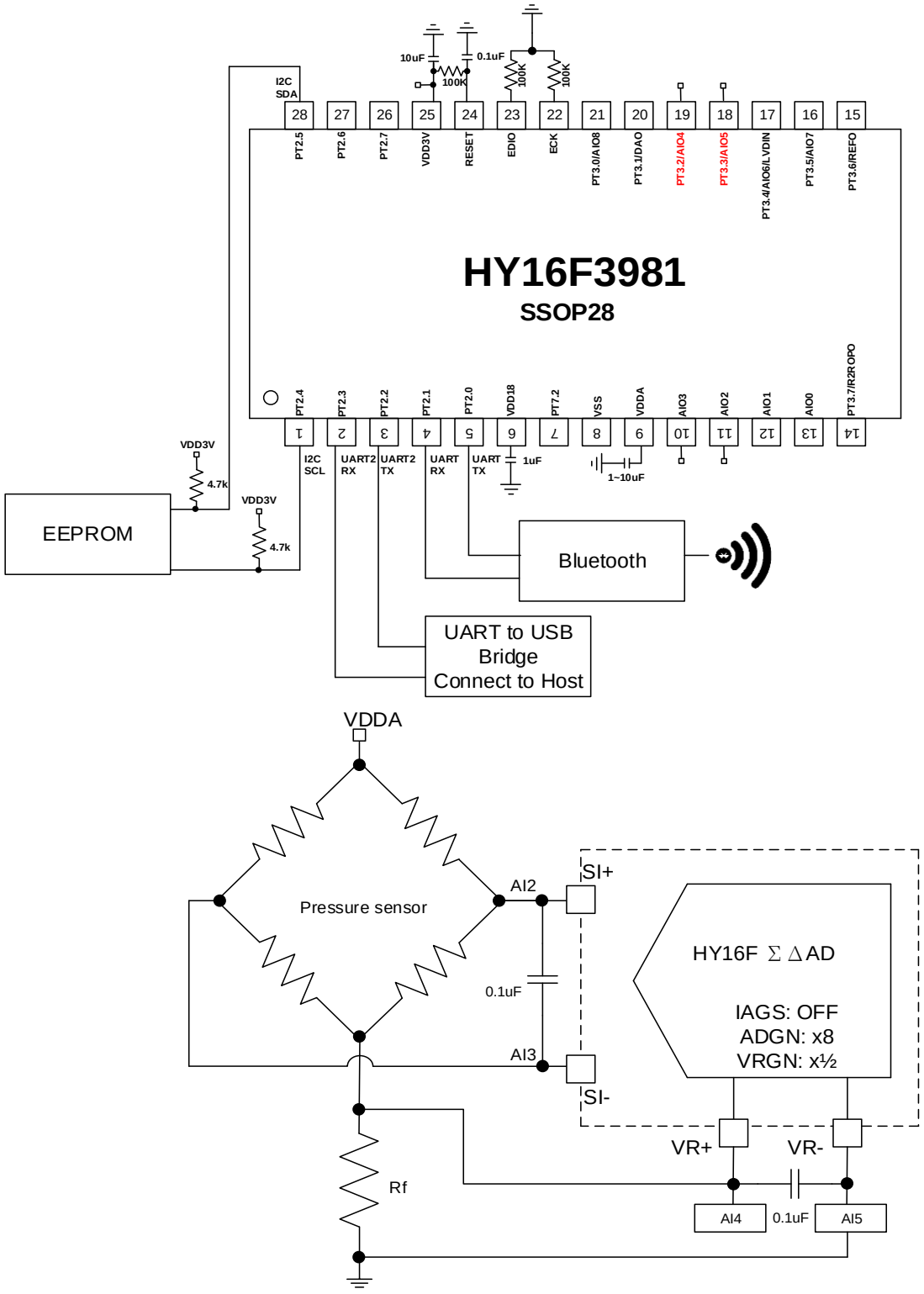


圖 3-4 血壓計傳感器應用電路(SSOP28無支援LCD)

4. 功能概述

4.1 內部框圖

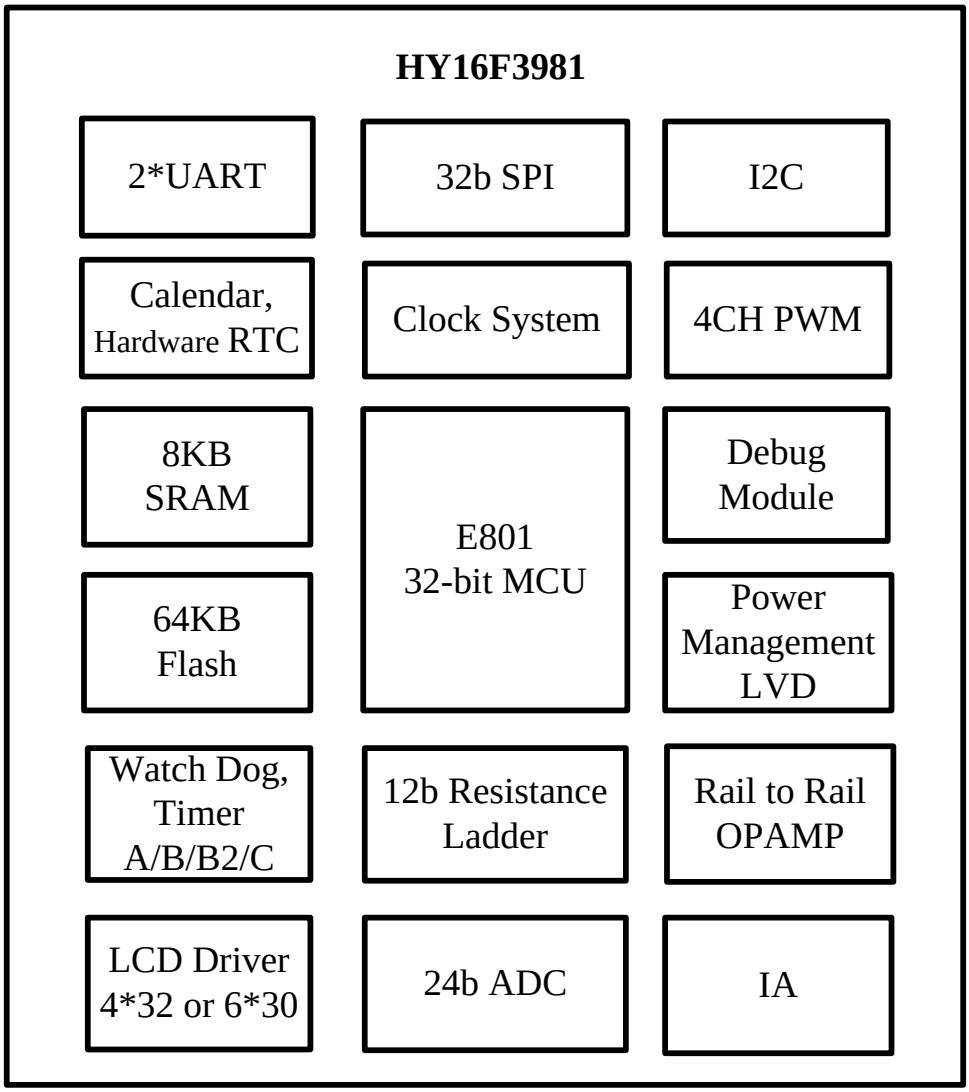


圖 4-1 HY16F3981 內部框圖

4.2 中央處理器核心方框圖

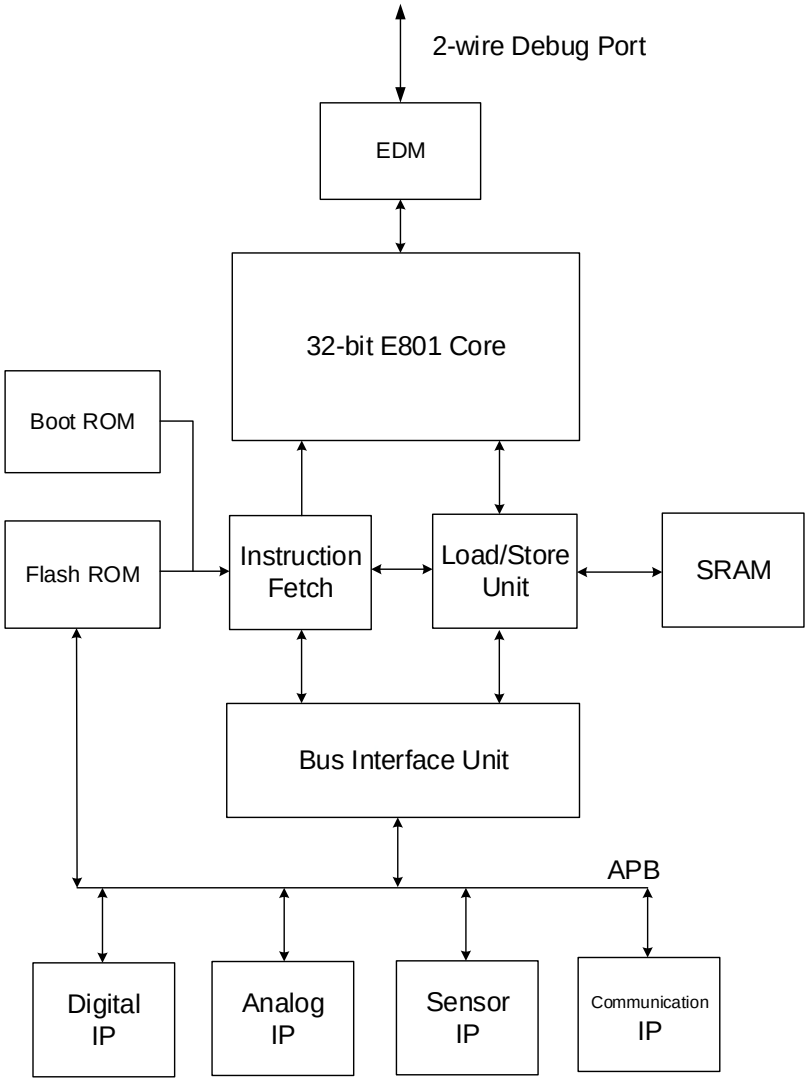
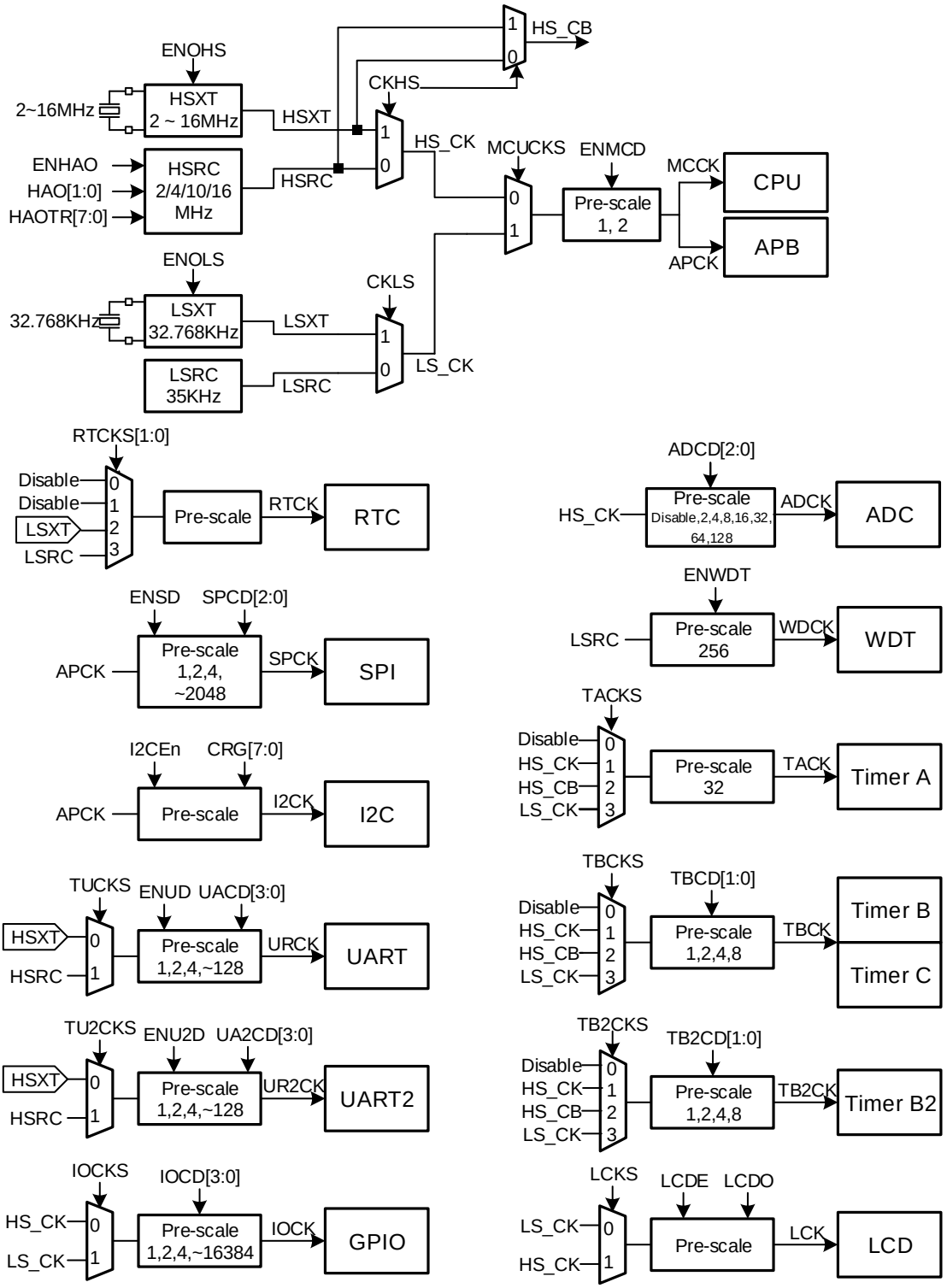


Figure 4-2 中央處理器核心方框圖

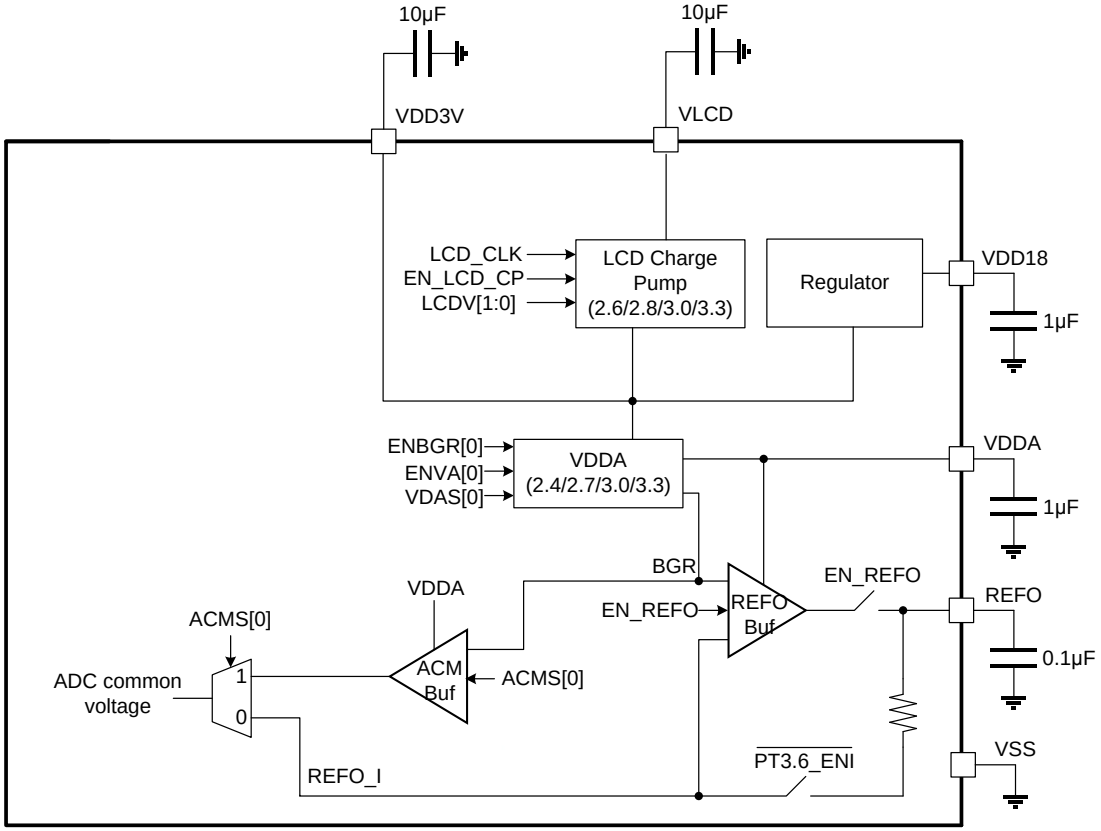
4.3 相關的支援文檔

檔案名稱	描述
UG-HY16F3981	HY16F3981 系列用戶手冊
APD-HY16IDE022	HY16F3981 C 函數庫手冊
APD-HY16IDE023	HY16F3981 各 IP 使用說明書
APD-HY16IDE001	HY16F 系列 IDE 軟體使用說明書/ HY16F Series Device 安裝程式
APD-HY16IDE009	HY16F 系列 ICE 硬體使用說明書
APD-HY16IDE006	HY16F 系列燒錄器使用說明書

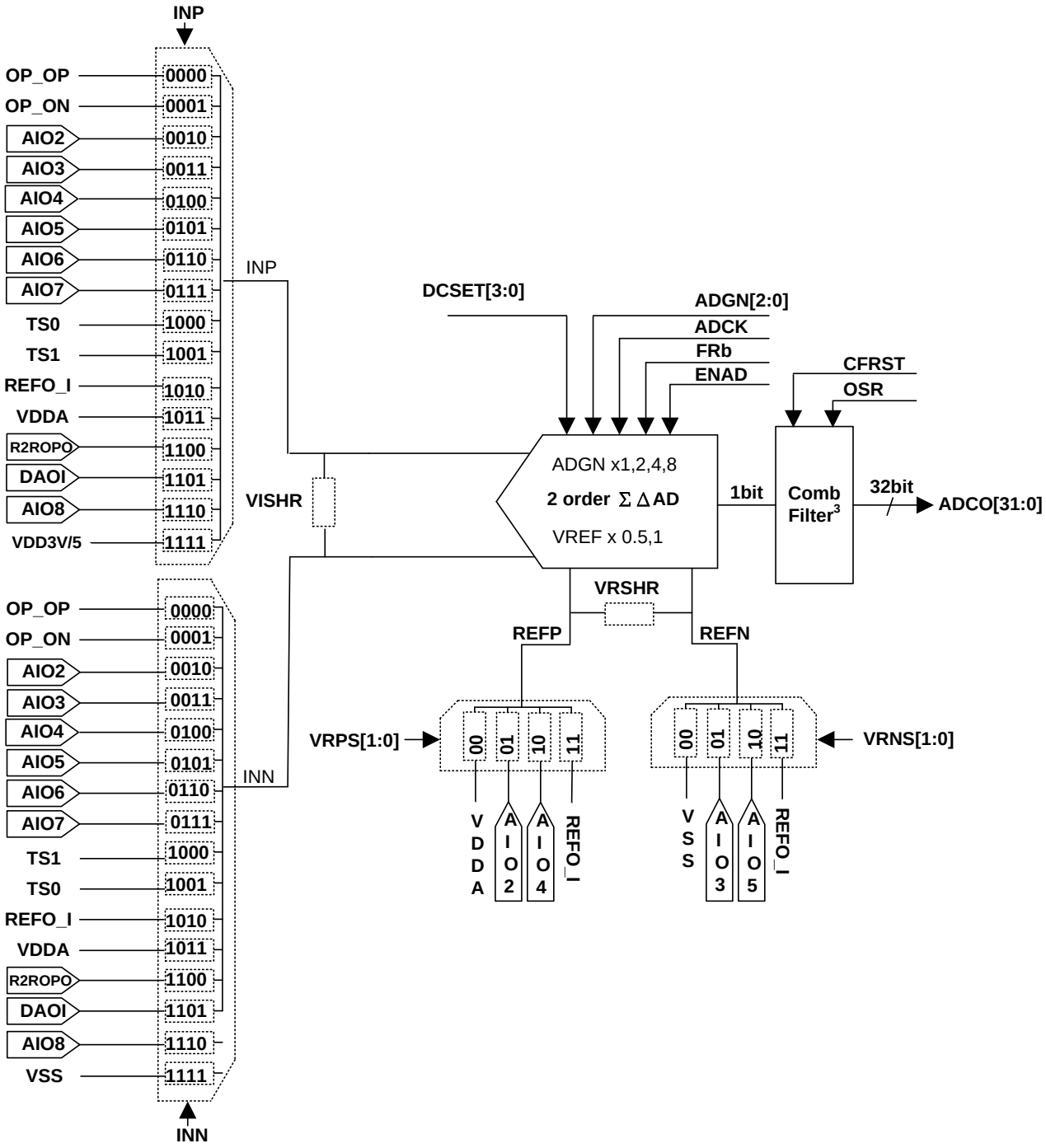
4.4 時鐘系統網絡


ENOHS
2~16MHz
HSXT
2 ~ 16MHz
HSXT
CKHS
HS_CB
ENHAO
HAO[1:0]
HAOTR[7:0]
HSRC
2/4/10/16
MHz
HSRC
HS_CK
MCUCKS
ENMCD
Pre-scale
1, 2
MCCK
CPU
APB
APCK
ENOLS
32.768KHz
LSXT
32.768KHz
LSXT
CKLS
LS_CK
LSRC
35KHz
LSRC
RTCKS[1:0]
Disable
Disable
LSXT
LSRC
Pre-scale
RTCK
RTC
ADCD[2:0]
HS_CK
Pre-scale
Disable,2,4,8,16,32,
64,128
ADCK
ADC
ENWDT
LSRC
Pre-scale
256
WDCK
WDT
ENSD
SPCD[2:0]
APCK
Pre-scale
1,2,4,
~2048
SPCK
SPI
TACKS
Disable
HS_CK
HS_CB
LS_CK
Pre-scale
32
TACK
Timer A
I2CEn
CRG[7:0]
APCK
Pre-scale
I2CK
I2C
TBCKS
TBCD[1:0]
Disable
HS_CK
HS_CB
LS_CK
Pre-scale
1,2,4,8
TBCK
Timer B
Timer C
TUCKS
ENUD
UACD[3:0]
HSXT
HSRC
Pre-scale
1,2,4,~128
URCK
UART
TB2CKS
TB2CD[1:0]
Disable
HS_CK
HS_CB
LS_CK
Pre-scale
1,2,4,8
TB2CK
Timer B2
TU2CKS
ENU2D
UA2CD[3:0]
HSXT
HSRC
Pre-scale
1,2,4,~128
UR2CK
UART2
IOCKS
IOCD[3:0]
HS_CK
LS_CK
Pre-scale
1,2,4,~16384
IOCK
GPIO
LCKS
LCDE
LCDO
LS_CK
HS_CK
Pre-scale
LCK
LCD

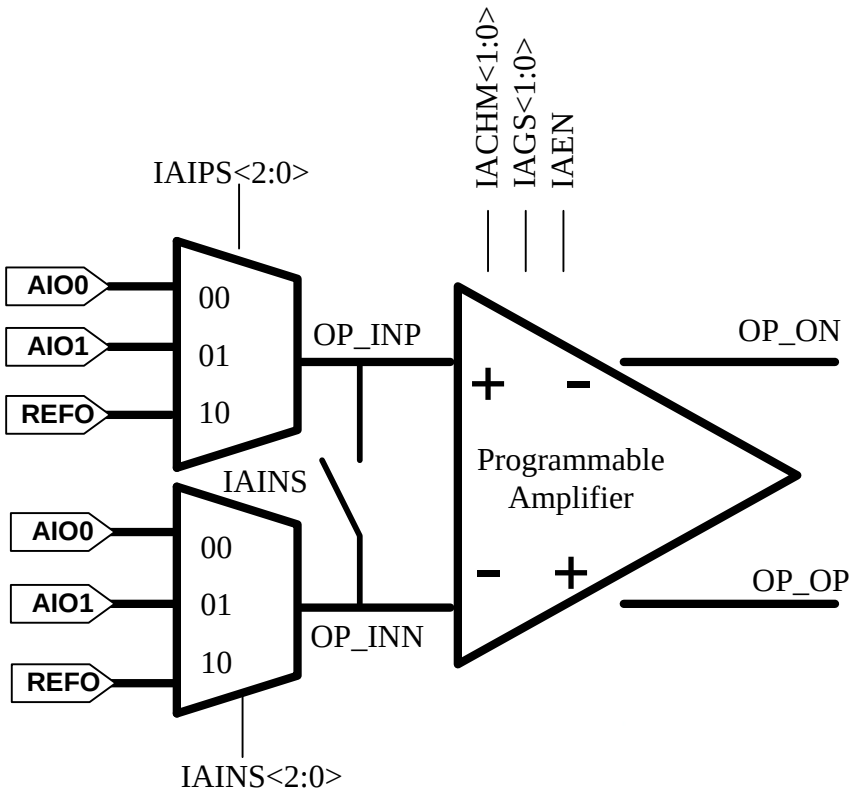
4.5 電源系統網絡


10μF
10μF
VDD3V
VLCD
LCD_CLK
EN_LCD_CP
LCDV[1:0]
LCD Charge Pump (2.6/2.8/3.0/3.3)
Regulator
VDD18
1μF
ENBGR[0]
ENVA[0]
VDAS[0]
VDDA (2.4/2.7/3.0/3.3)
VDDA
1μF
BGR
EN_REFO
REFO Buf
REFO
0.1μF
VDDA
ACMS[0]
ADC common voltage
1
0
ACM Buf
ACMS[0]
PT3.6_ENI
VSS
REFO_I

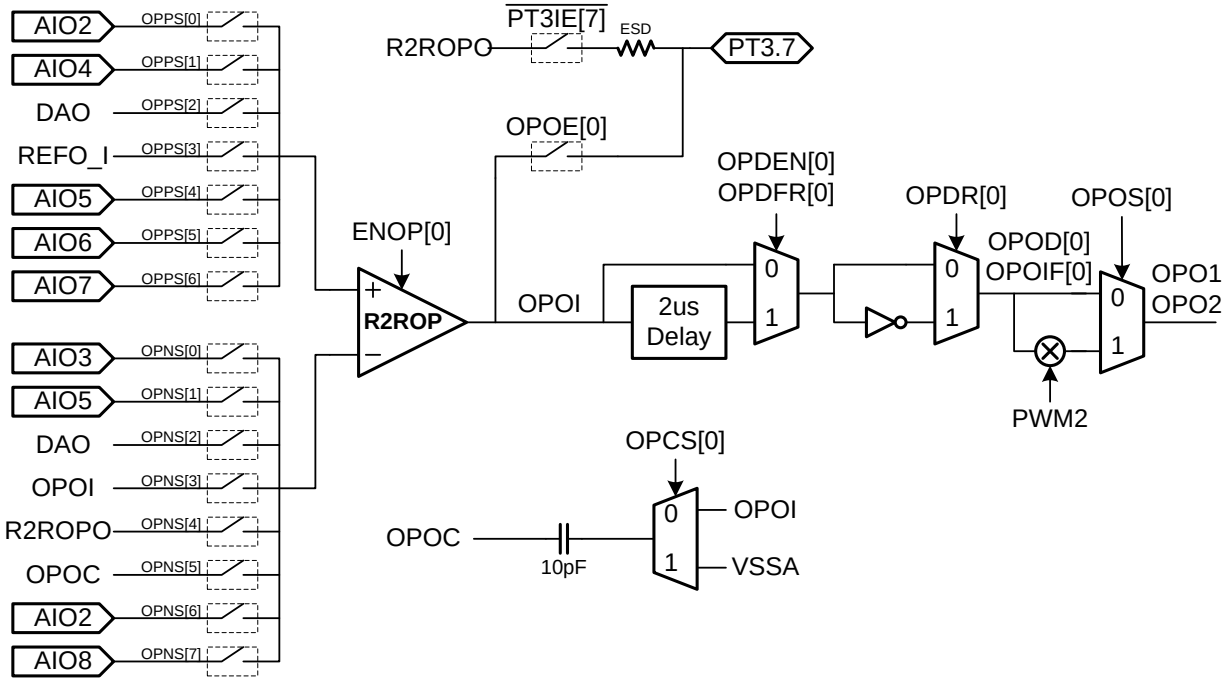
4.6 24-bit ΣΔADC 網路



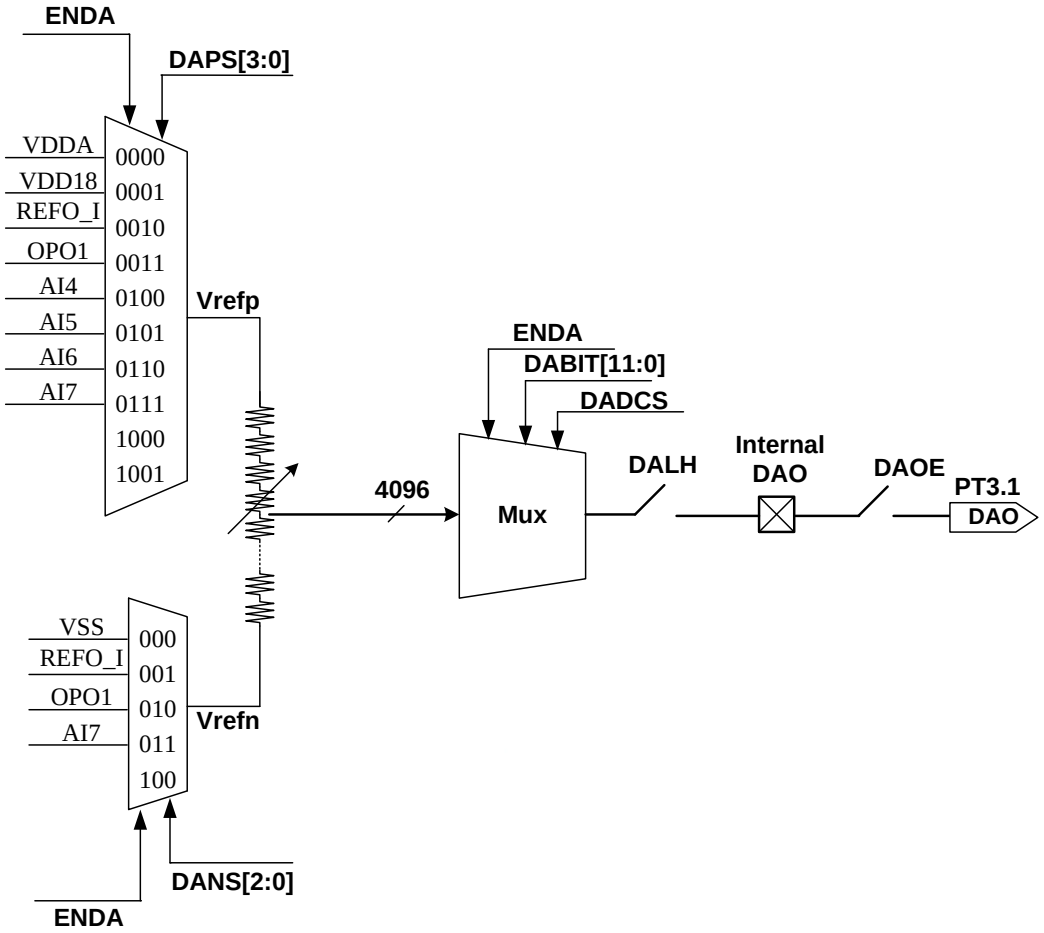
4.7 儀表放大器 IA 網路



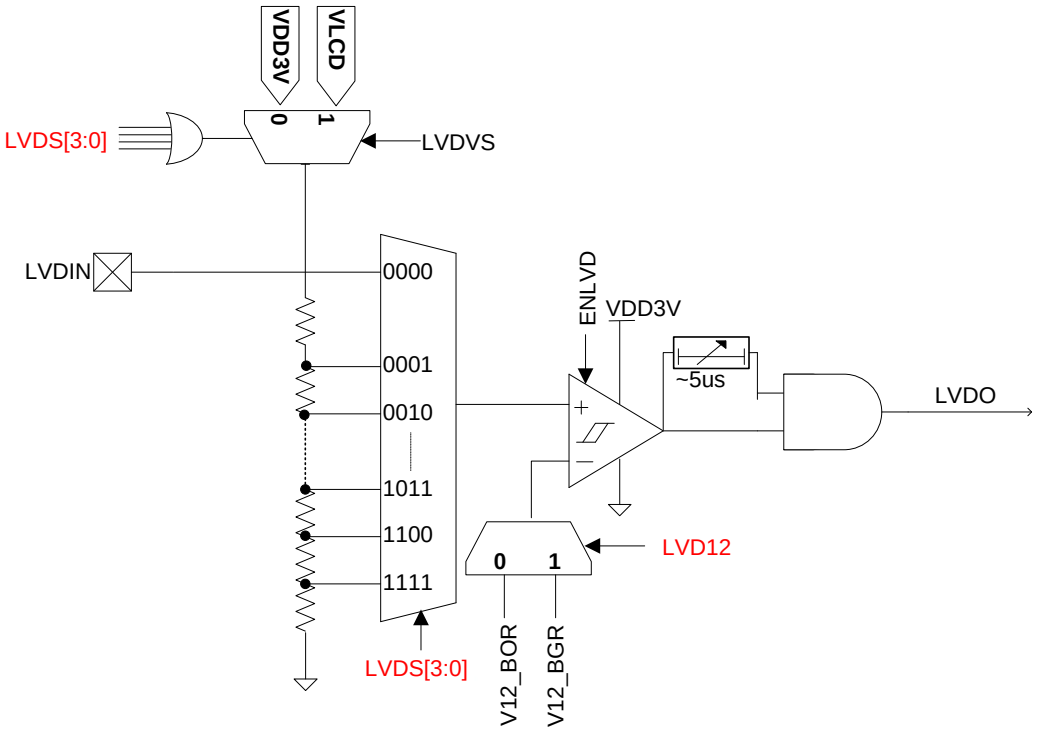
4.8 軌對軌運算放大器 OPAMP 網路



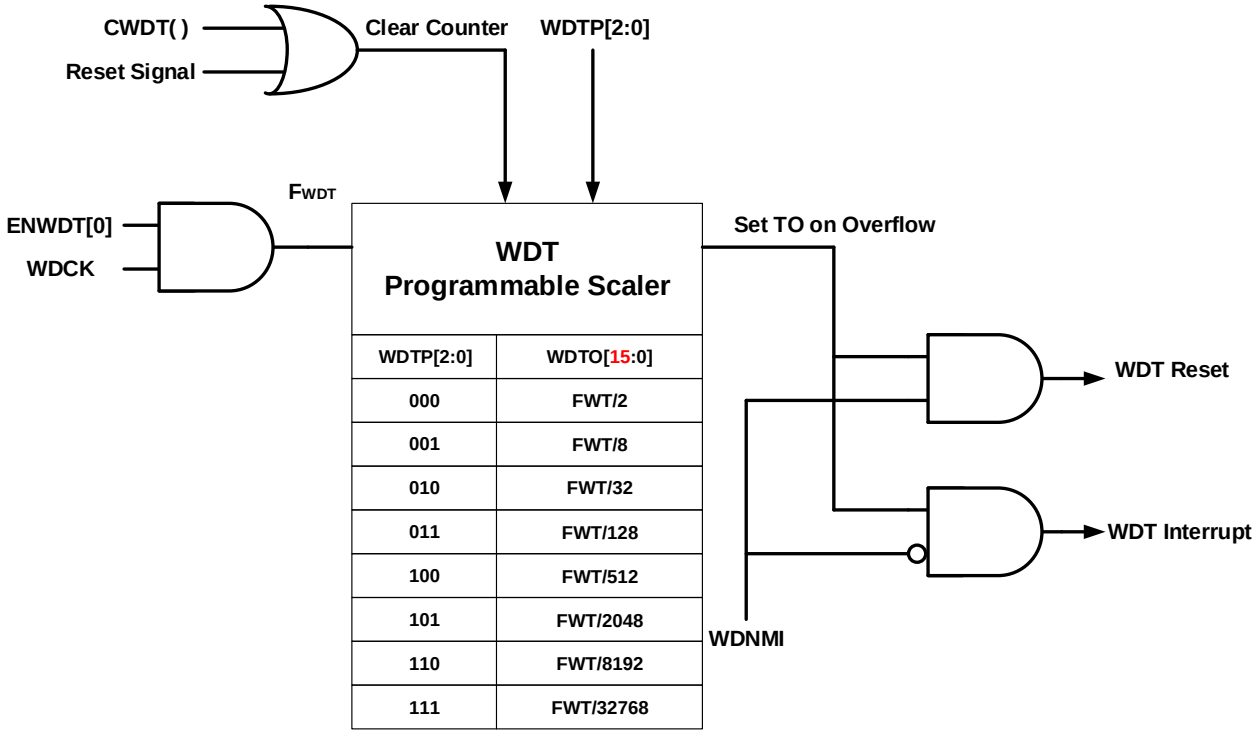
4.9 12-bit Resistance Ladder 網路



4.10 低電壓比較器網路

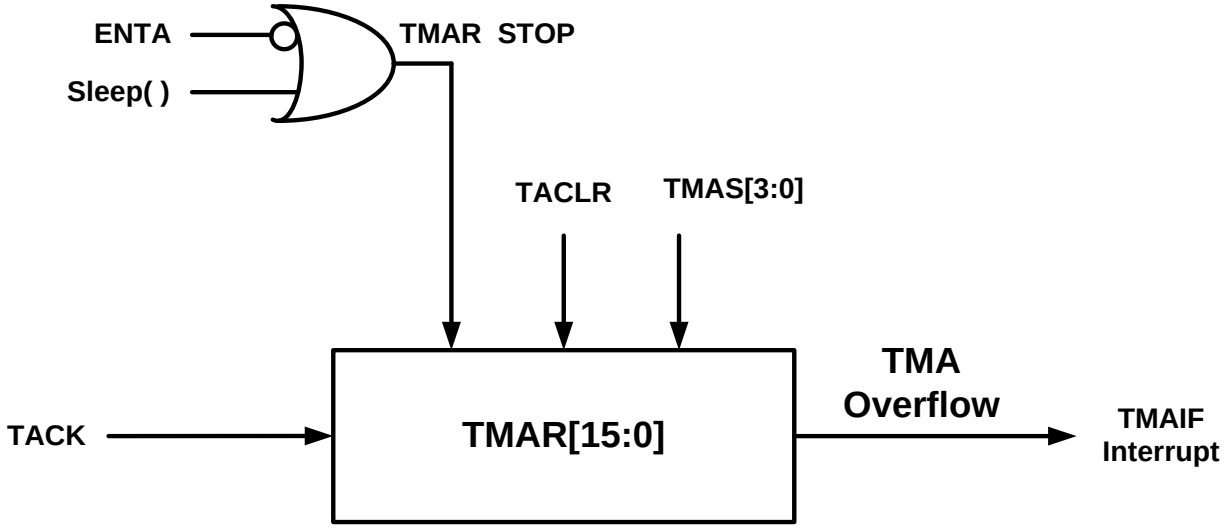


4.11 看門狗(WDT)網路



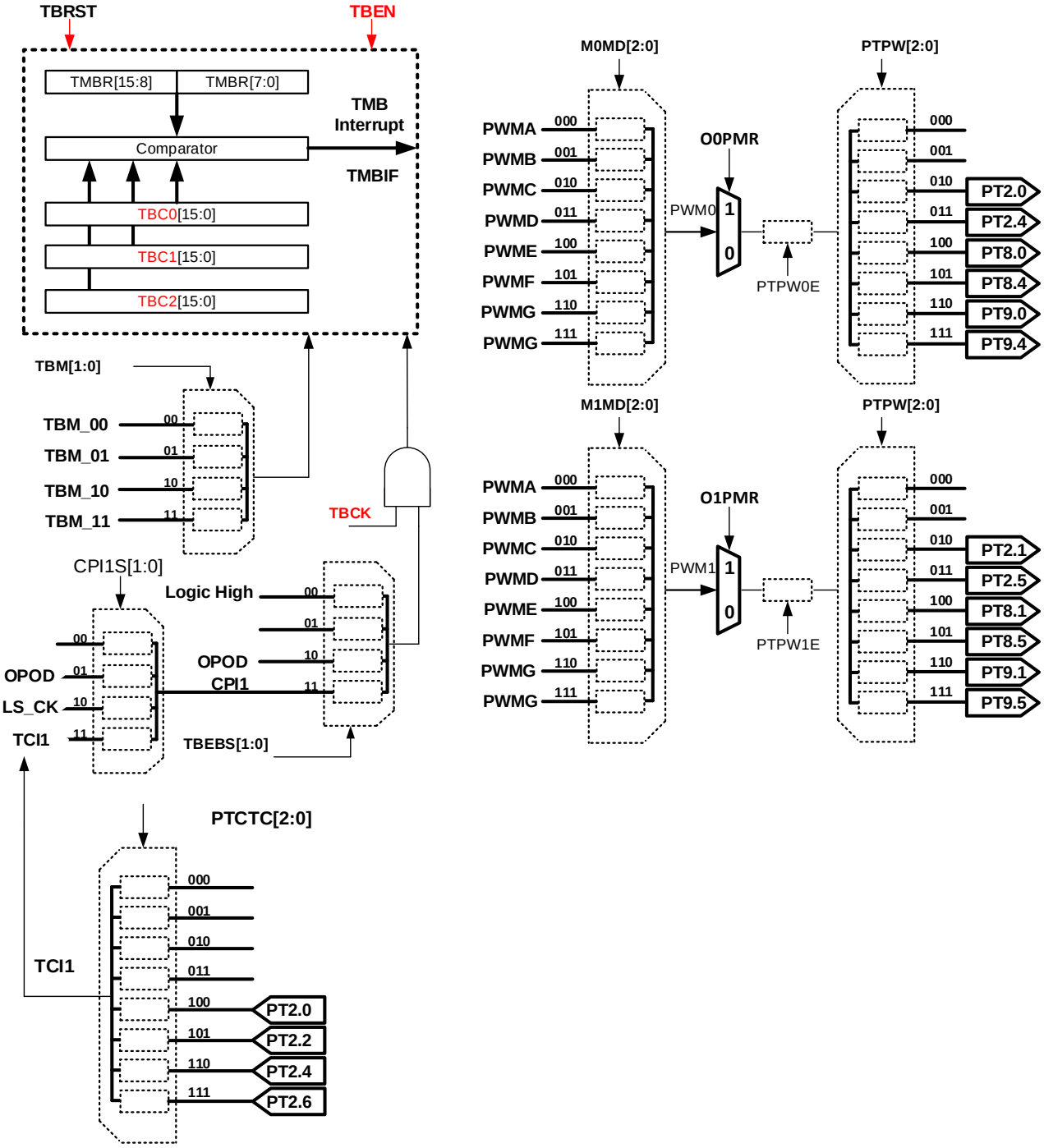
WDTP[2:0]	WDTO[15:0]
000	FWT/2
001	FWT/8
010	FWT/32
011	FWT/128
100	FWT/512
101	FWT/2048
110	FWT/8192
111	FWT/32768

4.12 定時計數器 A 網路

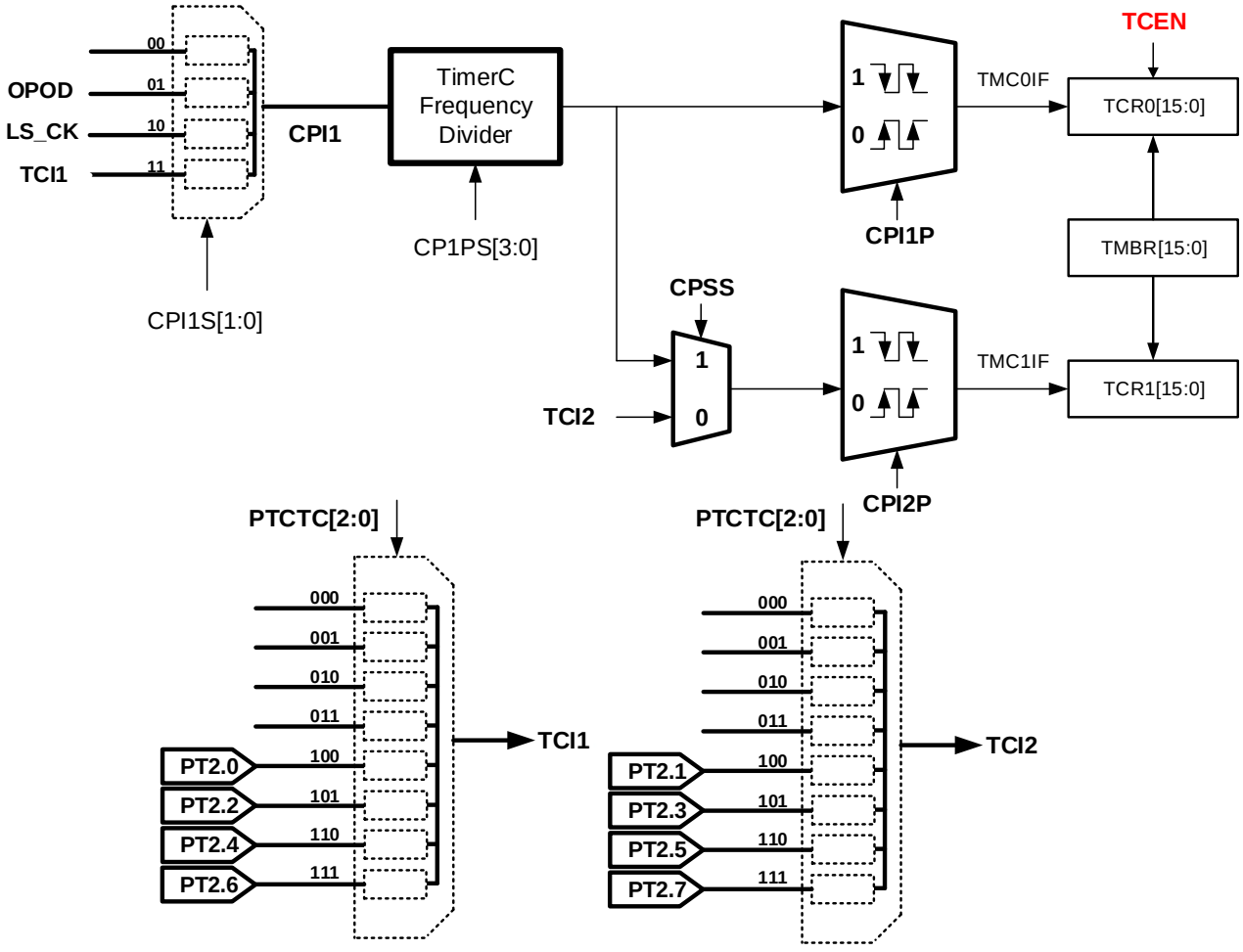


TMAS[3:0]	TMAR[15:0]	TMAS[3:0]	TMAR[15:0]
0000	TACK/2	1000	TACK/512
0001	TACK/4	1001	TACK/1024
0010	TACK/8	1010	TACK/2048
0011	TACK/16	1011	TACK/4096
0100	TACK/32	1100	TACK/8192
0101	TACK/64	1101	TACK/16384
0110	TACK/128	1110	TACK/32768
0111	TACK/256	1111	TACK/65536

4.13 定時計數器 B 網路

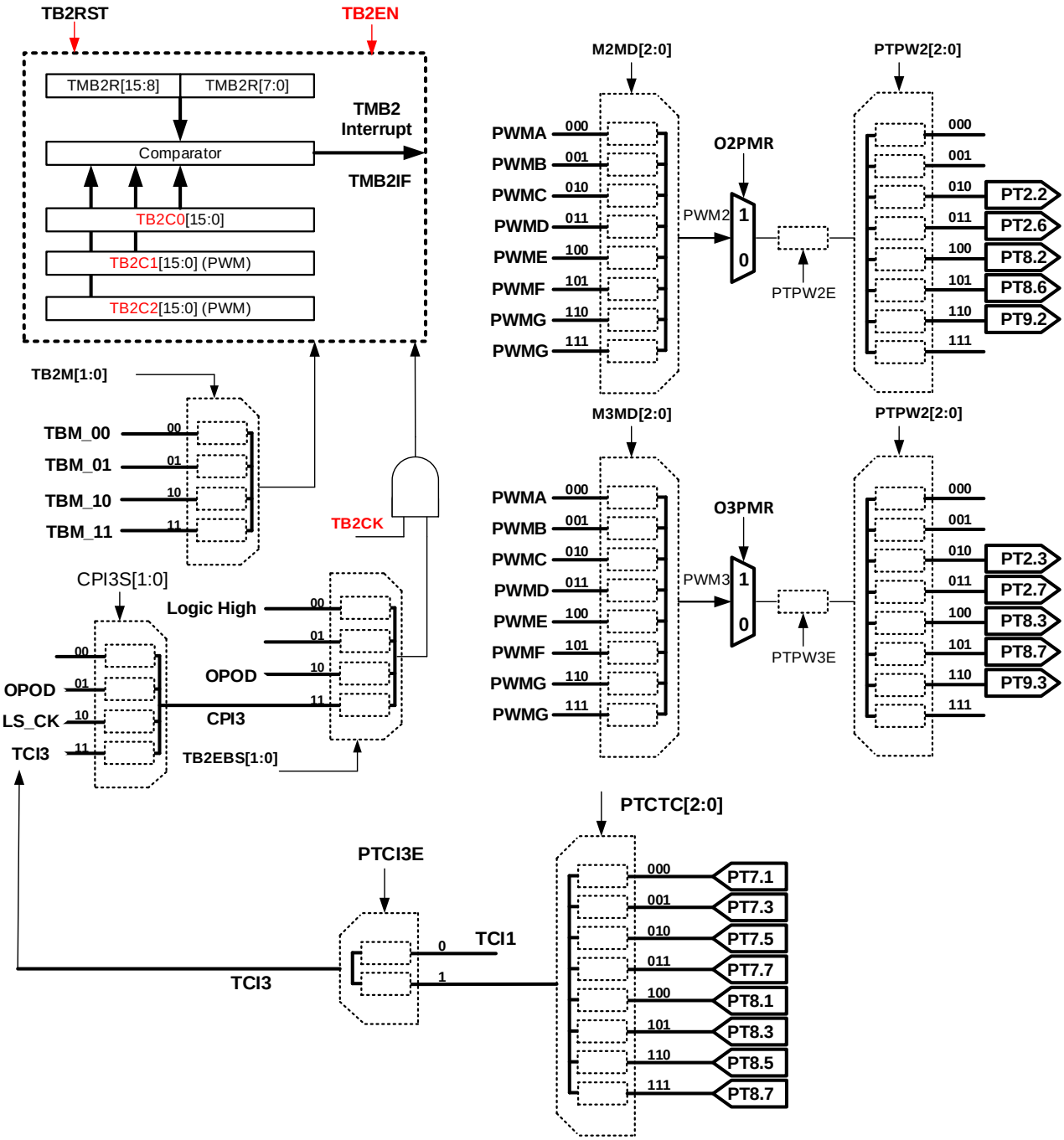


4.14 定時計數器 C 網路

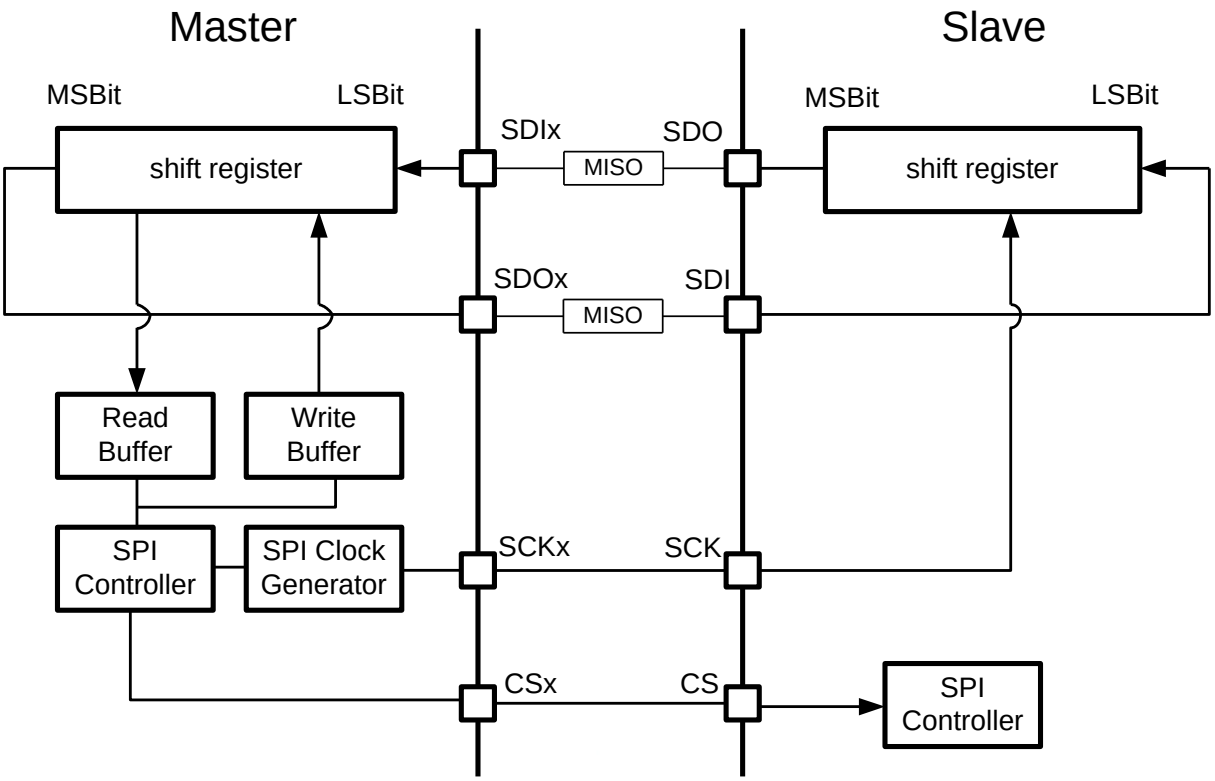


CP1PS[3:0]	CPI1 Divider	CP1PS[3:0]	CPI1 Divider
0000	CPI1/1	1000	CPI1/256
0001	CPI1/2	1001	CPI1/512
0010	CPI1/4	1010	CPI1/1024
0011	CPI1/8	1011	CPI1/2048
0100	CPI1/16	1100	CPI1/4096
0101	CPI1/32	1101	CPI1/8192
0110	CPI1/64	1110	CPI1/16384
0111	CPI1/128	1111	CPI1/32768

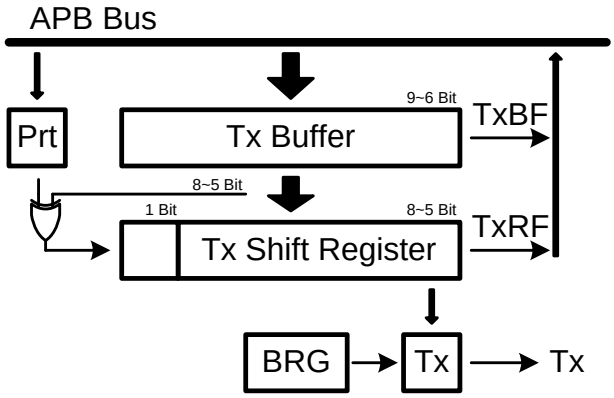
4.15 定時計數器 B2 網路



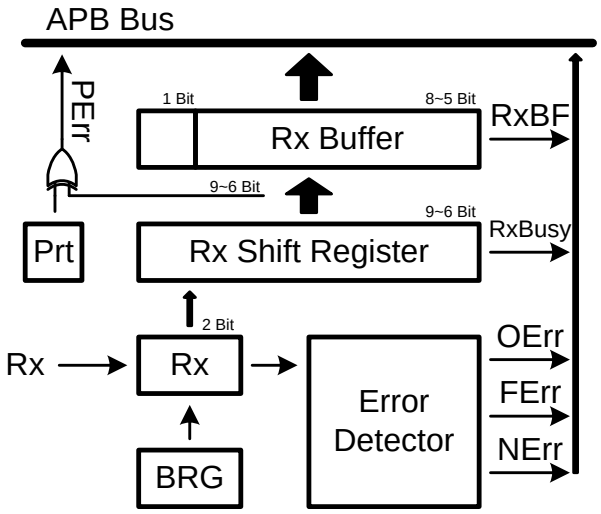
4.16 32-bit SPI 網路



4.17 UART 網路

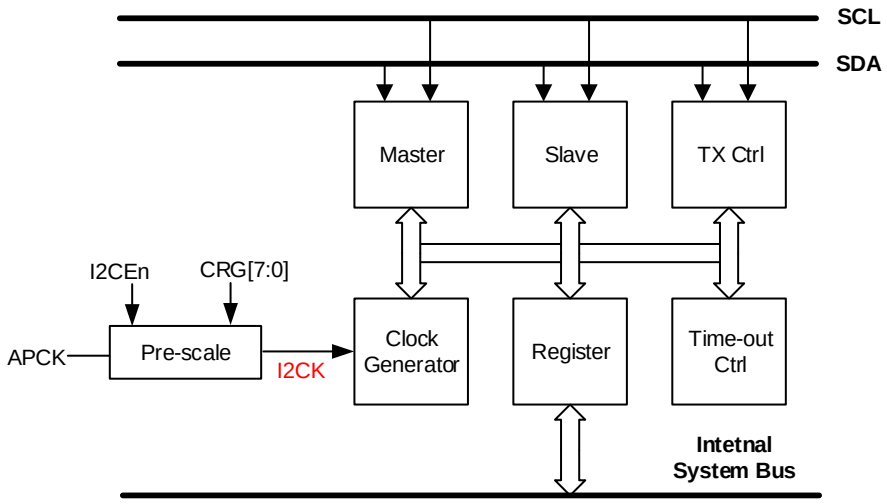


UART Transmit Block Diagram

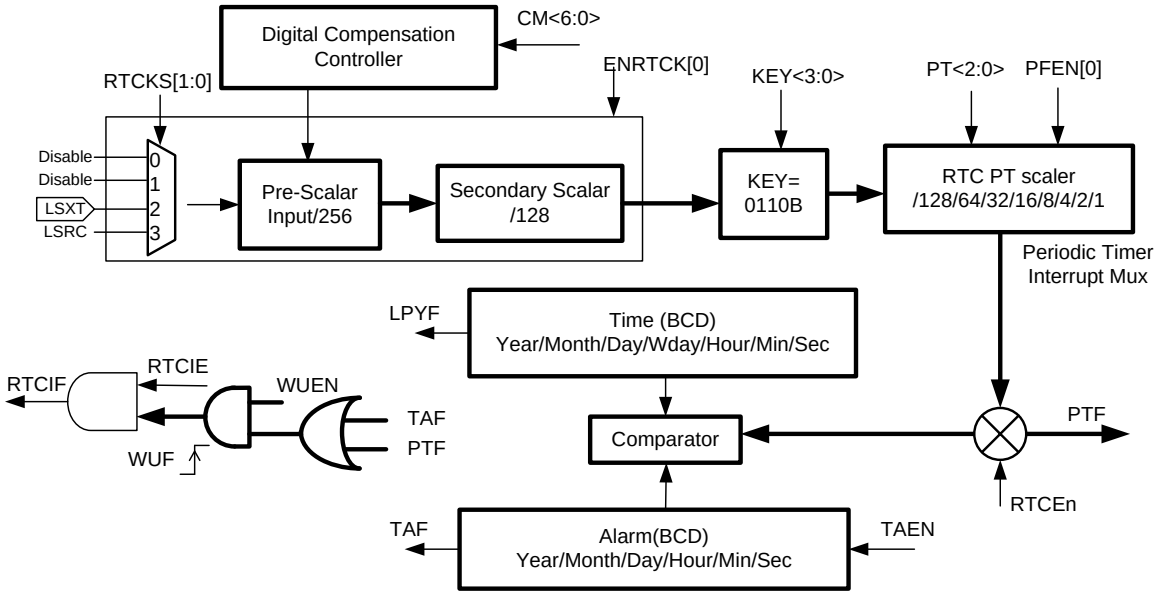


UART Receive Block Diagram

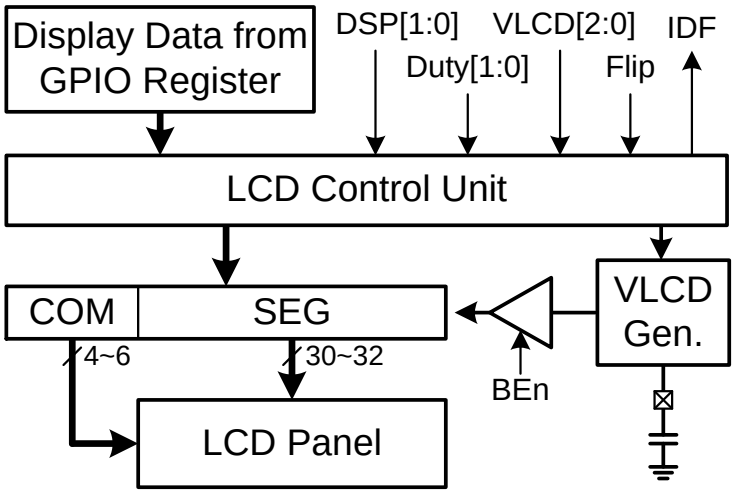
4.17 I2C 網路



4.18 硬體萬年曆 RTC 網路



4.19 LCD 網路


Display Data from GPIO Register
DSP[1:0]
Duty[1:0]
VLCD[2:0]
Flip
IDF
LCD Control Unit
COM
SEG
4~6
30~32
BEn
VLCD Gen.
LCD Panel

5. Electrical Characteristics

Absolute maximum ratings over operating free-air temperature (unless otherwise noted)
Voltage applied at VDD3V to VSS ……−0.2 V to 4.0 V
Voltage applied to any pin …….... −0.2 V to VDD3V + 0.3 V
Diode current at any device terminal…… ±2mA
Storage temperature, Tstg: (UN programmed device) ..... −55℃ to 150℃
(Programmed device) …….. −40℃ to 85℃
Soldering Temperature (10 Sec) . . . . +260°C
Maximum output current sink by any PORT2 to PORT13 I/O PIN ……10mA

5.1 Recommended Operating Conditions

VDD3V=3.0V.TA=25℃,Unless Otherwise Noted

Parameter	Sym.	Test Conditions	Min.	Typ.	Max.	Unit
Supply Voltage	VDD3V	Digital power	2.2	3.0	3.6	V
Supply Current	I_Sleep	Sleep Mode		2.5	5	uA
	I_Idle01	LSRC=35KHz LPO IDLE Mode		5	10	uA
	I_Idle02	LSXT=32768Hz IDLE Mode		6.5	12	uA
	I_Idle03	HSRC=2MHz+IDLE Mode		50	70	uA
	I_Idle04	HSRC=4MHz+IDLE Mode		100	130	uA
	I_Idle05	HSRC=10MHz+IDLE Mode		200	260	uA
	I_Idle06	HSRC=16MHz+IDLE Mode (VDD>= 2.6V)		350	460	uA
	Free Run_01MHz	HSRC=2MHz@CPU_CK:2MHz/2		0.6	0.8	mA
	Free Run_02MHz	HSRC=2MHz@CPU_CK:2MHz		1.0	1.2	mA
	Free Run_04MHz	HSRC=4MHz@CPU_CK:4MHz		2.0	2.4	mA
	Free Run_10MHz	HSRC=10MHz@CPU_CK:10MHz		3.0	3.6	mA
	Free Run_16MHz	HSRC=16MHz@CPU_CK:16MHz (VDD>= 2.6V)		4.0	4.8	mA
	Free Run_35KHz	LSRC=35KHz @CPU_CK: LSRC (Low power mode)		20	30	uA
Power Up Delay	$t_{PU,DLY}$	Power on or wake up from sleep mode		64	80	ms

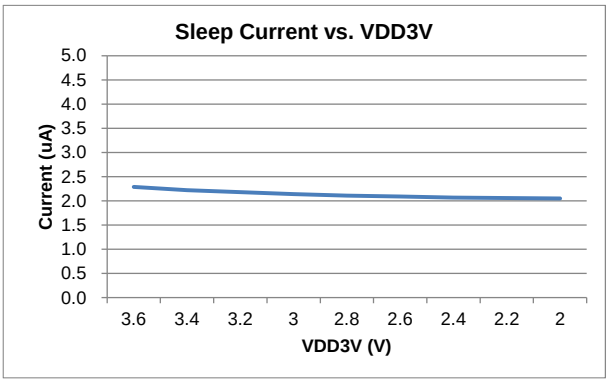


Figure5.1-1 Sleep Current vs. VDD3V

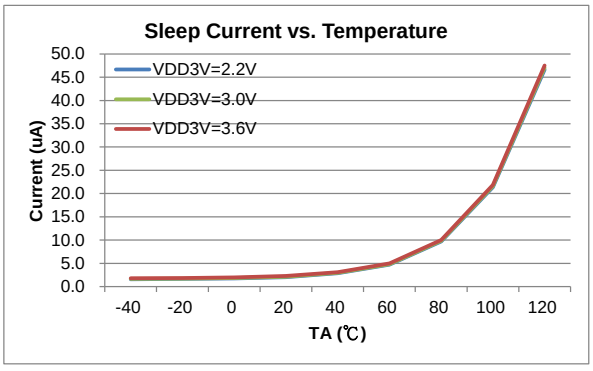


Figure5.1-2 Sleep Current vs. Temperature

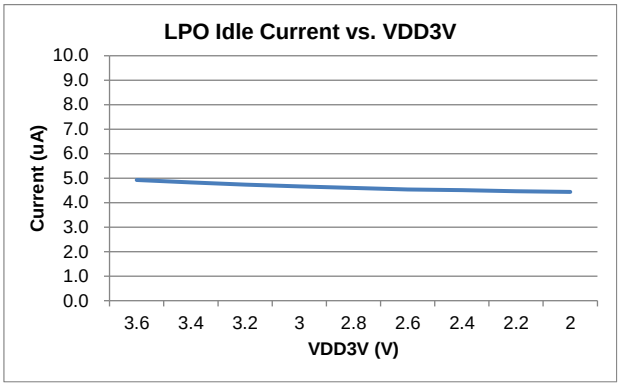


Figure5.1-3 LPO Idle Current vs. VDD3V

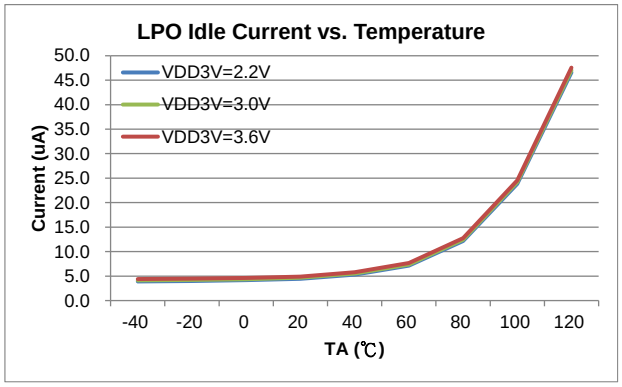


Figure5.1-4 LPO Idle Current vs. Temperature

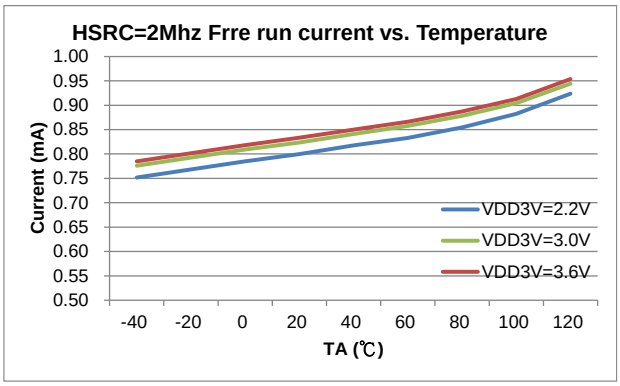


Figure5.1-5 2MHz Free run current vs. Temperature

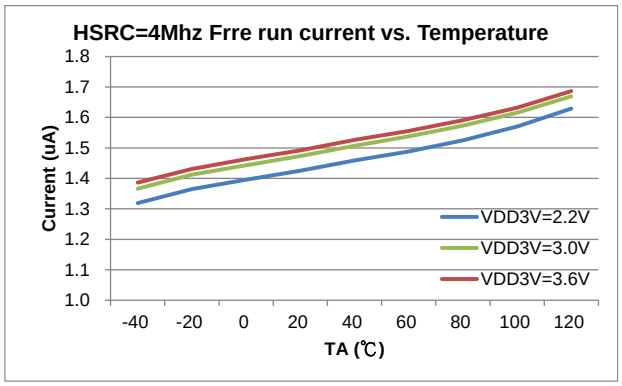


Figure5.1-6 4MHz Free run current vs. Temperature

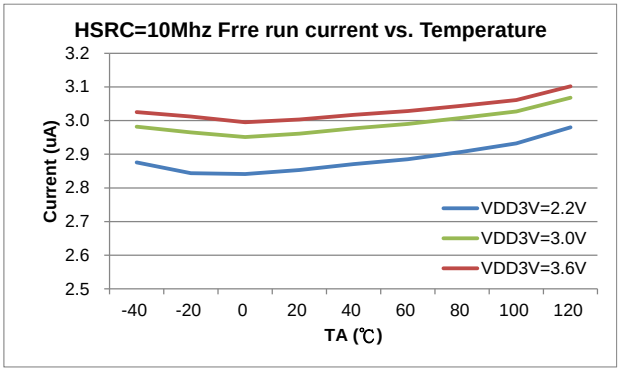


Figure5.1-7 10MHz Free run current vs. Temperature

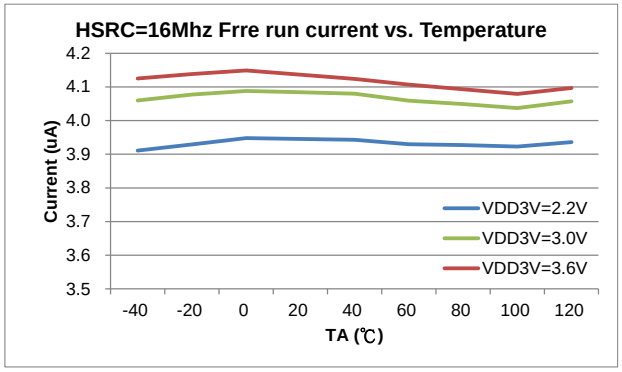


Figure5.1-8 16MHz Free run current vs. Temperature

5.2 Clock System

Typical values are at T_A=25℃ and VDD3V = 3.0V.Unless otherwise noted.

Sym.	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
External High Speed Oscillator						
VDD3V	Operation voltage		2.2		3.6	V
F_{XHS}	High speed oscillator frequency	VDD3V = 2.2V ~ 3.6V OHS_HS = 1b			10	MHz
		VDD3V = 2.6V ~ 3.6V OHS_HS = 1b			16	MHz
		VDD3V = 2.2V ~ 3.6V OHS_HS = 0b			4	MHz
I_{XHS}	High speed oscillator current	F_{XHS} = 16MHz, OHS_HS = 1b, (VDD>= 2.6V)		125		uA
D_{XHS}	Duty of high oscillator		40		60	%
External Low Speed Oscillator						
F_{XLS}	Low speed oscillator frequency	VDD3V = 2.2V ~ 3.6V		32.768		KHz
I_{XLS}	Low speed oscillator current			4		uA
D_{XLS}	Duty of low speed oscillator		40		60	%
RTC	Normal Mode	VDD3V=3.0V @Flash Run		22		uA
Internal High Speed Oscillator						
F_{HAO}	Internal high speed oscillator frequency	F_{HAO} = 2MHz, F_{HAO} = 2MHz, after trim Note1	-10% -2%	2 1.843	+10% +2%	MHz
		F_{HAO} = 4MHz, F_{HAO} = 4MHz, after trim Note1	-10% -2%	4 4.147	+10% +2%	MHz
		F_{HAO} = 10MHz, F_{HAO} = 10MHz, after trim Note1	-10% -2%	10 9.216	+10% +2%	MHz
		F_{HAO} = 16MHz, F_{HAO} = 16MHz, after trim Note1	-10% -2%	16 15.667	+10% +2%	MHz
	Voltage coefficient	VDD3V = 2.2V ~ 3.6V	-1.5		+1.5	%
T_{HAO}	Temperature coefficient	-40~85℃	-2.5		+2.5	%
I_{HAO}	Internal high speed oscillator current	F_{HAO} = 2MHz		20		uA
		F_{HAO} = 16MHz (VDD>= 2.6V)		105		uA
D_{HAO}	Duty of oscillator		40		60	%
WT_{HAO}	Wake up time	F_{HAO} = 2MHz		30		us
Internal Low Speed Oscillator						
F_{LPO}	Internal low speed oscillator frequency	VDD3V = 3.0V	-20%	35	+20%	KHz
	Voltage coefficient	VDD3V = 2.2V ~ 3.6V	-1.5		+1.5	%
T_{LPO}	Temperature coefficient	-40~85℃	-5		5	%
I_{LPO}	Internal low speed oscillator current			2.5		uA
D_{LPO}	Duty of low speed oscillator		40		60	%

Note1 :

After Trim: According to the factory calibration parameters of HAO to calibrate HAO, and need to corresponding to the selected HAO frequency. Configure the register 0x40304[7:0]. Please refer to the chapter 6.1.2 of “UG-HY16F3981_TC” to know how to use that in detail.

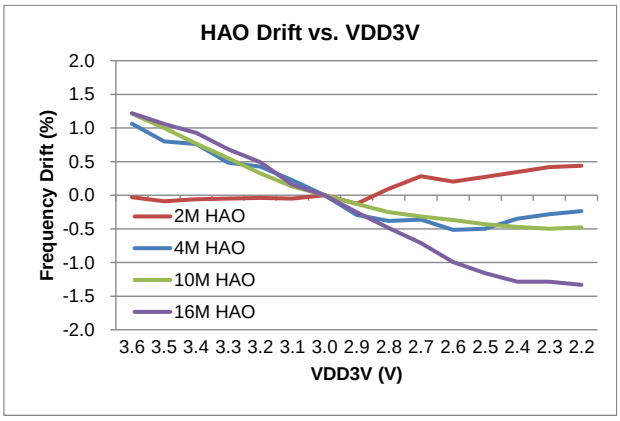


Figure5.2-1 HAO Drift vs. VDD3V

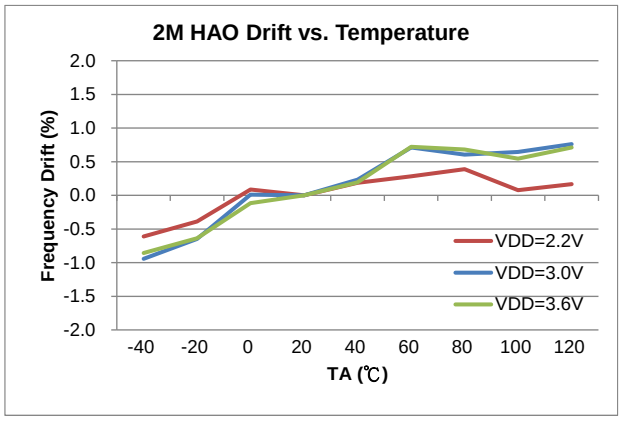


Figure5.2-2 2MHz HAO Drift vs. Temperature

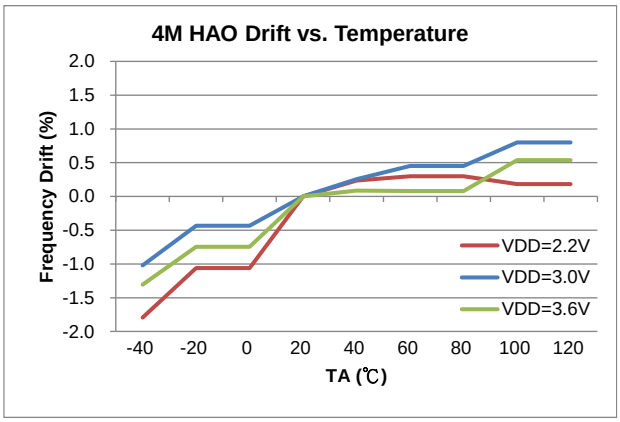


Figure5.2-3 4MHz HAO Drift vs. Temperature

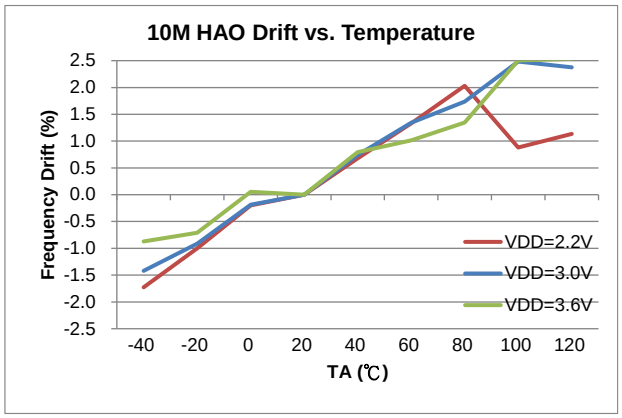


Figure5.2-4 10MHz HAO Drift vs. Temperature

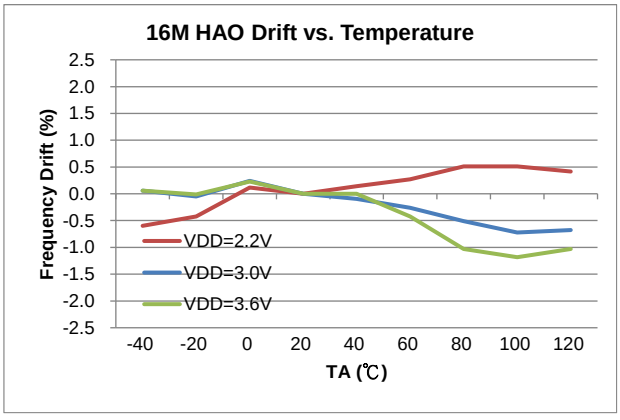


Figure5.2-5 16MHz HAO Drift vs. Temperature

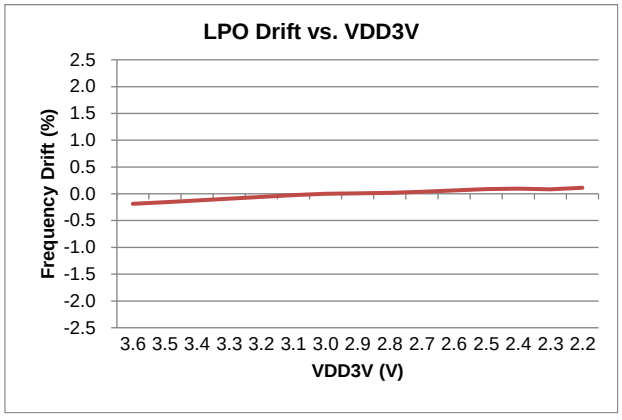


Figure5.2-5 LPO Drift vs. VDD3V

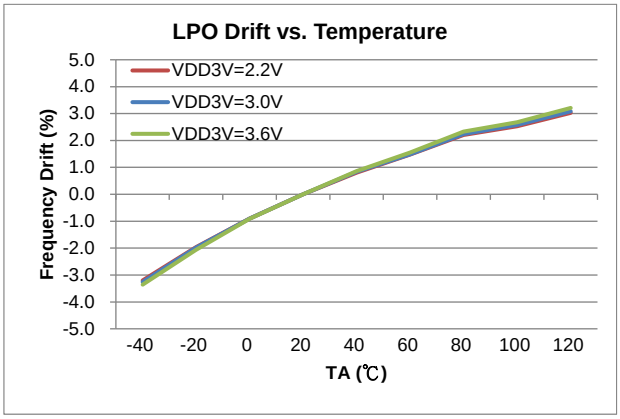


Figure5.2-5 LPO Drift vs. Temperature

5.3 Power Management System

Typical values are at T_A=25℃ and VDD3V = 3.0V. Unless otherwise noted.

Sym.	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
VDDA LDO						
	Output voltage error		-5		5	%
	Capacitor loading		0.1	1	10	uF
	Settling time	Capacitor loading = 0.1uF, 99% of VDDA		100		us
	Operation current	Bias + Band gap + VDDA LDO		35	50	uA
	Dropout voltage	I_L=10mA		0.2		V
	Voltage coefficient	VDD3V = 2.5 ~ 3.6V		0.1		%/V
	VDDA voltage 1 0x40400[19:18]=00b	I_L = 0.1mA	2.3	2.4		V
	VDDA voltage 2 0x40400[19:18]=01b	I_L = 0.1mA		2.6		V
	VDDA voltage 3 0x40400[19:18]=10b	I_L = 0.1mA		2.9		V
	VDDA voltage 4 0x40400[19:18]=11b	I_L = 0.1mA		3.2		V
	Temperature coefficient	By using BRG VDDA=3.0V		100		ppm/°C
VDD18 LDO						
	Output voltage		1.7	1.8	1.9	V
	Capacitor loading		100	1000	2200	nF
	Voltage coefficient	VDD3V= 2.2 ~ 3.6V		1		%/V
	Temperature coefficient			50		ppm/°C
	Load regulation	Load = 0.1~1mA		0.1		V/A
	Dropout voltage	Load = 1mA		0.2		V
REFO Buffer						
	Output voltage		1.1	1.2	1.3	V
	Capacitor loading		22	100	1000	nF
	Operation current			20		uA
	Output current	1% change voltage	-1		1	mA
	Temperature coefficient	VDDA=2.9V		80		ppm/°C
	Voltage coefficient	VDDA= 2.4V ~ 3.6V		0.1		%/V

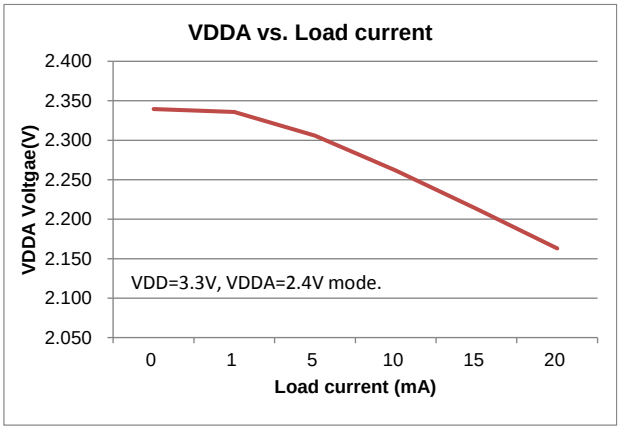


Figure5.3-1 VDDA=2.4V vs. IL

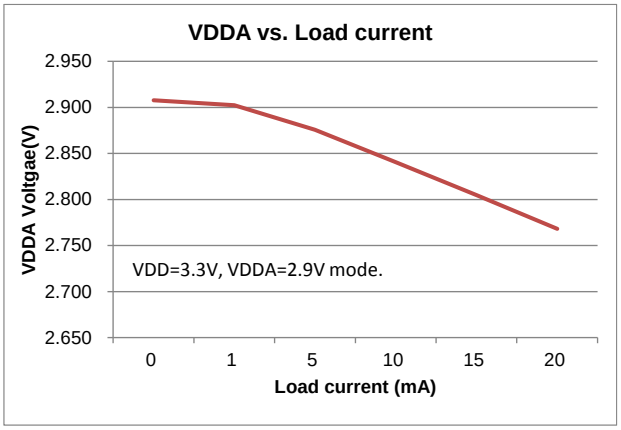


Figure5.3-2 VDDA=2.9V vs. IL

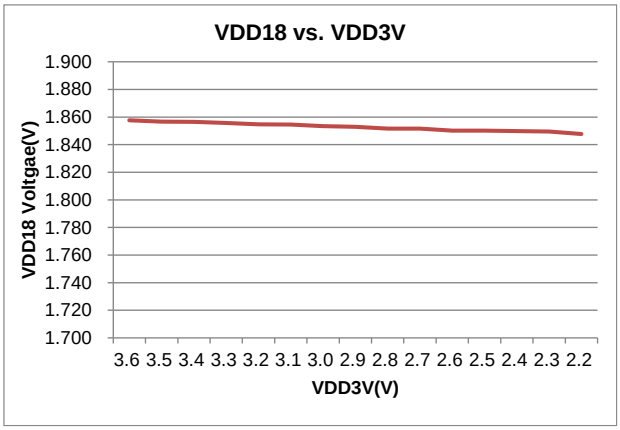


Figure5.3-3 VDD18 vs. VDD3V

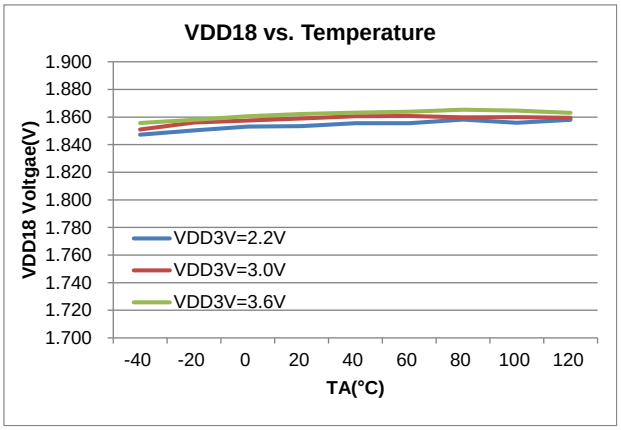


Figure5.3-4 VDD18 vs. Temperature

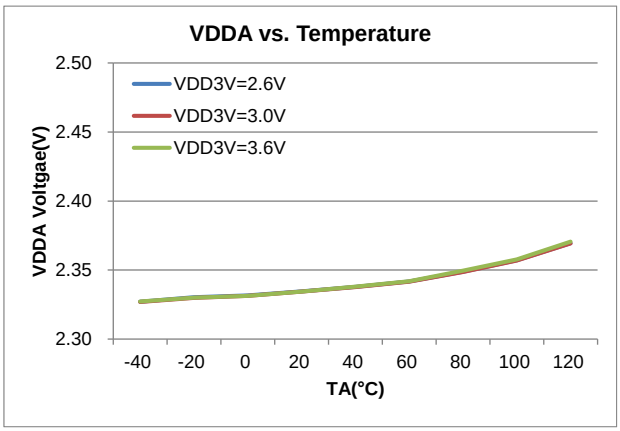


Figure5.3-5 VDDA=2.4V vs. Temperature

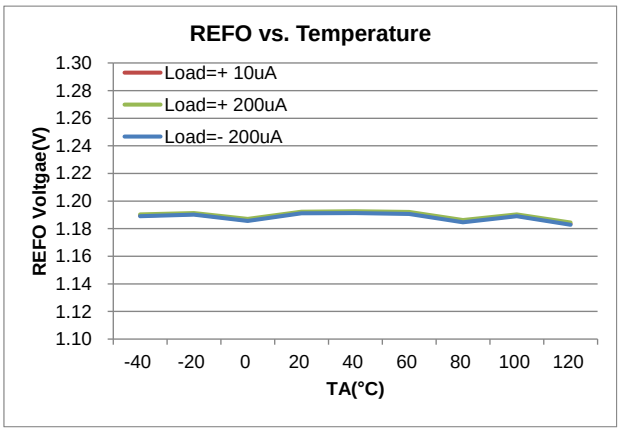


Figure5.3-6 REFO vs. Temperature

5.4 Reset Management System

Typical values are at T_A=25℃ and VDD3V = 3.0V. Unless otherwise noted.

Sym.	Parameter	Min.	Typ.	Max.	Unit
BOR	Pulse length needed to accepted reset internally, $t_{d\text{-}LVR}$	2			us
	VDD Start Voltage to accepted reset internally (L→H),V_{LVR}	1.8	1.95	2.1	V
	VDD Start Voltage to accepted reset internally (H→L),V_{HYS}	1.7	1.87	2.05	V
	Temperature drift, T_A=-40℃~85℃	-50		+50	mV
	Hysteresis, $V_{HYS\text{-}LVR}$		80		mV
POR	Operation Slew Rate			0.1	V/us
	Start Voltage to accepted reset	0.6			V

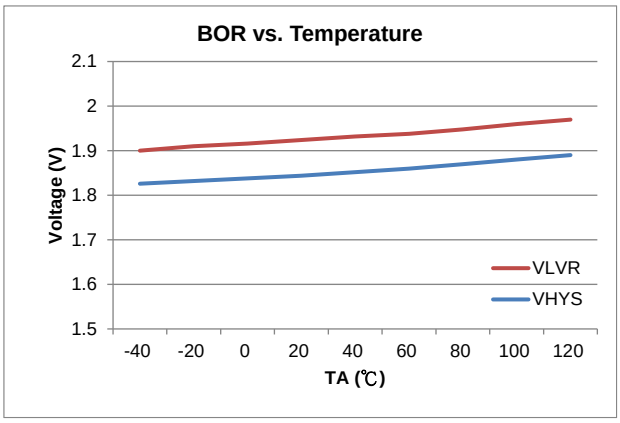


Figure5.4 VLVR and VHYS vs. Temperature

5.5 GPIO Port System

Typical values are at T_A=25℃ and VDD3V = 3.3V. Unless otherwise noted.

Sym.	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
PT 1.0 ~ 4.0 GPIO Port						
R_{PU}	Internal pull high resistor		65	85	105	kΩ
V_{IH}	Input high voltage		0.7*VDD3V			V
V_{IL}	Input low voltage				0.3*VDD3V	V
I_{OH}	Source current			10		mA
I_{OL}	Sink current			10		mA
PT 6.0 ~ 9.5 GPIO Port						
V_{IH}	Input high voltage		0.6*VDD3V			V
V_{IL}	Input low voltage				0.3*VDD3V	V
I_{OH}	Source current	VDD3V-0.3V		10		mA
I_{OL}	Sink current	VSS+0.3V		10		mA

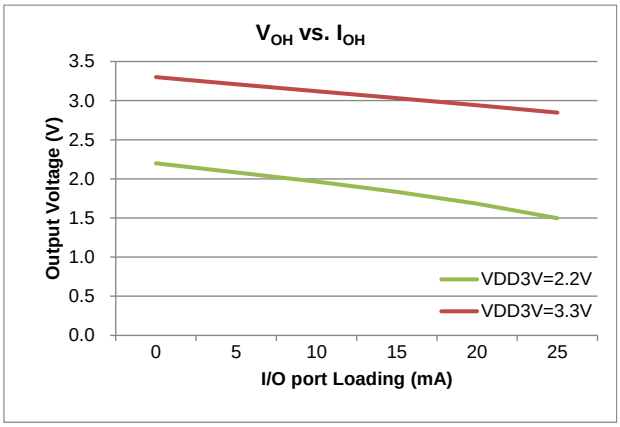


Figure5.5-1 VOH vs. IOH

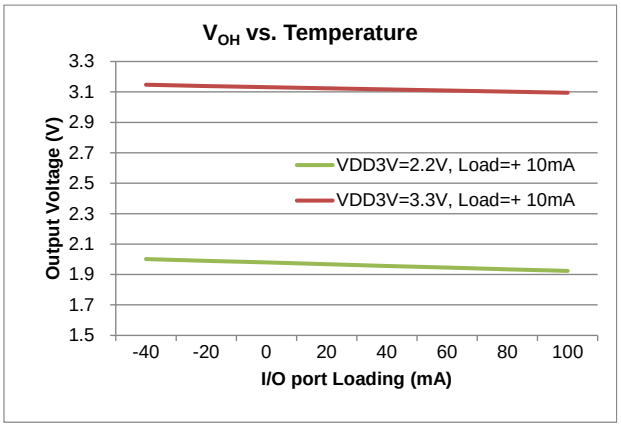


Figure5.5-2 VOH vs. Temperature

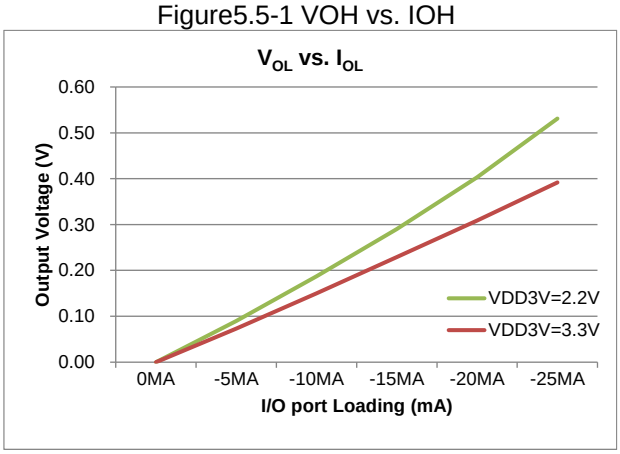


Figure5.5-3 VOL vs. IOL

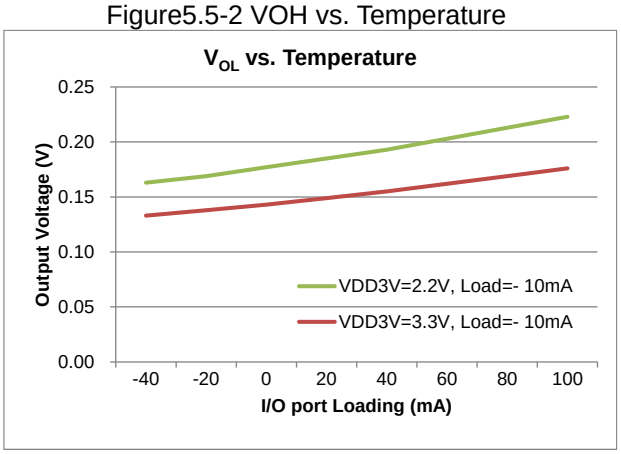


Figure5.5-4 VOL vs. Temperature

5.6 ΣΔADC ENOB and RMS Noise

Typical values are at TA=25℃ and VDD3V = 3.3V, VDDA=2.4V and HS_CK=4MHz, unless otherwise noted.HY16F3981 provides important input noise specification that aims at ΣΔADC. Table 5.6-1 and Table 5.6-2 lists out the relations of typical noise specification, Gain, Output rate, and maximum input voltage of single end. Test condition configuration and external input signal short, voltage reference: 1.2V and 1024 records were sampled. IA Chopper On means register IACHM=11b.

ENOB(RMS) with OSR/GAIN at A/D Clock=1Mhz, VDDA=2.4V, VREF=1.2V, IA Chopper On

Max. Vin(mV) =0.9*VREF (1)	OSR					64	128	256	512	1024	2048	4096	8192	16384	32768
	Output rate(HZ)					15625	7813	3906	1953	977	488	244	122	61	31
	Gain	=	IA	×	ADGN										
±1080	1	=	off	×	1	15.3	16.9	17.5	18.0	18.3	18.7	19.5	20.2	20.6	21.0
±540	2	=	off	×	2	15.2	16.7	17.3	17.8	18.2	18.8	19.3	19.8	20.2	20.5
±270	4	=	off	×	4	15.2	16.4	17.1	17.5	18.0	18.6	19.0	19.5	19.8	20.2
±135	8	=	off	×	8	14.9	16.1	16.6	17.2	17.6	18.2	18.5	18.9	19.3	19.6
±270	4	=	4	×	1	15.2	16.6	17.1	17.6	17.9	18.4	18.8	19.6	20.2	20.5
±135	8	=	4	×	2	14.8	15.9	16.5	17.0	17.4	17.9	18.4	19.0	19.4	20.0
±67.5	16	=	4	×	4	14.5	15.1	15.7	16.2	16.6	17.1	17.7	18.2	18.6	19.1
±33.75	32	=	4	×	8	13.7	14.2	14.7	15.2	15.7	16.3	16.8	17.2	17.7	18.1
±135	8	=	8	×	1	15.2	16.5	17.0	17.5	18.0	18.4	19.1	19.6	20.0	20.5
±67.5	16	=	8	×	2	14.8	15.9	16.3	16.8	17.3	17.9	18.3	18.9	19.3	19.7
±33.75	32	=	8	×	4	14.3	15.0	15.4	16.0	16.5	17.0	17.5	18.0	18.4	19.0
±16.875	64	=	8	×	8	13.5	14.0	14.5	15.0	15.5	16.0	16.5	17.0	17.5	17.9
±67.5	16	=	16	×	1	15.0	16.1	16.7	17.1	17.5	18.1	18.7	19.1	19.6	20.1
±33.75	32	=	16	×	2	14.5	15.3	15.8	16.3	16.7	17.3	17.8	18.2	18.7	19.3
±16.875	64	=	16	×	4	13.8	14.3	14.9	15.3	15.8	16.4	16.8	17.4	17.8	18.4
±8.4375	128	=	16	×	8	12.8	13.4	13.9	14.4	14.8	15.4	15.9	16.3	16.9	17.4
±33.75	32	=	32	×	1	14.6	15.3	15.9	16.4	16.9	17.4	17.9	18.4	18.9	19.4
±16.875	64	=	32	×	2	13.8	14.4	14.9	15.4	15.9	16.4	16.9	17.5	17.9	18.4
±8.4375	128	=	32	×	4	12.9	13.4	14.0	14.5	14.9	15.5	16.0	16.4	17.0	17.4
±4.21875	256	=	32	×	8	12.0	12.5	12.9	13.5	13.9	14.5	15.0	15.5	16.0	16.4

(1) Max.Vin (mV) is the max. input voltage of single end to ground (VSS).

Table 5.6-1 ΣΔADC ENOB Table

RMS Noise(uV) with OSR/GAIN at A/D Clock=1Mhz, VDDA=2.4V, VREF=1.2V, IA Chopper On															
Max. Vin(mV) =0.9*VREF	OSR					64	128	256	512	1024	2048	4096	8192	16384	32768
	Output rate(HZ)					15625	7813	3906	1953	977	488	244	122	61	31
	Gain	=	IA	×	ADGN										
±1080	1	=	off	×	1	58.85	19.18	12.49	8.86	7.08	5.33	3.24	1.98	1.46	1.11
±540	2	=	off	×	2	31.64	11.13	7.10	5.13	3.92	2.52	1.75	1.28	1.00	0.79
±270	4	=	off	×	4	15.79	6.77	4.29	3.19	2.19	1.52	1.11	0.79	0.64	0.48
±135	8	=	off	×	8	9.30	4.20	2.91	1.98	1.42	1.00	0.79	0.61	0.45	0.38
±270	4	=	4	×	1	15.10	5.99	4.04	3.01	2.31	1.68	1.32	0.75	0.48	0.39
±135	8	=	4	×	2	9.94	4.69	3.25	2.25	1.73	1.21	0.83	0.57	0.42	0.28
±67.5	16	=	4	×	4	6.38	4.09	2.84	1.90	1.48	1.01	0.70	0.49	0.36	0.25
±33.75	32	=	4	×	8	5.56	3.99	2.74	1.93	1.35	0.91	0.65	0.49	0.33	0.26
±135	8	=	8	×	1	7.99	3.15	2.25	1.54	1.14	0.84	0.52	0.36	0.28	0.19
±67.5	16	=	8	×	2	5.05	2.44	1.81	1.26	0.88	0.60	0.45	0.31	0.22	0.17
±33.75	32	=	8	×	4	3.56	2.28	1.66	1.14	0.79	0.55	0.40	0.29	0.20	0.14
±16.875	64	=	8	×	8	3.21	2.23	1.56	1.13	0.78	0.56	0.38	0.28	0.19	0.15
±67.5	16	=	16	×	1	4.57	2.04	1.38	1.03	0.76	0.53	0.35	0.25	0.19	0.13
±33.75	32	=	16	×	2	3.12	1.83	1.29	0.94	0.70	0.46	0.32	0.25	0.17	0.11
±16.875	64	=	16	×	4	2.57	1.79	1.23	0.89	0.62	0.43	0.32	0.22	0.16	0.11
±8.4375	128	=	16	×	8	2.58	1.74	1.21	0.86	0.62	0.43	0.31	0.23	0.15	0.11
±33.75	32	=	32	×	1	3.02	1.76	1.20	0.85	0.61	0.43	0.29	0.21	0.15	0.10
±16.875	64	=	32	×	2	2.54	1.69	1.16	0.82	0.59	0.41	0.30	0.20	0.15	0.10
±8.4375	128	=	32	×	4	2.35	1.65	1.14	0.79	0.58	0.40	0.28	0.21	0.14	0.10
±4.21875	256	=	32	×	8	2.22	1.56	1.16	0.79	0.59	0.39	0.29	0.20	0.14	0.10

Table 5.6-2 ΣΔADC RMS Table

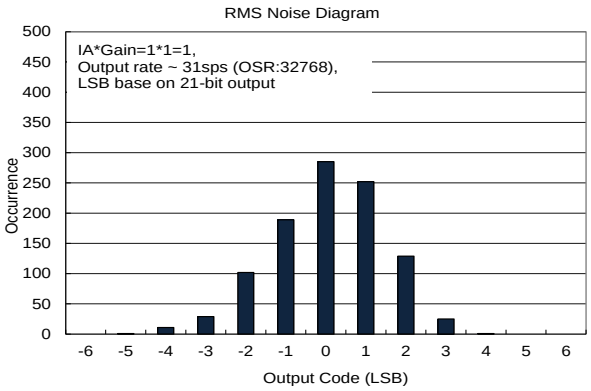


Figure5.6-1(a) RMS Noise Diagram

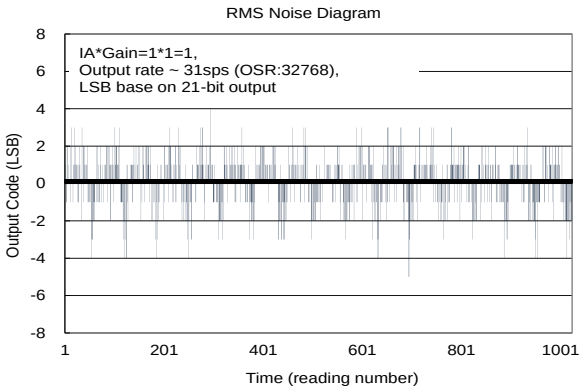


Figure5.6-1(b) Output Code Diagram

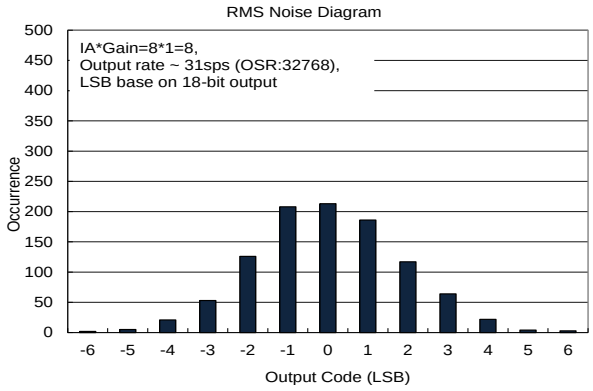


Figure5.6-2(a) RMS Noise Diagram

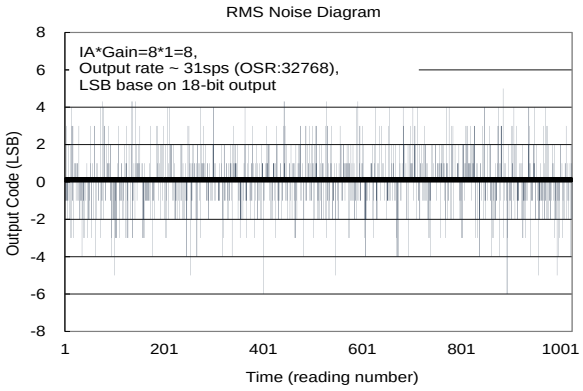


Figure5.6-2(b) Output Code Diagram

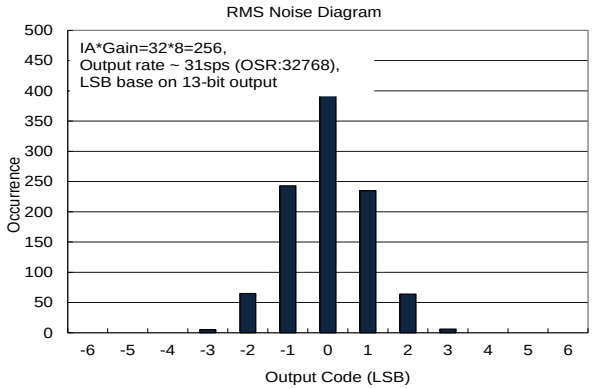


Figure5.6-3(a) RMS Noise Diagram

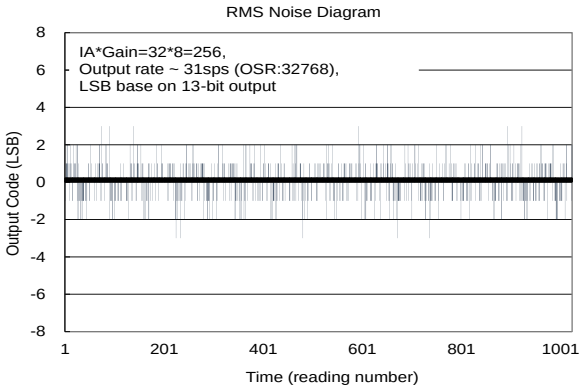


Figure5.6-3(b) Output Code Diagram

5.7 ADC Management System

All specifications at T_A=-40℃ to +85℃,
VDDA=REFP=3.0V, REFN=VSS, Unless otherwise noted.

Sym.	Parameter	Test Conditions		Min.	Typ.	Max.	Unit
Analog Inputs							
	Full-scale input voltage (VINP - AINN) Note1	Considering ADC performance matches ADC ENOB table. REFP=VDDA, REFN=VSS VREF be set to 1/2 only		±0.5*VREF/Gain			V
		Considering ADC performance matches ADC ENOB table. REFP=REFO_I REFN=VSS VREF be set to 1 only		±VREF/Gain			
	Common-mode input range	Gain = 1, @25℃		VSS-0.2V		VDDA	V
System Performance							
	Resolution	No missing codes			24		Bits
	Data rate				ADC Clock /OSR		SPS
	Digital filter settling time	Full setting			3		Data
	Integral nonlinearity (INL)	Differential input End-point fit, OSR=32768			15		PPM
	ADC Gain drift				2		ppm/℃
	Normal-mode rejection	f_{IN}=60Hz ±1Hz, Output rate = 31 SPS	Internal OSC		70		dB
			External OSC		80		dB
	Common-mode rejection	ΔVDDA = 0.1V @ DC			80		dB
	Input-referred noise	Output rate= 31 SPS, ADC Gain=1			0.38		uV, rms
	Power-supply rejection	ΔVDDA = 0.1V @ DC			80		dB
Voltage Reference Input							
	Voltage reference input	VREF = REFP - REFN				VDDA	V
	Positive Reference Input	REFP, @25℃		>REFN		VDDA	V
	Negative Reference Input	REFN, @25℃		VSS		<REFP	V
ADC Modulator Current							
ADC	ADC Modulator	VDD3V=3.3V,VDDA=2.4V, ADC Clock=1Mhz			350		uA
IA	ADC IA	VDD3V=3.3V,VDDA=2.4V			300		uA

Note1 :

當 REFP-REFN(VREF) = 1*VDDA 時,

則 VINP-VINN 的差動輸入信號不能大於 1/2*VDDA, 否則會有線性度問題

當 REFP-REFN(VREF) = 1/2*VDDA 時,

則 VINP-VINN 的差動輸入信號不能大於 0.9*VREF, 否則會有線性度問題

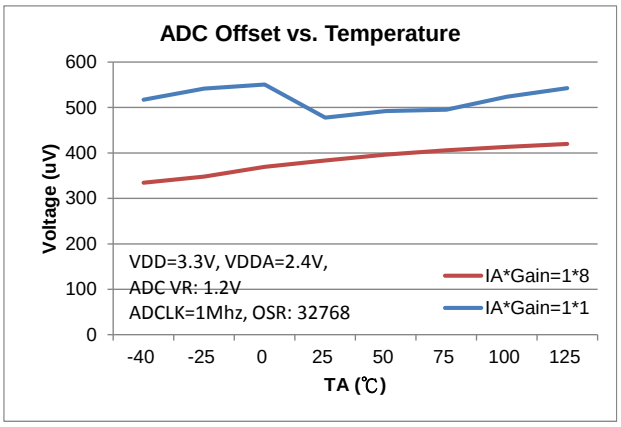


Figure5.7-1 ADC Offset vs. Temperature

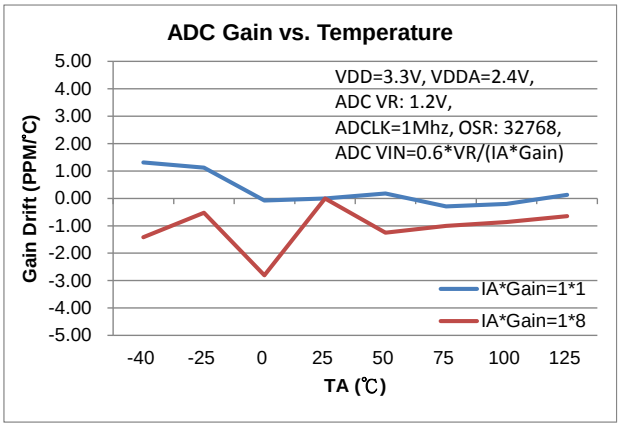


Figure5.7-3 ADC Gain Drift vs. Temperature

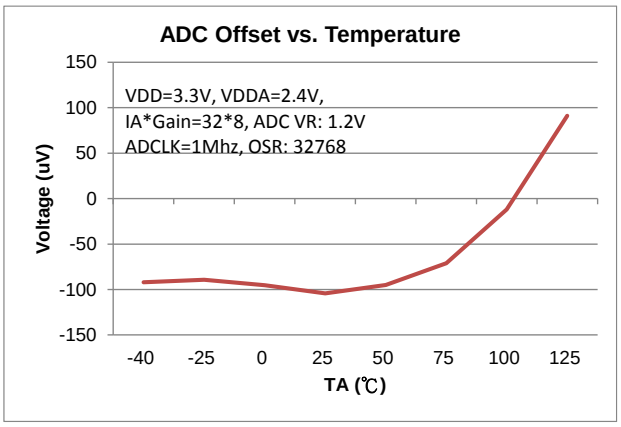


Figure5.7-2 ADC Offset vs. Temperature

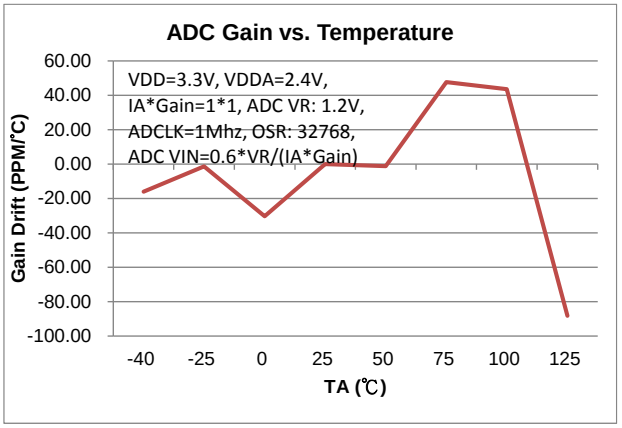


Figure5.7-4 ADC Gain Drift vs. Temperature

5.8 Internal Temperature Sensor

Typical values are at T_A=25℃, VDD3V = 3.0V, and VDDA=2.4V. Unless otherwise noted.

Sym.	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
TC_S	Sensor temperature drift			172		uV/℃
KT	Absolute temperature scale 0K			-283		℃
TC_{ERR}	One point calibrate error temperature	Calibration at 25℃ of -40℃~85℃		±2		℃

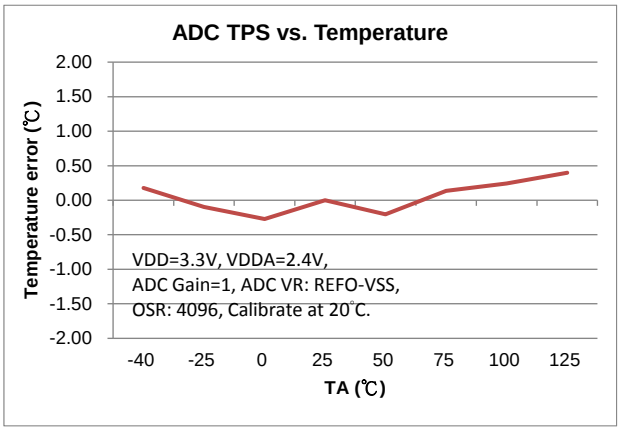


Figure5.8-1 ADC Temperature Sensor Error

5.9 12-Bit Resistance Ladders

Typical values are at T_A=25℃ and VDD3V = 3.0V. Unless otherwise noted.

Sym.	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
	Resolution	Monotonic		12		Bit
	Power Supply		2.4		VDDA	V
	Operation current			50		uA
V_{OUT}	Output range	DA output is between VR- and VR+	0		VDDA	V
V_{REFP}	Positive reference voltage range	V_{REFP} > V_{REFN}	0		VDDA	V
V_{REFN}	Negative reference voltage range		0		VDDA	V
R_{ON}	12-Bit Resistance ladders. output switch(DAOE switch resistance)	VDDA=2.4V 0.5V < DAO < VDDA-0.5V			200	Ω
		VDDA=2.4V 0.5V > DAO , DAO > VDDA-0.5V		10		Ω
R_{RSW}	Reference voltage switch(Vrefp switch resistance, Vrefn switch resistance)	V_{REFP} = 2.2V, V_{REFN} = 0V, VDDA = 2.4V		15	30	Ω
R_{LADDER}	One LSB resistance ladder		170	200	230	Ω
INL	Integral linearity error	VR+ = 2.4V, VR- = 0V (After compensation)		±3		LSB
DNL	Differential linearity error	VR+ = 2.4V, VR- = 0V (After compensation)			±1	LSB
E_{OS}	Offset error	VR+ = 2.4V, VR- = 0V			1	LSB
12-Bit Resistance Ladders.	(Vin Floating)	VDD3V=3.3V,VDDA=2.4V		0.1		uA

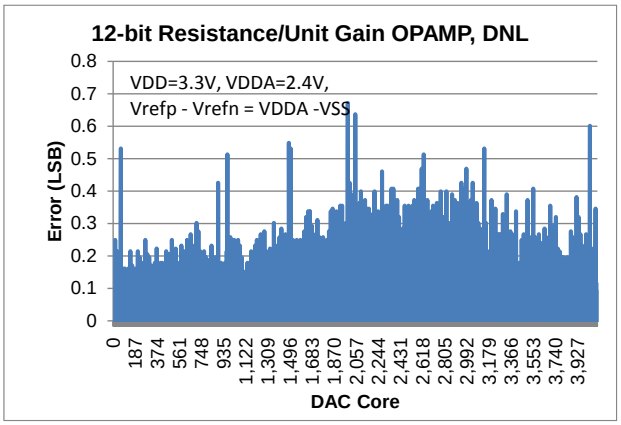


Figure5.9-1 12-Bit Resistance DNL

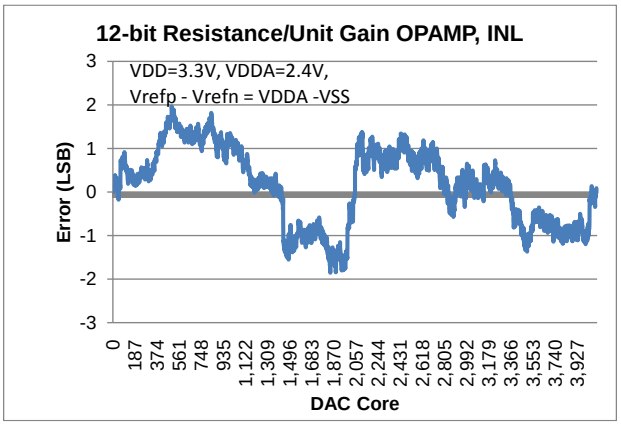


Figure5.9-2 12-Bit Resistance INL

5.10 Rail-to-rail OPAMP Management System

Typical values are at T_A=25℃, VDD3V = 3.0V, and C_{VLCD}=10uF. Unless otherwise noted.

Sym.	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
VDDA	Power supply		2.4		3.6	V
V_{OUT}	Output range		0		VDDA	V
V_{IN}	Input common range		0		VDDA	V
I_{OPA}	OPAMP current			120		uA
I_{OPA_LOAD}	Output current loading (push or pull)	VDDA = 3.0V, 0.3V< Output voltage <VDDA-0.3V			1	mA
		VDDA = 2.4V, 0.3V< Output voltage <VDDA-0.3V			0.5	mA
C_{LOAD}	Max output capacitor load				1	nF
SR	Slew rate	Loading R=10K, C=100pF, 0.3V to VDDA-0.3V		0.6		V/us
UGB	Unit gain bandwidth	Loading C=100pF		1000		KHz
V_{OS}	Offset error	Vin = 1.2V	-5		+5	mV
DFD	Digital filter delay	VDDA = 3.0V		2		us
C_{SA}	Sample capacitor			10		pF

5.11 LVD Comparator Management System

Typical values are at TA=25℃ and VDD3V = 3.0V. Unless otherwise noted.

Sym.	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
LVD	Operation current, I_{V12_BOR}			1		uA
	Operation current, I_{V12_BGR}			10		uA
	V12_BOR Reference Voltage		1.1	1.2	1.3	V
	V12_BOR Reference Voltage Temperature drift			50		PPM/℃
	V12_BOR Reference Voltage to VDD3V Voltage drift			±2		%/V
	V12_BGR Reference Voltage		1.15	1.2	1.25	V
	V12_BGR Reference Voltage Temperature drift			50		PPM/℃
	V12_BGR Reference Voltage to VDD3V Voltage drift			±0.2		%/V
	Compare reference voltage temperature drift, T_A = -40℃ ~ 85 ℃			50		ppm/℃
	Detect V_{DD3V} voltage rang by user option, V_{SVS} VLDS [3:0]=1111b			3.4		
	Detect V_{DD3V} voltage rang by user option, V_{SVS} VLDS [3:0]=1110b			3.3		V
	Detect V_{DD3V} voltage rang by user option, V_{SVS} VLDS [3:0]=1101b			3.2		
	Detect V_{DD3V} voltage rang by user option, V_{SVS} VLDS [3:0]=1100b			3.1		
	Detect V_{DD3V} voltage rang by user option, V_{SVS} VLDS [3:0]=1011b			3.0		
	Detect V_{DD3V} voltage rang by user option, V_{SVS} VLDS [3:0]=1010b			2.9		
	Detect V_{DD3V} voltage rang by user option, V_{SVS} VLDS [3:0]=1001b			2.8		
	Detect V_{DD3V} voltage rang by user option, V_{SVS} VLDS [3:0]=1000b			2.7		
	Detect V_{DD3V} voltage rang by user option, V_{SVS} VLDS [3:0]=0111b			2.6		
	Detect V_{DD3V} voltage rang by user option, V_{SVS} VLDS [3:0]=0110b			2.5		
	Detect V_{DD3V} voltage rang by user option, V_{SVS} VLDS [3:0]=0101b			2.4		
	Detect V_{DD3V} voltage rang by user option, V_{SVS} VLDS [3:0]=0100b			2.3		
	Detect V_{DD3V} voltage rang by user option, V_{SVS} VLDS [3:0]=0011b			2.2		
	Detect V_{DD3V} voltage rang by user option, V_{SVS} VLDS [3:0]=0010b			2.1		
	Detect V_{DD3V} voltage rang by user option, V_{SVS} VLDS [3:0]=0001b			2.0		
	Detect V_{DD3V} voltage rang by user option, V_{SVS} VLDS [3:0]=0000b			LVDIN		
LVD：Low Voltage Detect						

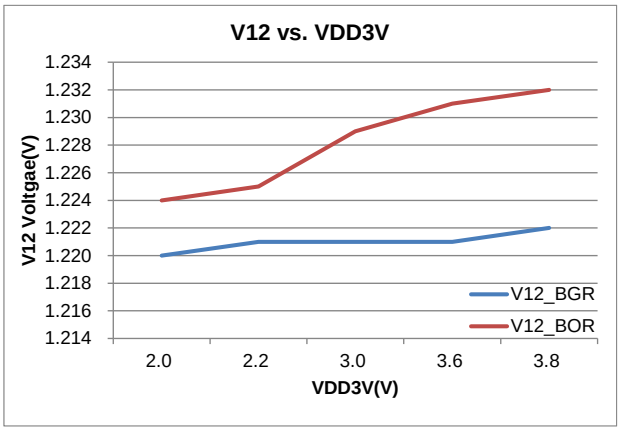


Figure5.11-1 V12 vs. VDD3V

5.12 LCD System

Typical values are at T_A=25℃, VDD3V = 3.3V, and C_{VLCD}=10uF. Unless otherwise noted.

Sym.	Parameter	Test Conditions		Min.	Typ.	Max.	Unit
I_{LCD}	Operation Current Charge Pump Mode		W/O Panel		10		uA
VLCD	Supply Voltage Range	VLCD	With Buffer	2.50		3.80	V
VLCD	Embedded Charge Pump Output Voltage @ VLCD Pin	VDD3V = 2.4V CVLCD = 10uF	Mode1: Data[1]=00_011B (After trim) Note1	-5%	3.43	+5%	V
			Mode1: Data[1]=00_011B	-10%	3.30	+10 %	
			Mode2: Data[1]=00_100B (After trim) Note1	-5%	3.16	+5%	
			Mode2: Data[1]=00_100B	-10%	3.00	+10 %	
			Mode3: Data[1]=00_101B (After trim) Note1	-5%	2.93	+5%	
			Mode3: Data[1]=00_101B	-10%	3.00	+10 %	
			Mode4: Data[1]=11_101B (After trim) Note1	-5%	2.73	+5%	
			Mode4: Data[1]=11_101B	-10%	2.80	+10 %	
			Mode5: Data[1]=01_101B (After trim) Note1	-5%	2.55	+5%	
			Mode5: Data[1]=01_101B	-10%	2.6	+10 %	
Z_{LCD}	Output Impedance With LCD Buffer	F_{LCD} = LS_CK/32/9, VLCD = 3.16V			10		KΩ

Data1 Bit: 0X41B10 [EN_Rshift1, EN_Rshift0], 0X41B00 [VLCD2, VLCD1, VLCD0]
Note1 :
After Trim : According to the factory calibration parameters of VLCD to calibrate VLCD, and need to corresponding to the selected VLCD voltage. User can refer to the document “UG-HY16F3981_TC” to know how to use that in detail.

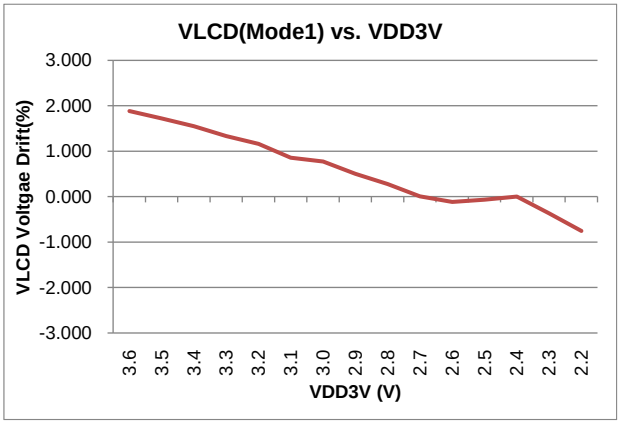


Figure5.12-1 VLCD(Mode1) vs. VDD3V

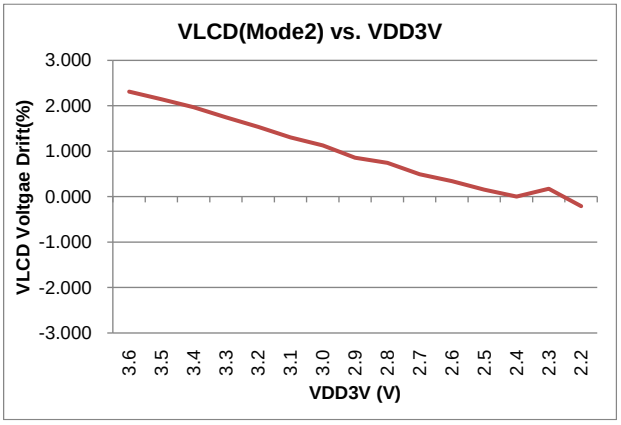


Figure5.12-2 VLCD(Mode2) vs. VDD3V

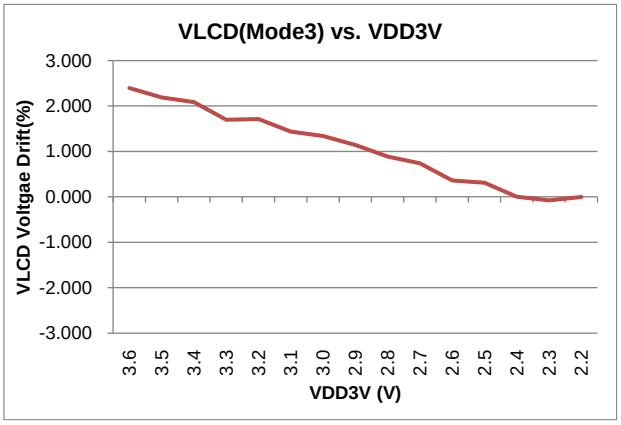


Figure5.12-3 VLCD(Mode3) vs. VDD3V

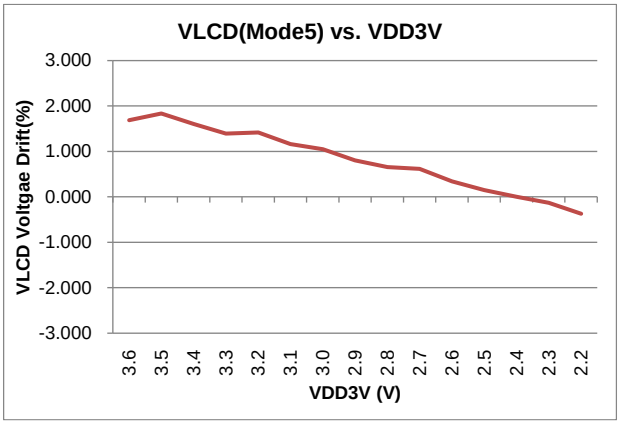


Figure5.12-5 VLCD(Mode5) vs. VDD3V

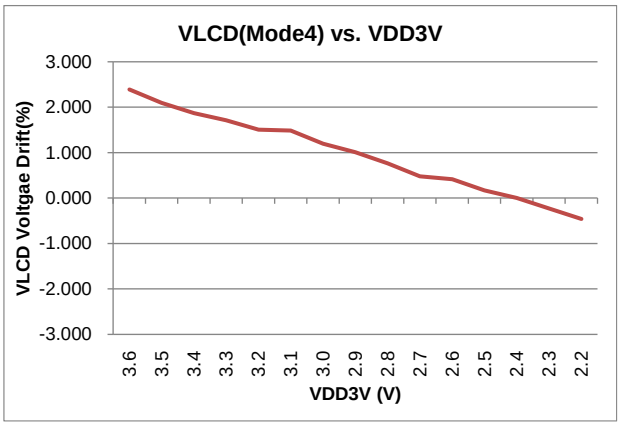


Figure5.12-4 VLCD(Mode4) vs. VDD3V

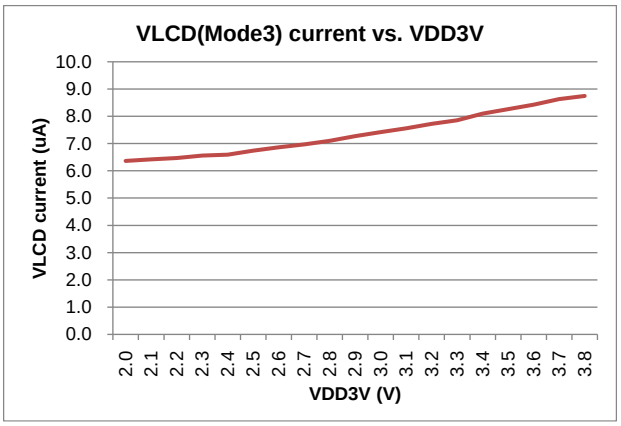


Figure5.12-6 VLCD current vs. VDD3V

6. 訂貨資訊

6.1 HY16F3981 系列選型編碼

下單品名 [1]	封裝型式	引腳數	封裝型式 描述方式		程式碼 編號 [2]	出貨包裝 形式	個裝 數量	材料 組成	MSL[3]
HY16F3981-D000	Die	-	D	000	-	-		Green[4]	-
HY16F3981-L064	LQFP	64	L	064	-	Tray	250	Green[4]	MSL-3
HY16F3981-E028	SSOP	28	E	028	000	Tube	48	Green4	MSL-3
HY16F3981-E028	SSOP	28	E	028	000	Tape & Reel	2000	Green4	MSL-3

[1] 下單品名: 描述的內容為：晶片型號 – 晶片封裝形式

EX：你需求的是 LQFP 64 引腳封裝. 下單品名就是 HY16F3981-L064.

當需要以 Tray 出貨，在下訂單時除下單品名外，請清楚指明出貨包裝形式為 Tray.

[3] MSL:

濕敏度等級符合 IPC/JEDEC J-STD-020 的行業分類工業標準.

產品的加工、包裝、運輸及使用都參考 IPC/JEDEC J-STD-033 行業標準.

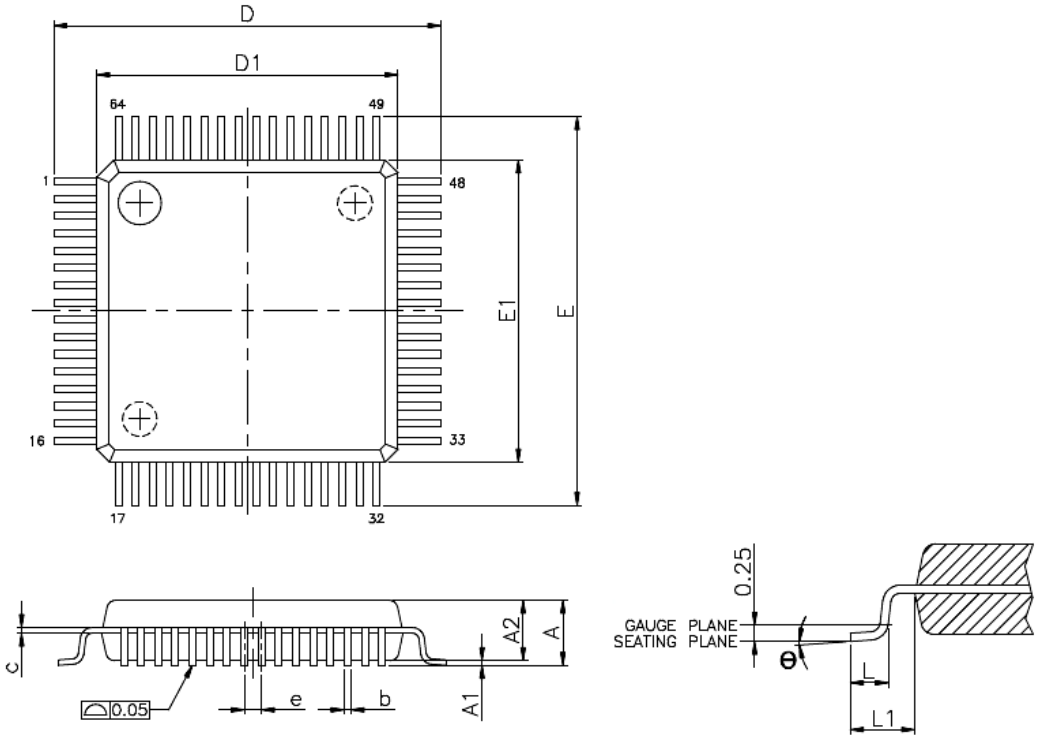
[4] Green (RoHS & no Cl/Br):

HYCON 產品皆為 Green Product，符合 RoHS 指令以及無鹵素規定(Br<900ppm or Cl<900ppm or (Br+Cl)<1500ppm)

7. 封裝尺寸資訊

7.1 LQFP 7x7 64L(L064) 封裝圖

7.1.1 Package Dimensions



VARIATIONS (ALL DIMENSIONS SHOWN IN MM)

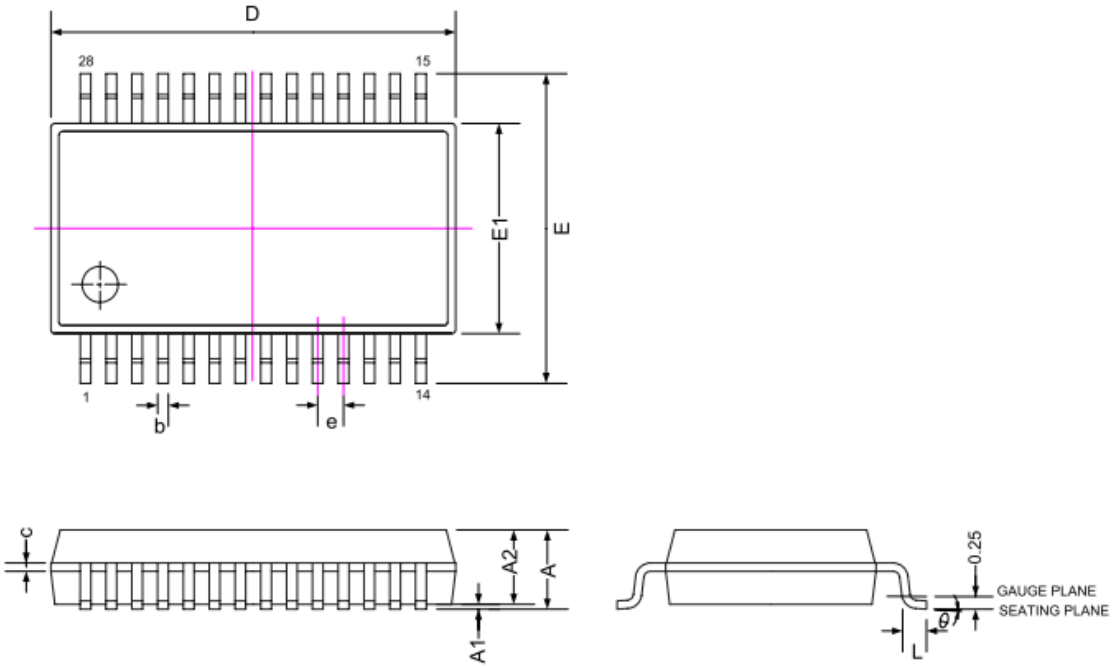
SYMBOLS	MIN.	NOM.	MAX.
A	—	—	1.60
A1	0.05	—	0.15
A2	1.35	1.40	1.45
b	0.13	0.18	0.23
c	0.09	—	0.20
D	9.00 BSC		
D1	7.00 BSC		
e	0.40 BSC		
E	9.00 BSC		
E1	7.00 BSC		
L	0.45	0.60	0.75
L1	1.00 REF		
θ	0°	3.5°	7°

Note:

1. All dimensions refer to JEDEC OUTLINE MS-026.
2. Do not include Mold Flash or Protrusions.
3. Unit: mm.

7.2 SSOP28(209mil) 封裝圖

7.2.1 Package Dimensions



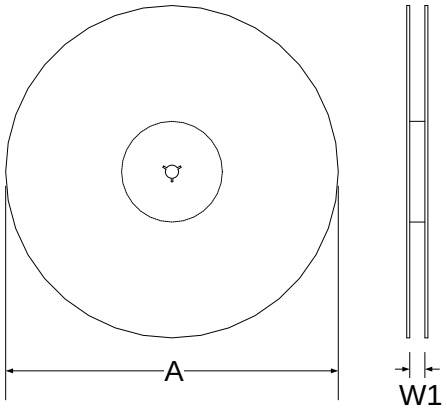
SYMBOLS	MIN	NOM	MAX
A	-	-	2.00
A1	0.05	-	-
A2	1.65	1.75	1.85
b	0.22	-	0.38
c	0.09	-	0.25
D	10.05	10.20	10.50
E1	5.00	5.30	5.60
E	7.65	7.80	7.90
L	0.55	0.75	0.95
e	0.65 BASIC		
θ°	0	4	8

Note:

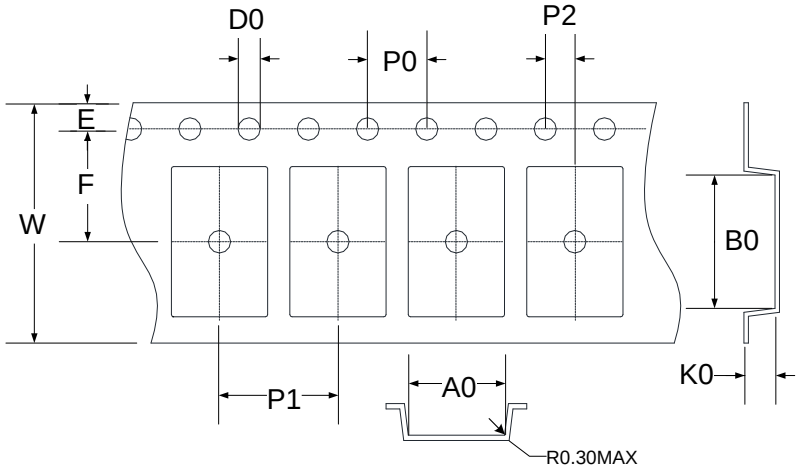
1. All dimensions refer to JEDEC OUTLINE MO-150.
2. Do not include Mold Flash or Protrusions.
3. Unit: mm.

7.2.2 Tape & Reel Information

7.2.2.1 Reel Dimensions



7.2.2.2 Carrier Tape Dimensions

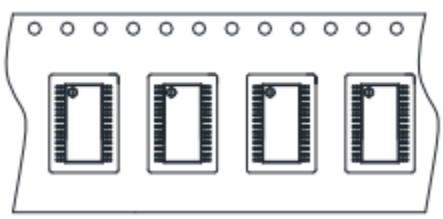


SYMBOLS	Reel Dimensions		Carrier Tape Dimensions									
	A	W1	A0	B0	K0	P0	P1	P2	E	F	D0	W
Spec.	330	24.5	8.40	10.65	2.40	4.00	12.00	2.00	1.75	11.50	1.50	24.00
Tolerance	+6/-3	+1.5/-0	±0.10	±0.10	±0.10	±0.10	±0.10	±0.10	±0.10	±0.10	+0.1/-0	±0.30

Unit: mm

Note: 10 Sprocket hole pitch cumulative tolerance is ±0.20mm.

7.2.2.3 Pin1 direction



8. 修改記錄

以下描述本文件差異較大的地方，而標點符號與字形的改變不在此描述範圍。

版本	頁數	變更摘要
V01	All	初版發行
V02	P12	E028, PIN7 為 PT7.2
	P37~P38	新增圖表 Sleep / Idle / HAO Free Run(2M/4M/10M/16M) Current vs. VDD3V
	P50	新增圖表 V12 vs. VDD3V
	P51	新增圖表 VLCD Current vs. VDD3V
V03	All	新增各圖表以及更新電器規格
V05	All	1.移除 PT3.2/PT3.3 腳位的 GPIO 複用功能，該腳位只保留 AIO4/AIO5 類比功能. 2.修改 5.5 章節 RPU 參數規格(並且增加上下限) 3.新增 5.9 章節 RLADDER 參數規格(上下限) 4.修改 12-bit Resistance Ladder 網路圖與增加電器規格說明 5.修正 ADC 網路圖(ADCLK 更名為 ADCK) 6.修正 ADC ENOB(RMS)與 RMS noise Table 表
V06	All	1. 新增 SSOP28 無支援 LCD 功能的紅外線傳感器與血壓計傳感器應用參考線路 2. 移除硬體 I2C 功能描述，硬體 I2C 功能不開放使用
V07	All	1. 新增說明 Flash 閃存特性 2. 新增說明 VLCD 可透過效正函數提供 5 段 VLCD 偏壓 3. 新增說明 VDDA Voltage 1~4 的暫存控制說明 4. 修正應用電路圖，連接外部 EEPROM 的引腳只需要連接外部上拉電阻,不需要接 GND. 5. 修正 IR 應用電路, Thermistor 線路, Rf 參考電阻為 100k, 分壓電阻為 300k, REFO 新增設計可切換 Switch 開關短路到 AI1. 6. 修正 LVD 方塊圖，並且修正 LVDS 電器規格描述. 7. 新增 PT3.2/PT3.3 腳位的 GPIO 複用功能，該腳位可以工作於數位與類比複用功能. 8. 新增硬體 I2C 功能

		9. 新增 Note1 在 ADC 電器特性章節, 說明 ADC 差動輸入範圍限制. 10. Timer B 方塊圖的 TBCLK 修正為 TBCK, TMBC0/TMBC1/TMBC2 修正為 TBC0/TBC1/TBC2, ENTMB 修正為 TBEN. 11. Timer B2 方塊圖的 TBCLK 修正為 TB2CK, TMB2C0/TMB2C1/TMB2C2 修正為 TB2C0/TB2C1/TB2C2, ENTMB2 修正為 TB2EN. 12. Timer C 方塊圖的 ENTMC 修改為 TCEN.