HY15P43
Datasheet

8-Bit RISC-like Mixed Signal Microcontroller
Embedded 8x8 LED Driver
18-Bit ΣΔADC

Table of Contents

注意：

1、 本說明書中的內容，隨著產品的改進，有可能不經過預告而更改。請客戶及時到本公司網站下載更新 http://www.hycontek.com。

2、 本規格書中的圖形、應用電路等，因第三方工業所有權引發的問題，本公司不承擔其責任。

3、 本產品在單獨應用的情況下，本公司保證它的性能、典型應用和功能符合說明書中的條件。當使用在客戶的產品或設備中，以上條件我們不作保證，建議客戶做充分的評估和測試。

4、 請注意輸入電壓、輸出電壓、負載電流的使用條件，使 IC 內的功耗不超過封裝的容許功耗。對於客戶在超出說明書中規定額定值使用產品，即使是瞬間的使用，由此所造成的損失，本公司不承擔任何責任。

5、 本產品雖內置防靜電保護電路，但請不要施加超過保護電路性能的過大靜電。

6、 本規格書中的產品，未經書面許可，不可使用在要求高可靠性的電路中。例如健康醫療器械、防災器械、車輛器械、車載器械及航空器械等對人體產生影響的器械或裝置，不得作為其部件使用。

7、 本公司一直致力於提高產品的品質和可靠度，但所有的半導體產品都有一定的失效概率，這些失效概率可能會導致一些人身事故、火災事故等。當設計產品時，請充分留意冗餘設計並採用安全指標，這樣可以避免事故的發生。

8、 本規格書中內容，未經本公司許可，嚴禁用於其他目的之轉載或複製。

1. 特點

- 8 位元 H08A 加強型精簡指令集，共有 66 個指令包含硬體乘法指令及查表指令
- 2.2V to 5.5V 工作電壓範圍，-40~85℃工作溫度範圍.
- 支援外部石英震盪器 1MHZ~4MHZ/32768HZ 及內部高精度 RC 震盪器 2MHZ/4MHZ，多種 CPU 工作時脈切換選擇，可讓使用者達到最佳省電規劃
  - 運行模式
  - 待機模式
  - 休眠模式
- 5KWord OTP Type 程式記憶體，128Byte 資料記憶體
- Brownout detector及Watch dog Timer，可防止CPU進入死機模式.
- 8 個七段顯示驅動器
  - 支援LED顯示控制寄存器
  - 共陰極或是共陽極驅動支援
  - 單一位元設定可以閃爍字節顯示
  - 12 個LED埠可設定為數位輸出埠
  - 支援Non-Overlap掃描方式
- 18bit 全差動輸入ΣΔADC 類比數位轉換器
  - 內置PGA (Programmable Gain Amplifier) 可有 128 倍輸入信號放大倍率選擇
  - 內置輸入零點調整，可針對不同應用增加其量測範圍
  - 可選擇不同的數據輸出速率，最高可達 15.6ksps
  - 內置絕對溫度感測器
- LVD 低電壓檢測功能具 14 段檢測電壓設置與外部輸入電壓檢測功能
- 類比電壓源VDDA具 10mA穩壓電壓源輸出能力，快速啟動功能，可提供傳感器驅動電壓
- 8-bit Timer A
- 16-bit Timer B模組具Compare/PWM功能
- 串列通訊EUART，SPI，I2C模組
- Built-In EPROM (BIE)，內建 2.75V低壓燒錄控制電路
- Support 6 stack level.

2. 引腳定義

2.1. LQFP 7x7 48L 引腳圖

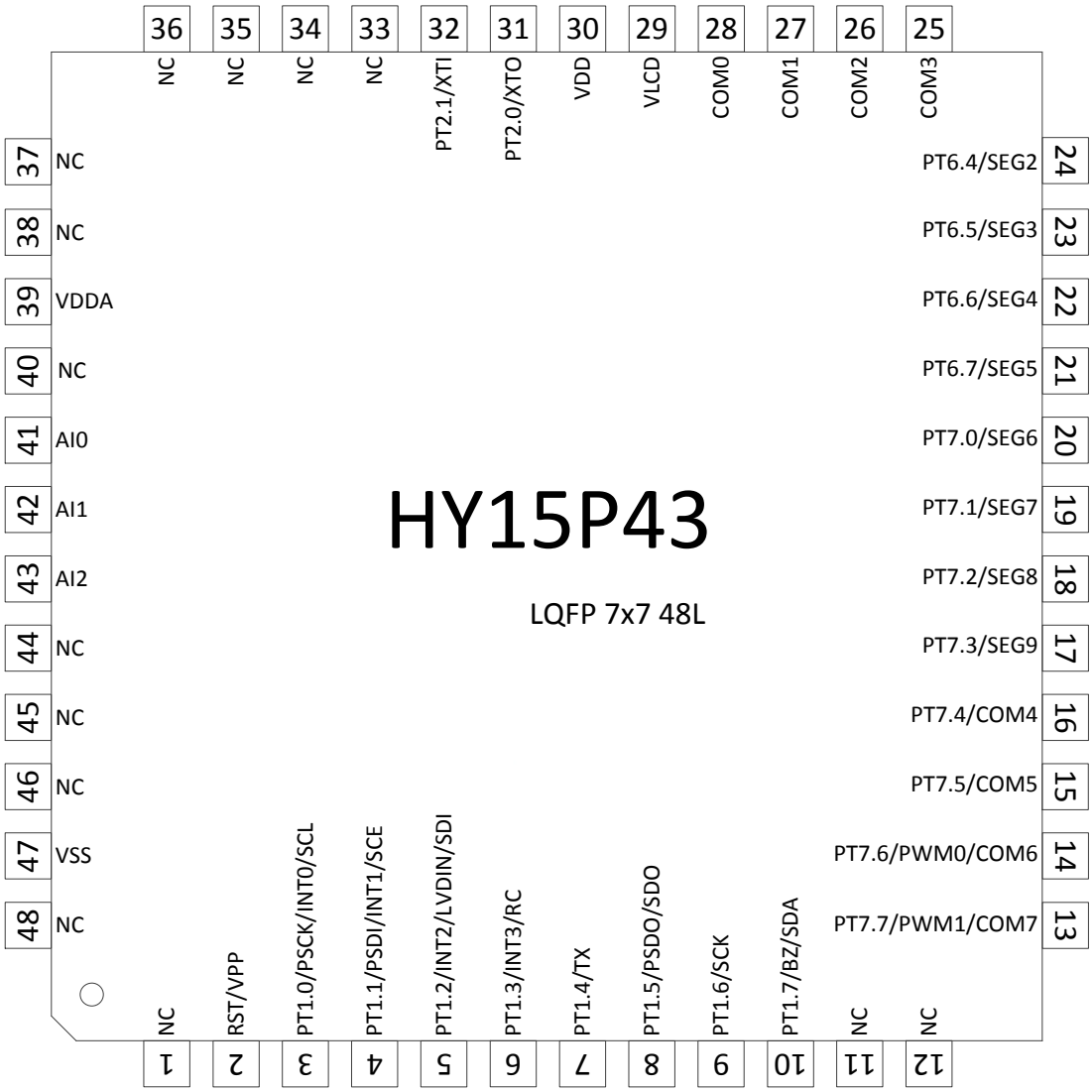


圖 2-1 HY15P43 LQFP 7x7 48L 引腳圖

2.2. TSSOP28 引腳圖

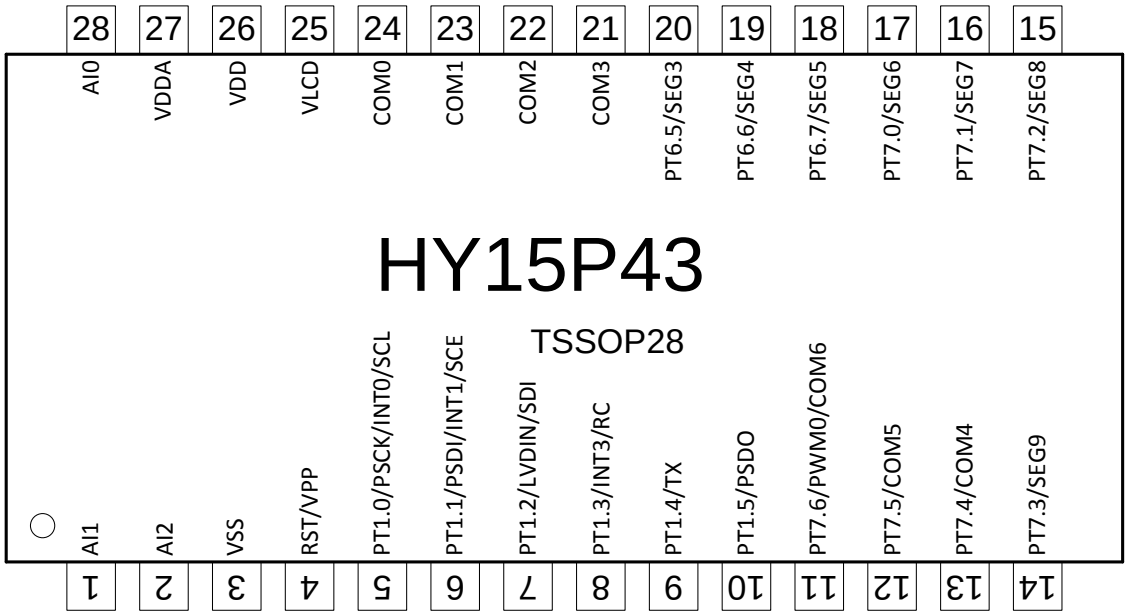


圖 2-2 HY15P43 TSSOP28 引腳圖

註 1：VPP與RST復用同一接口，非燒錄OTP時禁止輸入高電壓

2.3. I/O 定義與說明

"I/O"輸入/輸出,"I"輸入,"O"輸出,"S"史密斯觸發,"C"CMOS 特性兼容輸出與輸入,"P"電壓源,"A"類比通道

LQFP48 引腳編號	TSSOP28 引腳編號	引腳名稱	引腳特性		功能說明
			格式	緩衝	
2	4	RST/VPP			
		RST	I	S	復位晶片
		VPP	P	P	OTP讀/寫時的電壓源
3	5	PT1.0/INT0/PSCK/SCL			
		PT1.0	I/O	S	數位輸入/輸出
		INT0	I	S	中斷源INT0
		PSCK	I	S	OTP讀/寫介面接口
		SCL	I/O	S	I2C 通訊介面引腳
4	6	PT1.1/INT1/PSDI/SCE			
		PT1.1	I/O	S	數位輸入/輸出
		INT1	I	S	中斷源INT1
		PSDI	I	S	OTP讀/寫介面接口
		SCE	I/O	S	SPI 通訊介面接口
5	7	PT1.2/INT2/LVDIN/SDI			
		PT1.2	I/O	S	數位輸入
		INT2	I	S	中斷源INT2
		LVDIN	A	A	LVD外部信號輸入接口
		SDI	I/O	S	SPI通訊介面接口
6	8	PT1.3/INT3/RC			
		PT1.3	I/O	S	數位輸入
		INT3	I	S	中斷源INT3
		RC	I	S	EUART通訊介面接口
7	9	PT1.4/TX			
		PT1.4	I/O	S	數位輸入/輸出
		TX	O	S	EUART通訊介面接口
8	10	PT1.5/PSDO/SDO			
		PT1.5	I/O	S	數位輸入/輸出
		PSDO	O	C	OTP讀/寫介面接口
		SDO	I/O	S	SPI 通訊介面接口
9	-	PT1.6/SCK			
		PT1.6	I/O	S	數位輸入/輸出
		SCK	I/O	S	SPI通訊介面接口
10	-	PT1.7/BZ/SDA			
		PT1.7	I/O	S	數位輸入/輸出

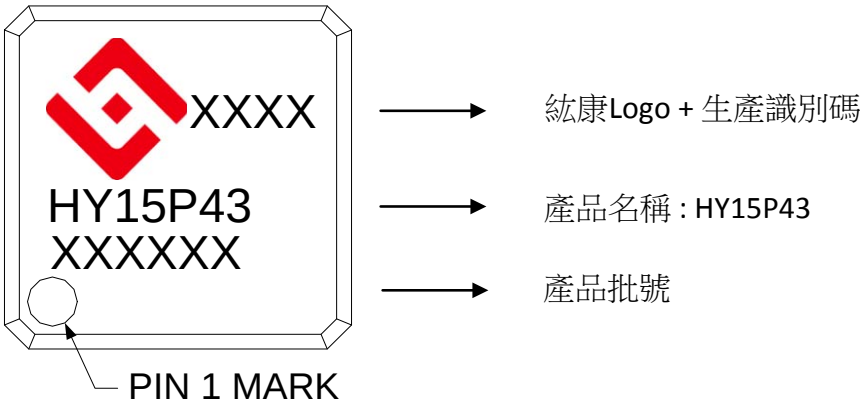
		BZ	O	C	蜂鳴器輸出端
		SDA	I/O	S	I2C 通訊介面引腳
13	-	PT7.7/PWM1/COM7			
		PT7.7	O	S	數位輸出
		PWM1	O	C	PWM1 輸出接口
		COM7	O	C	LED COM 輸出
14	11	PT7.6/PWM0/COM6			
		PT7.6	O	S	數位輸出
		PWM0	O	C	PWM0 輸出接口
		COM6	O	C	LED COM 輸出
15	12	PT7.5/COM5			
		PT7.5	O	S	數位輸出
		COM5	O	C	LED COM 輸出
16	13	PT7.4/COM4			
		PT7.4	O	S	數位輸出
		COM4	O	C	LED COM 輸出
17	14	SEG9/PT7.3			
		SEG9	O	A	LED Segment輸出
		PT7.3	O	S	數位輸出
18	15	SEG8/PT7.2			
		SEG8	O	A	LED Segment輸出
		PT7.2	O	S	數位輸出
19	16	SEG7/PT7.1			
		SEG7	O	A	LED Segment輸出
		PT7.1	O	S	數位輸出
20	17	SEG6/PT7.0			
		SEG6	O	A	LED Segment輸出
		PT7.0	O	S	數位輸出
21	18	SEG5/PT6.7			
		SEG5	O	A	LED Segment輸出
		PT6.7	O	S	數位輸出
22	19	SEG4/PT6.6			
		SEG4	O	A	LED Segment輸出
		PT6.6	O	S	數位輸出
23	20	SEG3/PT6.5			
		SEG3	O	A	LED Segment輸出
		PT6.5	O	S	數位輸出
24	-	SEG2/PT6.4			

		SEG2 PT6.4	O O	A S	LED Segment輸出 數位輸出
25	21	COM3	O	A	LED COM輸出
26	22	COM2	O	A	LED COM輸出
27	23	COM1	O	A	LED COM輸出
28	24	COM0	O	A	LED COM輸出
29	25	VLCD	P	P	BIE電壓源
30	26	VDD	P	P	晶片工作電壓源
31	-	PT2.0/XTO PT2.0 XTO	 I/O A	 S A	 數位輸入/輸出 外接振盪器輸出端
32	-	PT2.1/XTI PT2.1 XTI	 I/O A	 S A	 數位輸入/輸出 外接振盪器輸入端
39	27	VDDA	P	P	穩壓器輸出，類比電路電壓源
41	28	AI0	A	A	類比輸入通道
42	1	AI1	A	A	類比輸入通道
43	2	AI2	A	A	類比輸入通道
47	3	VSS	P	P	晶片工作電壓源接地端
Others	Others	NC	-	-	未使用

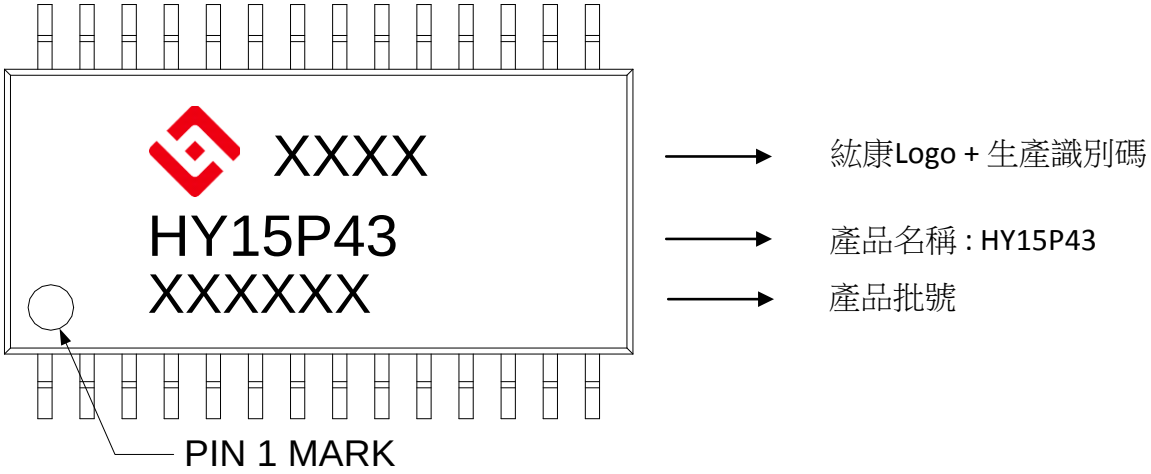
表 2-1 引腳定義與功能說明

2.4. 封裝片標記信息

2.4.1. LQFP 封裝片標記信息



2.4.2. TSSOP28 封裝片標記信息



3. 應用電路

3.1. 橋式感測器 LED 顯示

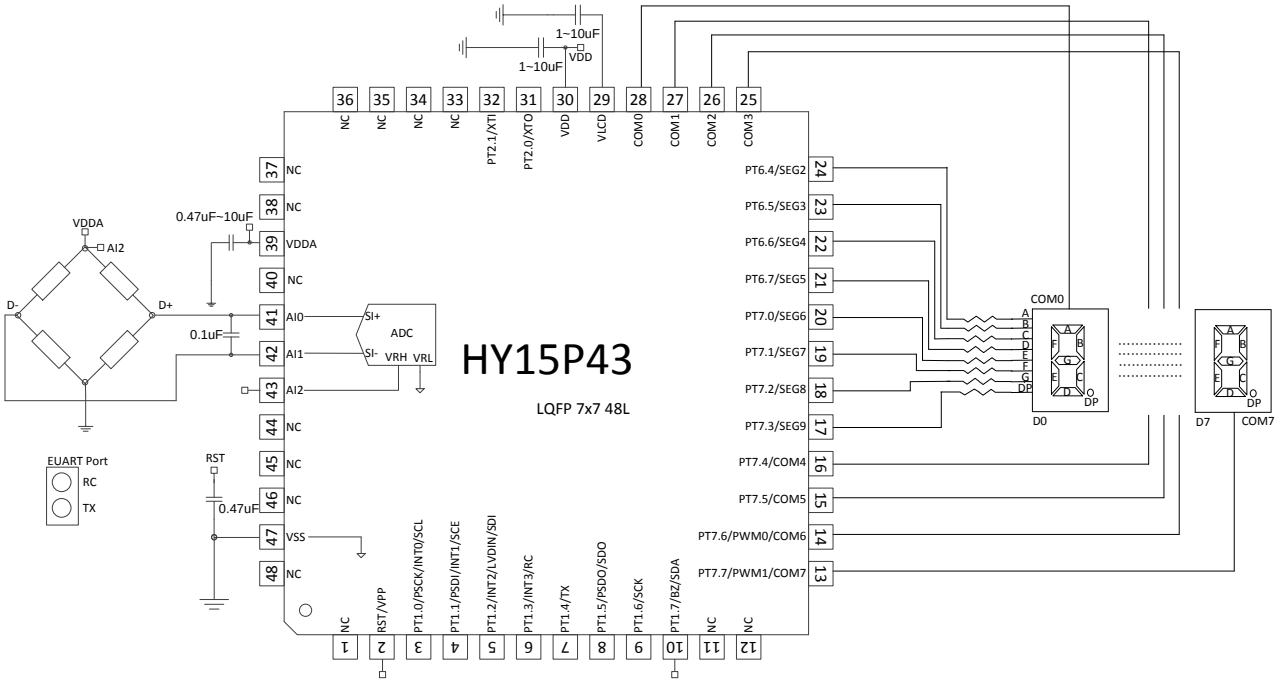


圖 3-1 橋式感測器 LED 顯示應用電路

4. 功能概述

4.1. 內部方塊圖

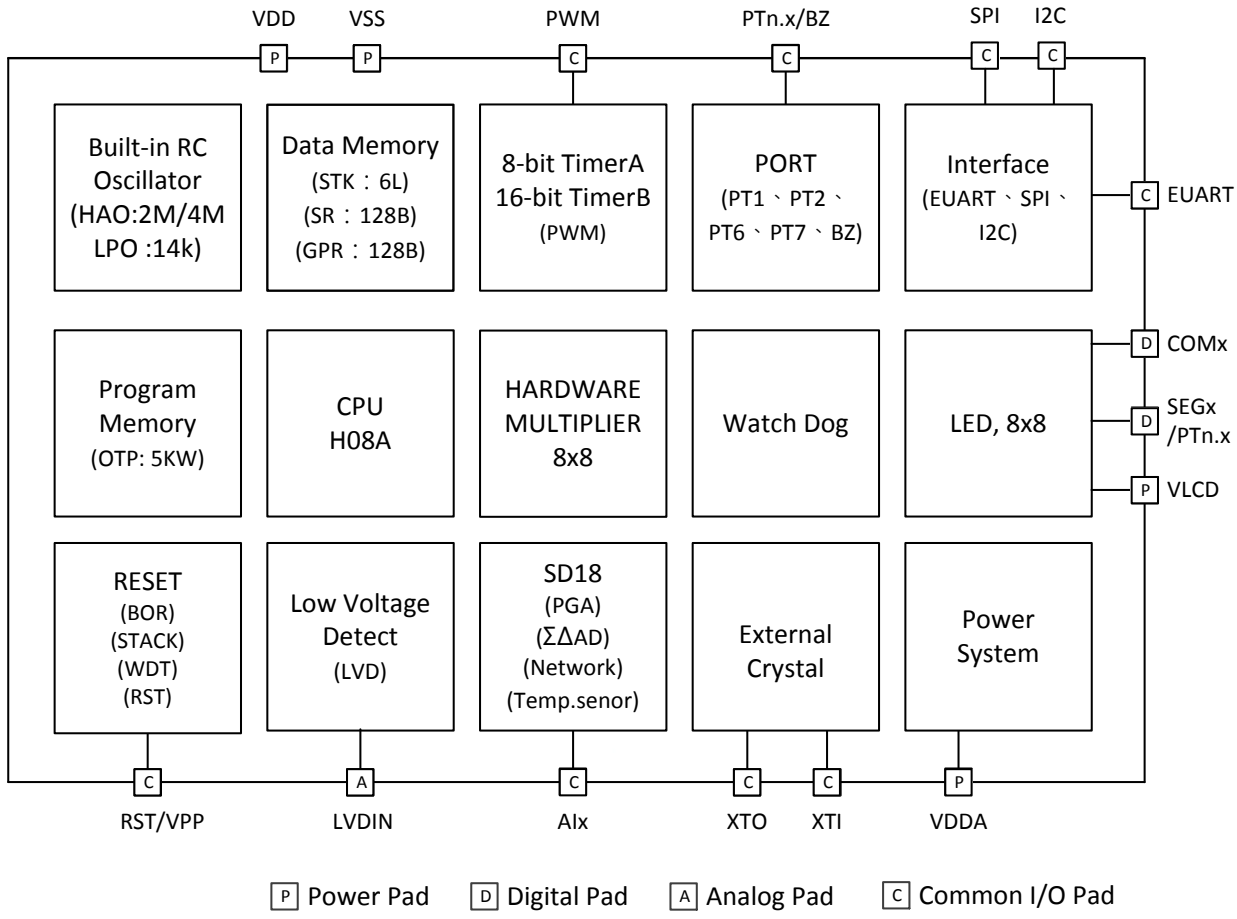


圖 4-1 HY15P43 內部方塊圖

4.2. 相關說明與支援文件

晶片功能相關使用說明書

DS-HY15P43	HY15P43 說明書
UG-HY15S50	HY15S50 使用說明書
APD-CORE002	H08A 指令集說明書

開發工具相關使用說明書

APD-HY15PIDE001	HY15P 系列開發工具軟體使用說明書
APD-HY15PIDE002	HY15P 系列開發工具硬體使用說明書
APD-OTP001	OTP 燒錄引腳資訊

產品生產相關使用說明書

APD-HY15PIDE004	HY15P 系列生產線專用燒錄器說明書
BDI-HY15P43	HY15P43 個別產品的裸片打線資訊

4.3. Clock System

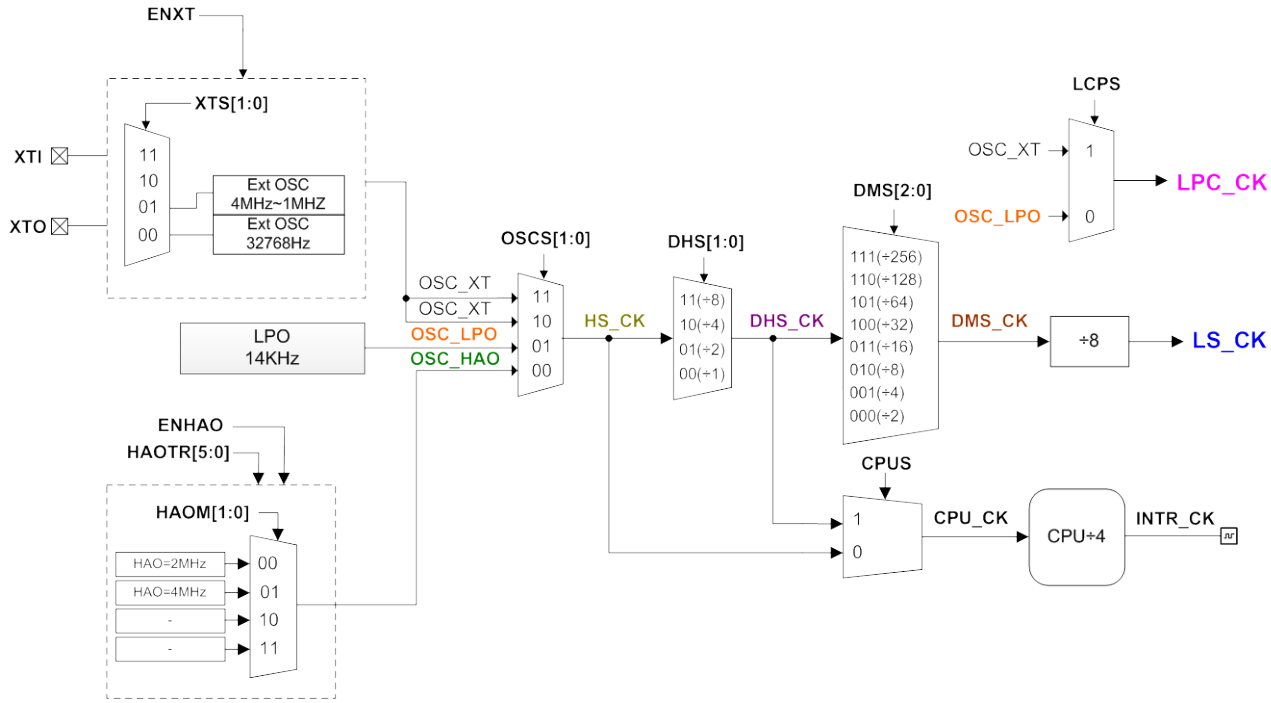


圖 4-2 Clock System 方塊圖(一)

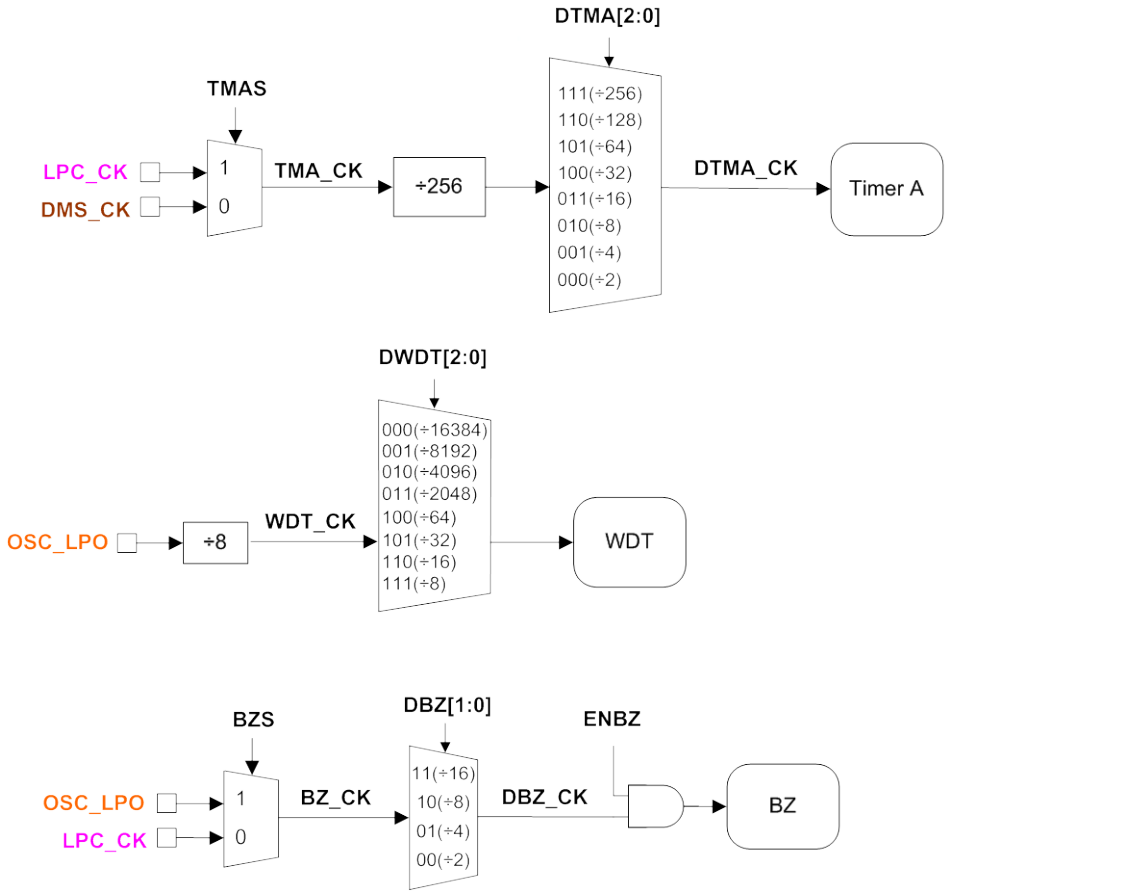


圖 4-3 Clock System 方塊圖(二)

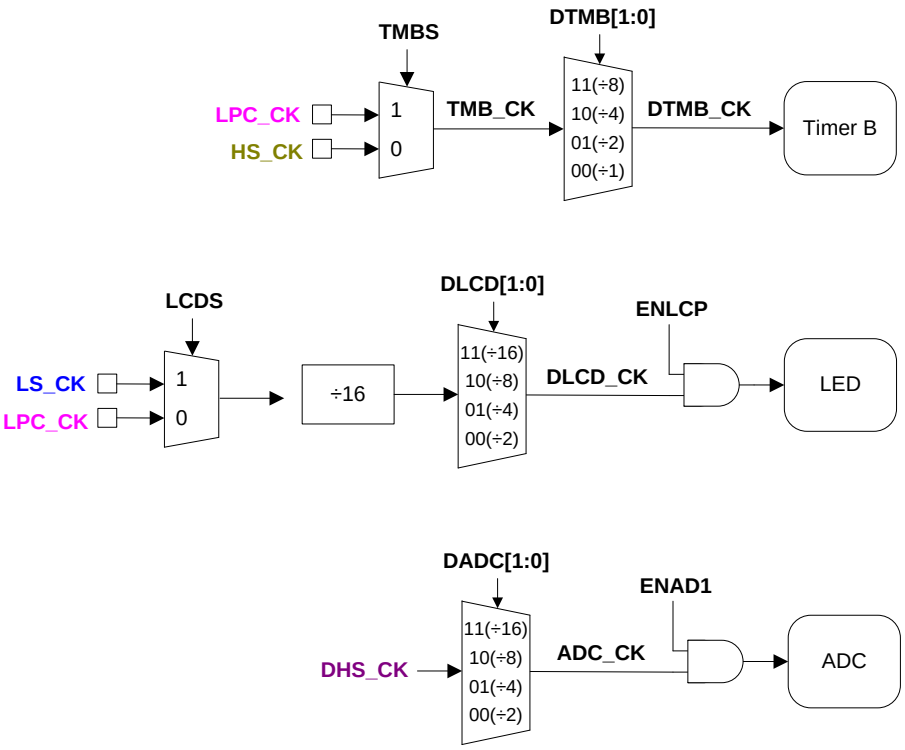


圖 4-4 Clock System 方塊圖(三)

4.4. Low Voltage Detect(LVD)

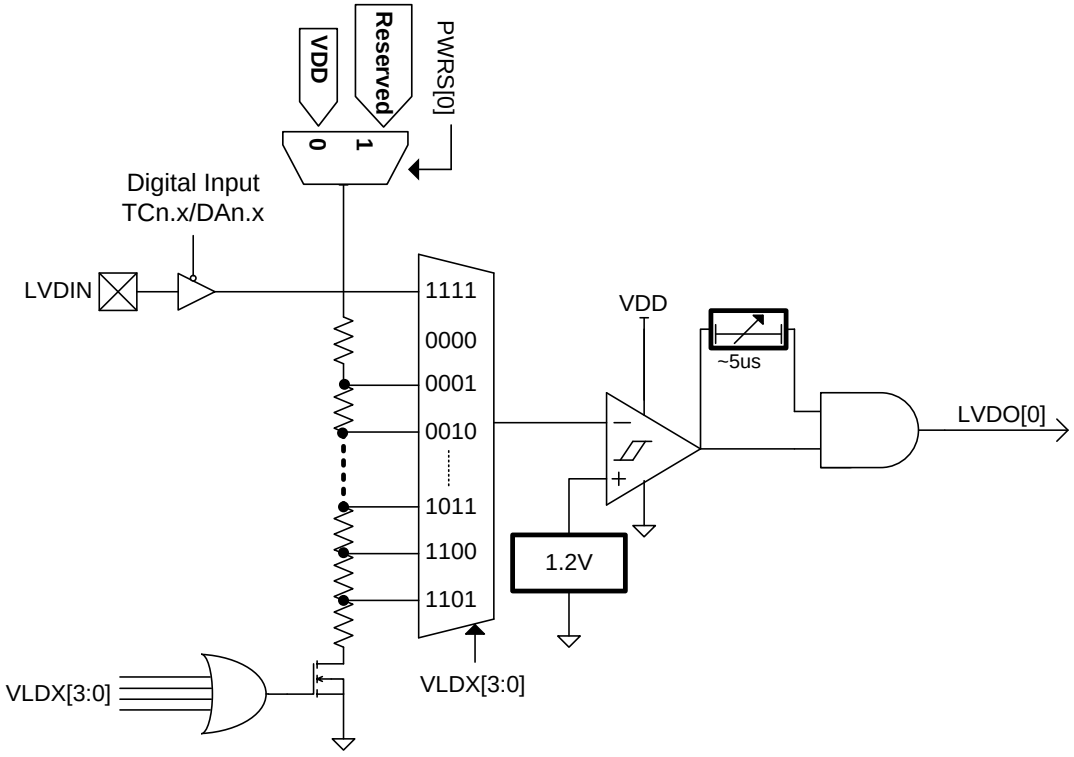


圖 4-5 Low Voltage Detect 方塊圖

4.5. Reset

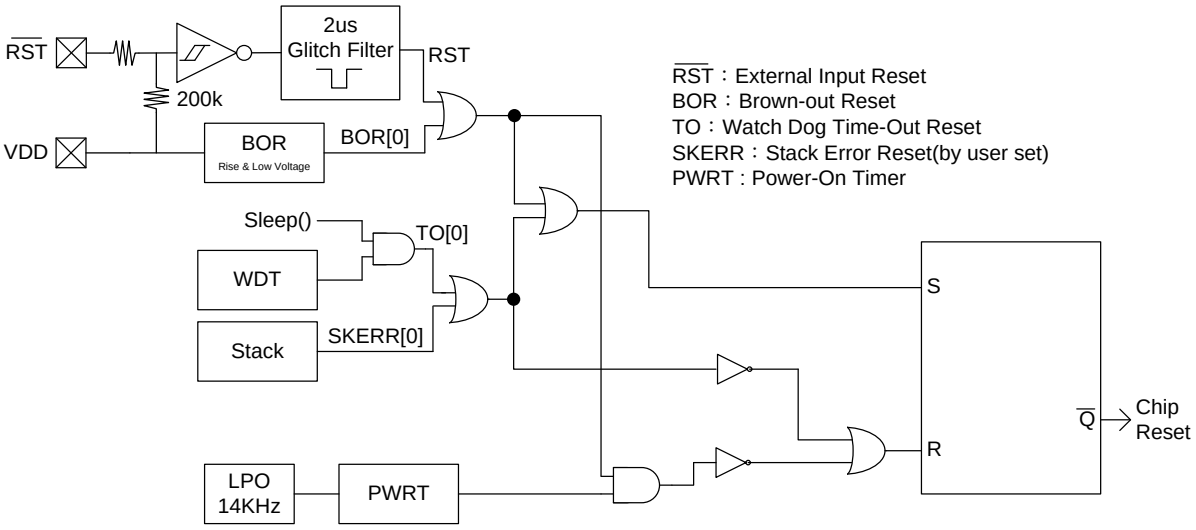


圖 4-6 Reset 方塊圖

4.6. Power System

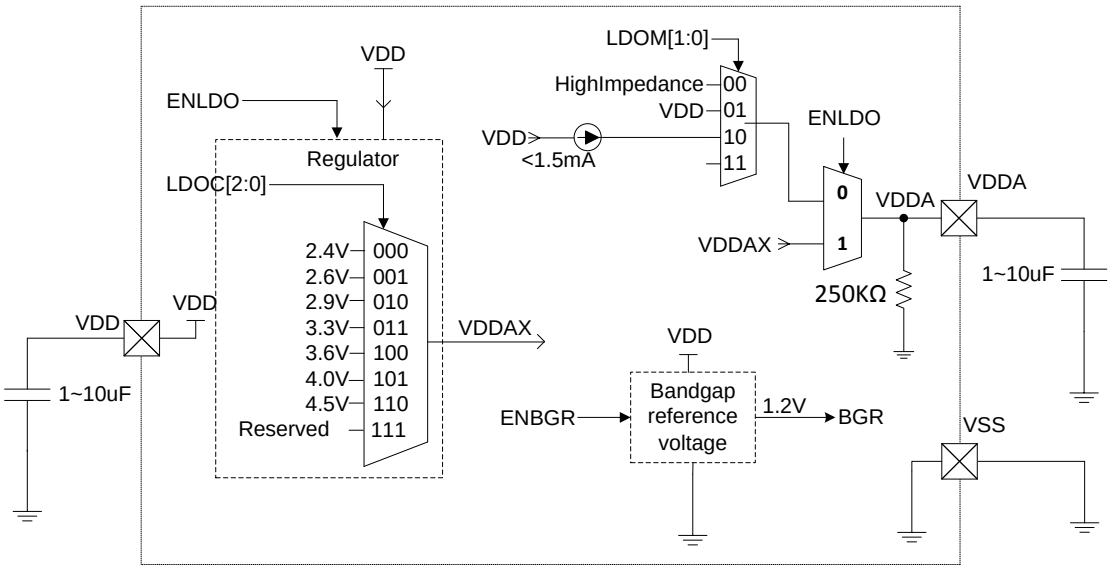


圖 4-7 Power System 方塊圖

4.7. SD18 Network

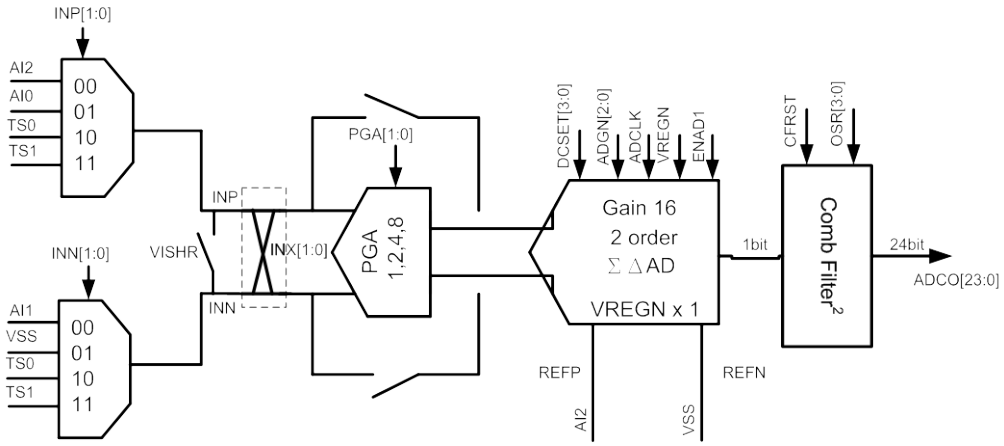


圖 4-8 SD18 Network 方塊圖

4.8. GPIO

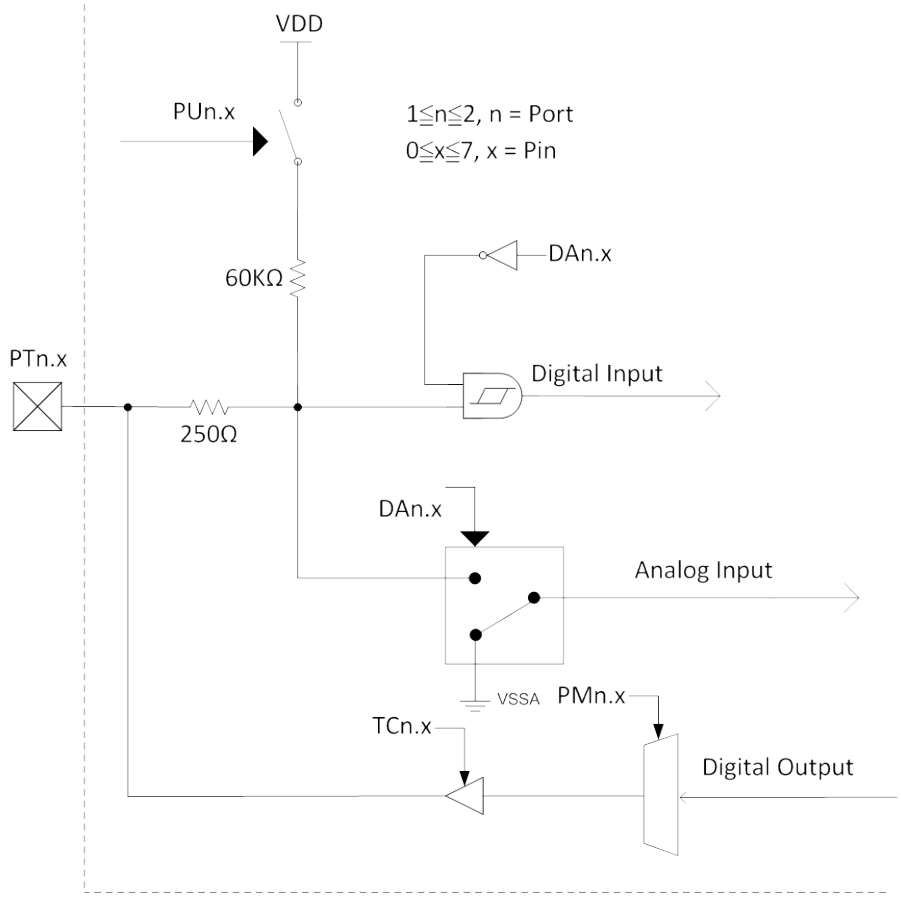


圖 4-9 GPIO 方塊圖

4.9. Watch Dog

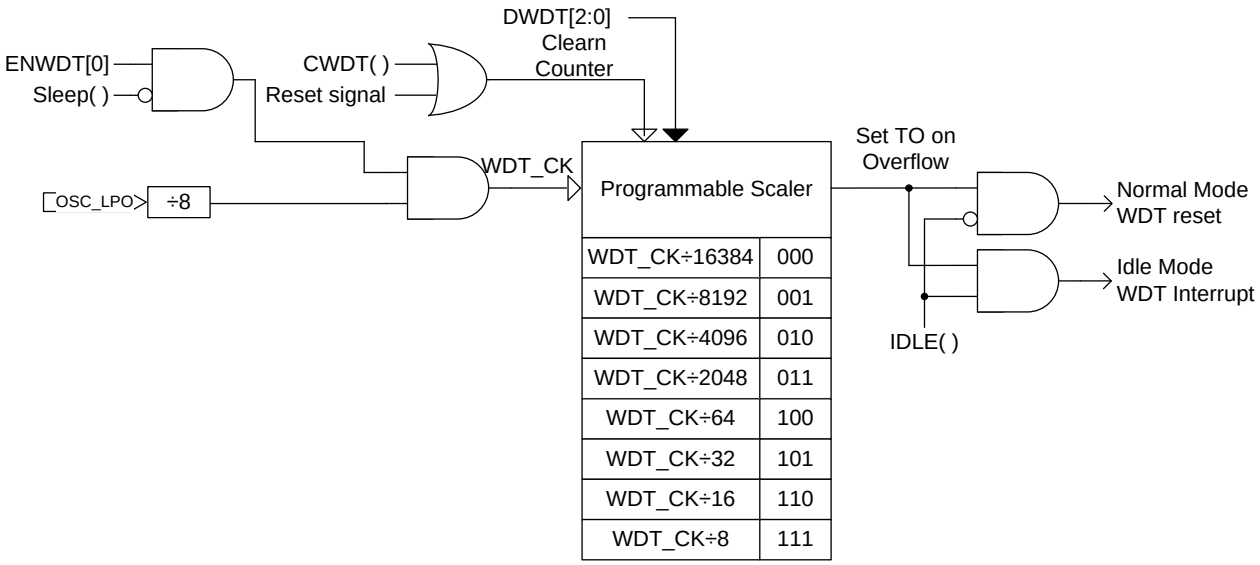


圖 4-10 Watch Dog 方塊圖

4.10. 8-bit Timer A

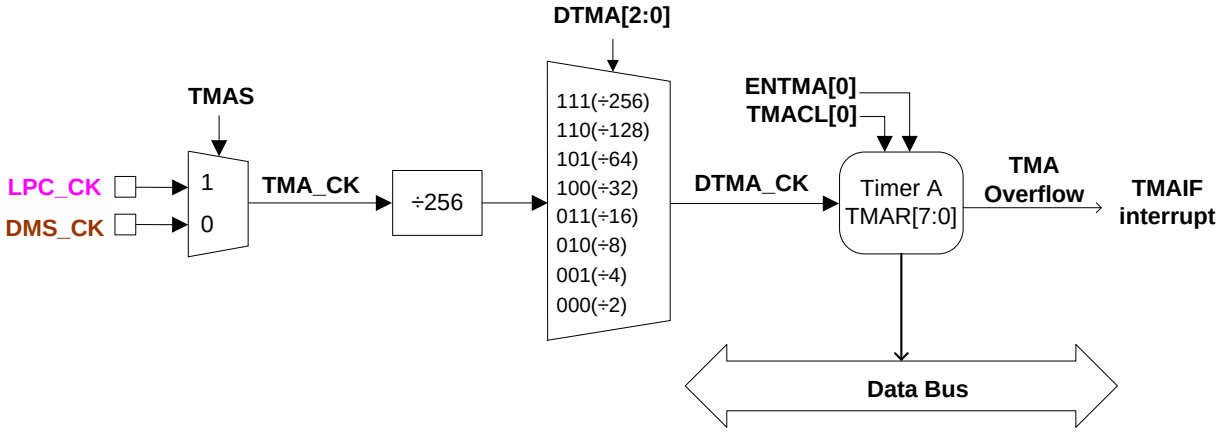


圖 4-11 8-bit Timer A 方塊圖

4.11. 16-bit Timer B

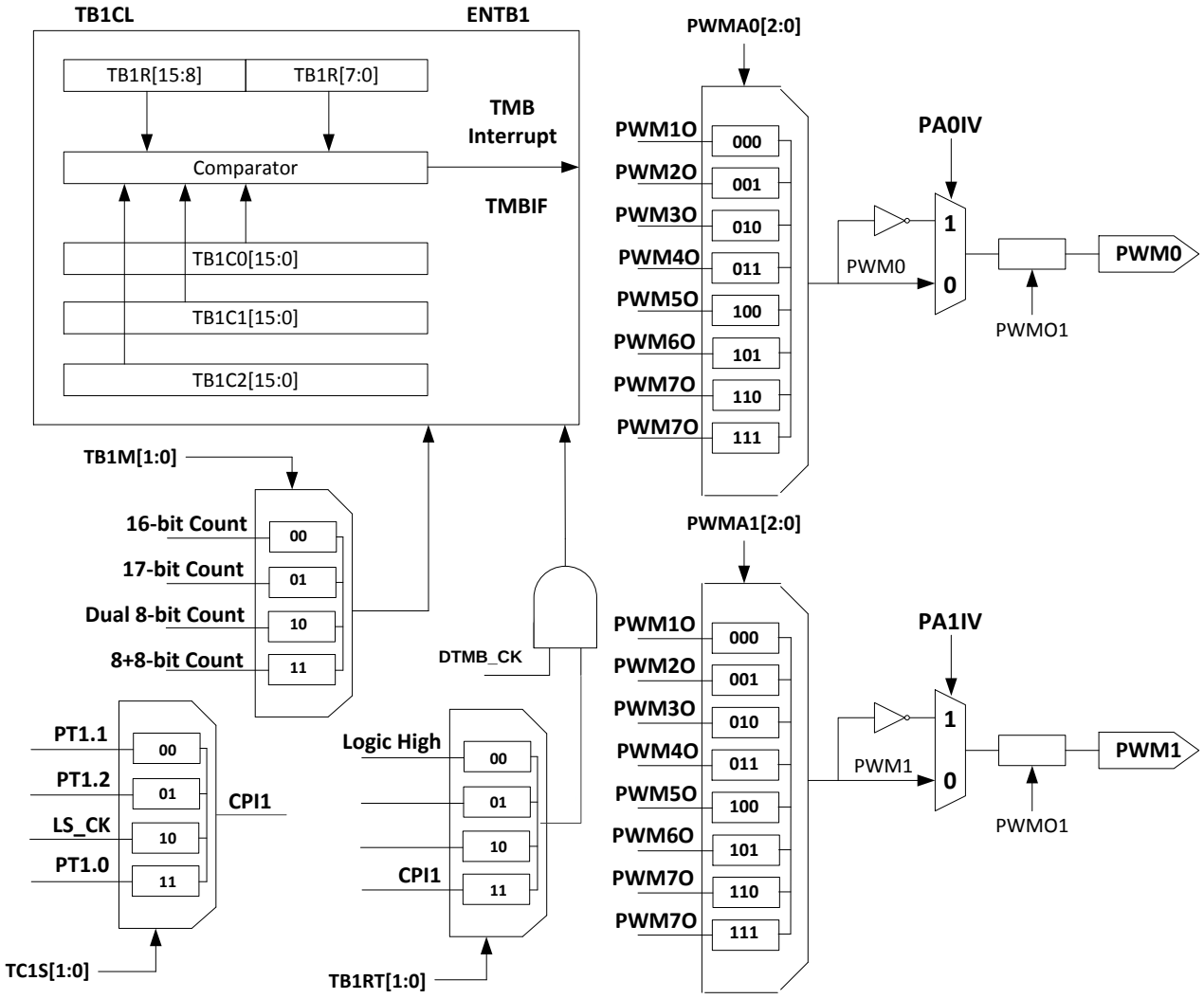


圖 4-12 16-bit Timer B 方塊圖

4.12. LED

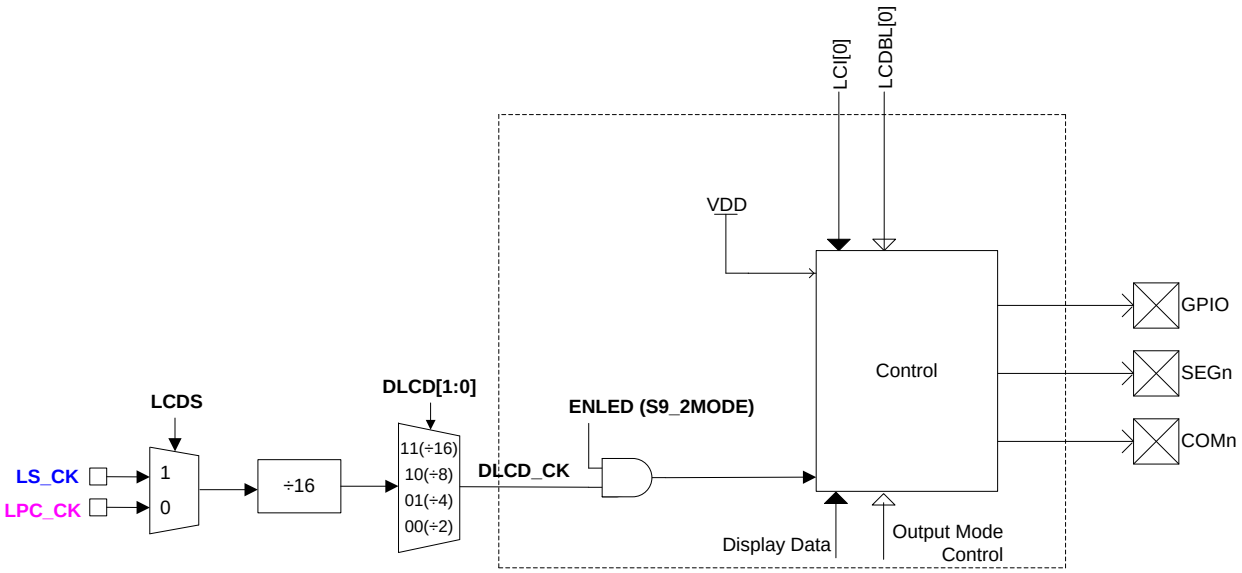


圖 4-13 LED 方塊圖

4.13. EUART

EUART TRANSMIT BLOCK DIAGRAM

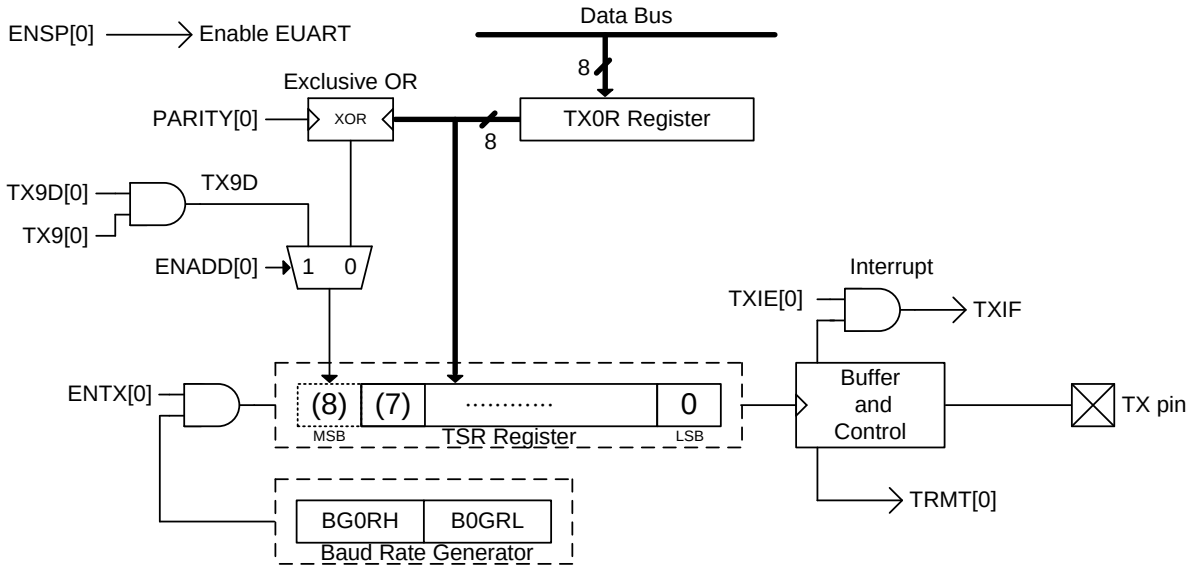
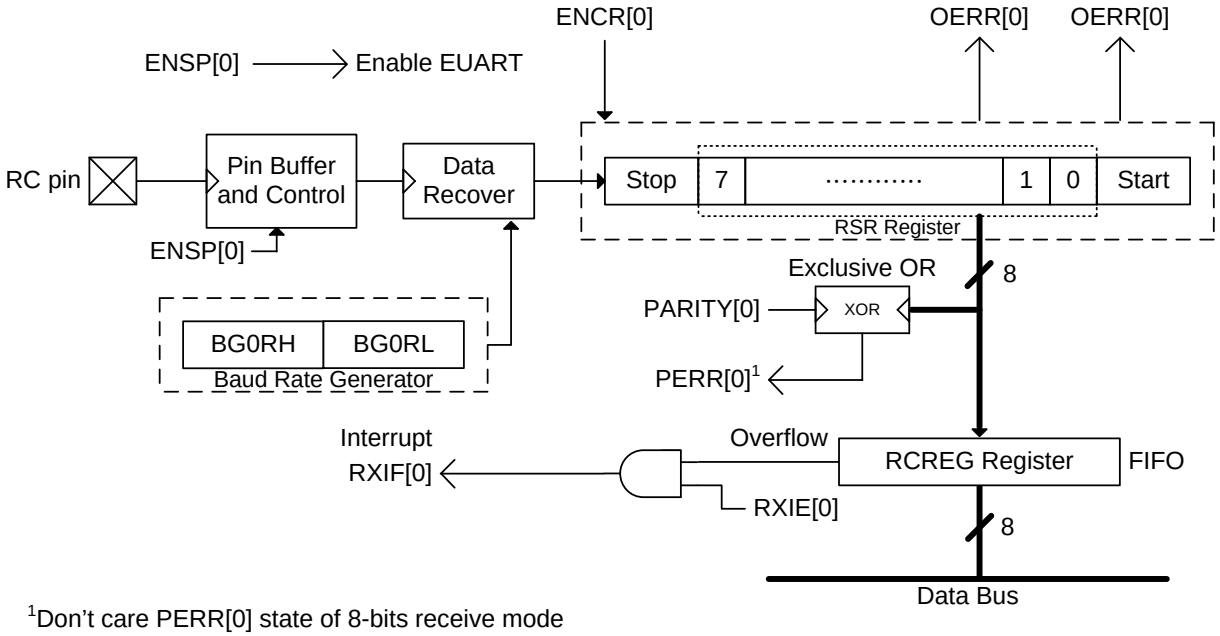


圖 4-14 EUART 傳送方塊圖

EUART 8-BITs RECEIVE BLOCK DIAGRAM



[1]Don't care PERR[0] state of 8-bits receive mode

圖 4-15 EUART 8-bits 接收方塊圖

4.14. SPI

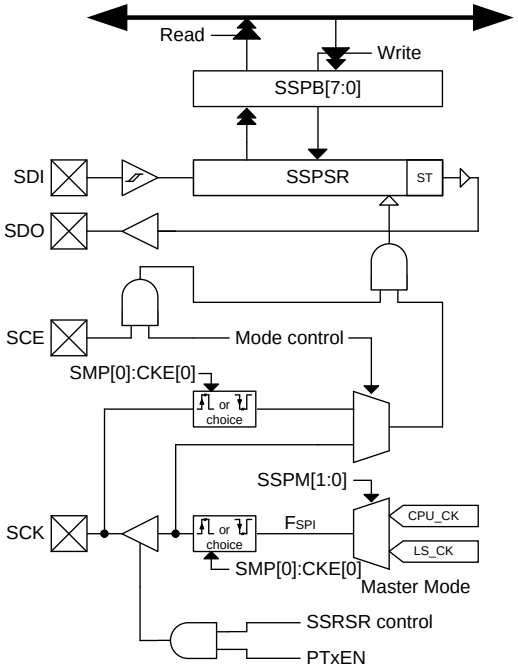


圖 4-16 SPI 方塊圖

4.15. I2C

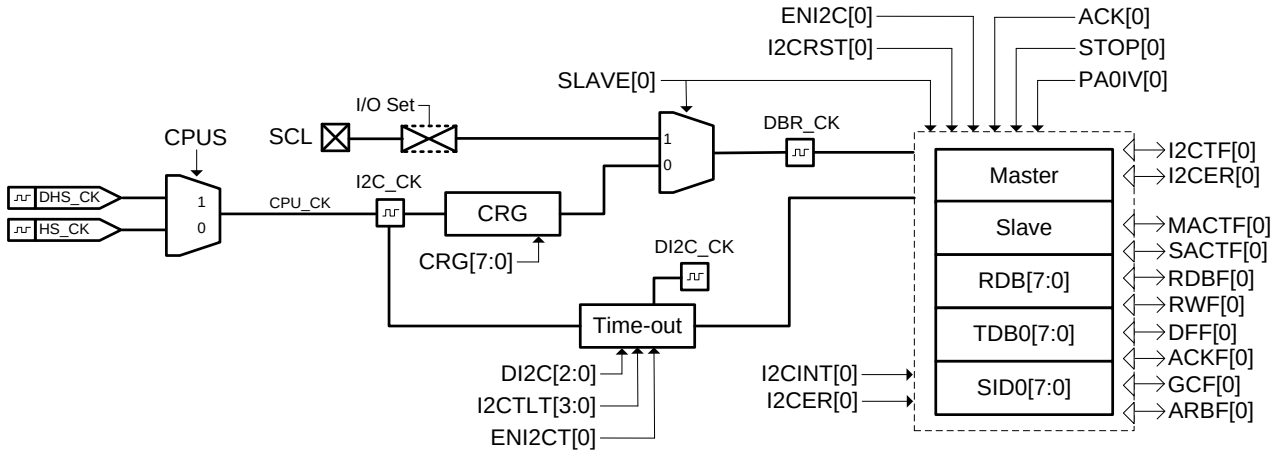


圖 4-17 I2C 方塊圖

5. 暫存器列表

"-"no use,"*"read/write,"w"write,"r"read,"r0"only read 0,"r1"only read 1,"w0"only write 0,"w1"only write 1
"$"for event status,"."unimplemented bit,"x"unknown,"u"unchanged,"d"depends on condition

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	ARST	IRST	R/W
000h	INDF0	Contents of FSR0 to address data memoryvalue of FSR0 not changed								xxxx xxxx	uuuu uuuu	*,*,*,*,*,*,*,*
001h	POINC0	Contents of FSR0 to address data memoryvalue of FSR0 post-incremented								xxxx xxxx	uuuu uuuu	*,*,*,*,*,*,*,*
002h	PODEC0	Contents of FSR0 to address data memoryvalue of FSR0 post-decremented								xxxx xxxx	uuuu uuuu	*,*,*,*,*,*,*,*
003h	PRINC0	Contents of FSR0 to address data memoryvalue of FSR0 pre-incremented								xxxx xxxx	uuuu uuuu	*,*,*,*,*,*,*,*
004h	PLUSW0	Contents of FSR0 to address data memoryvalue of FSR0 offset by W								xxxx xxxx	uuuu uuuu	*,*,*,*,*,*,*,*
005h	INDF1	Contents of FSR1 to address data memoryvalue of FSR0 not changed								xxxx xxxx	uuuu uuuu	*,*,*,*,*,*,*,*
006h	POINC1	Contents of FSR1 to address data memoryvalue of FSR0 post-incremented								xxxx xxxx	uuuu uuuu	*,*,*,*,*,*,*,*
007h	PODEC1	Contents of FSR1 to address data memoryvalue of FSR0 post-decremented								xxxx xxxx	uuuu uuuu	*,*,*,*,*,*,*,*
008h	PRINC1	Contents of FSR0 to address data memoryvalue of FSR1 pre-incremented								xxxx xxxx	uuuu uuuu	*,*,*,*,*,*,*,*
009h	PLUSW1	Contents of FSR1 to address data memoryvalue of FSR0 offset by W								xxxx xxxx	uuuu uuuu	*,*,*,*,*,*,*,*
00Fh	FSR0H	-	-	-	-	-	-	-	FSR0[8]	 xxxx	.... uuuu	-,-,-,- *,*,*,*
010h	FSR0L	Indirect Data Memory Address Pointer 0 Low Byte,FSR0[7:0]								xxxx xxxx	uuuu uuuu	*,*,*,*,*,*,*,*
011h	FSR1H	-	-	-	-	-	-	-	FSR1[8]	xxx	.... .uuu	-,-,-,- *,*,*,*
012h	FSR1L	Indirect Data Memory Address Pointer 0 Low Byte,FSR0[7:0]								xxxx xxxx	uuuu uuuu	*,*,*,*,*,*,*,*
016h	TOSH	-	-	-	-	TOS[11]	TOS[10]	TOS[9]	TOS[8]	..xx xxxx	..uu uuuu	-,-,*,*,*,*,*,*
017h	TOSL	Top-of-Stack Low Byte (TOS<7:0>)								xxxx xxxx	uuuu uuuu	*,*,*,*,*,*,*,*
018h	SKCN	SKFL	SKUN	SKOV	-	-	SKPRT[2:0]			000. 0000	u$$. $$$$	rw0,rw0,rw0,- *,*,*,*
01Ah	PCLATH	-	-	-	-	PC[11]	PC[10]	PC[9]	PC[8]	..00 0000	..00 0000	*,*,*,*,*,*,*,*
01Bh	PCLATL	PC Low Byte for PC<7:0>								0000 0000	0000 0000	*,*,*,*,*,*,*,*
01Dh	TBLPTRH	-	-	-	Program Memory Table Pointer High Byte (TBLPTR<12:8>)					..xx xxxx	..uu uuuu	-,-,*,*,*,*,*,*
01Eh	TBLPTRL	Program Memory Table Pointer Low Byte (TBLPTR<7:0>)								xxxx xxxx	uuuu uuuu	*,*,*,*,*,*,*,*
01Fh	TBLDH	Program Memory Table Latch High Byte								xxxx xxxx	uuuu uuuu	*,*,*,*,*,*,*,*
020h	TBLDL	Program Memory Table Latch Low Byte								xxxx xxxx	uuuu uuuu	*,*,*,*,*,*,*,*
021h	PRODH	Product Register of Multiply High Byte								xxxx xxxx	uuuu uuuu	*,*,*,*,*,*,*,*
022h	PRODL	Product Register of Multiply Low Byte								xxxx xxxx	uuuu uuuu	*,*,*,*,*,*,*,*
023h	INTE0	GIE	-	ADIE	WDTIE	TB1IE	TMAIE	E1IE	E0IE	0000 0000	0uuu uuuu	*,*,*,*,*,*,*,*
024h	INTE1	-	SPIIE	TXIE	RCIE	I2CERIE	I2CIE	E3IE	E2IE	0000 0000	uuuu uuuu	*,*,*,*,*,*,*,*
026h	INTF0	-	-	ADIF	WDTIF	TB1IF	TMAIF	E1IF	E0IF	.000 0000	.uuu uuuu	*,*,*,*,*,*,*,*
027h	INTF1	-	SPIIF	TXIF	RCIF	I2CERIF	I2CIF	E3IF	E2IF	0000 0000	uuuu uuuu	*,*,*,* r,r,*,*
029h	WREG	Working Register								xxxx xxxx	uuuu uuuu	*,*,*,*,*,*,*,*
02Ah	BSRCN	-	-	-	-	-	-	-	BSR[0]	 xxxx	.... uuuu	-,-,-,- *,*,*,*
02Bh	MSTAT	-	-	-	C	DC	N	OV	Z	...x xxxx	...u uuuu	-,-,-,*,*,*,*,*
02Ch	PSTAT	BOR	PD	TO	IDL	RST	SKERR	-	-	$000 $00.	uu$u u$u.	rw0,rw0,rw0,rw0 rw0,rw0,rw0,-
02Eh	BIECN	1			ENBVD	VPPHV	ENBCP	BIEWR	BIERD	1... $000	1... $uuu	r1,-,-,- r,*,*,*
02Fh	BIEARH	IFR & eIFR		1	1	1	1	1	1	0... xxxx	u... uuuu	*,-,-,- *,*,*,*
030h	BIEARL			BIE Address Register as BIEAL[5:0]						xxxx xxxx	uuuu uuuu	*,*,*,*,*,*,*,*
031h	BIEDRH	BIE High Byte Data Register								xxxx xxxx	uuuu uuuu	*,*,*,*,*,*,*,*
032h	BIEDRL	BIE Low Byte Data Register								xxxx xxxx	uuuu uuuu	*,*,*,*,*,*,*,*
033h	PWRCN	ENBGR	LDOC[2:0]			LDOM[0]	LDOM	ENLDO	CSFON	0000 0000	uuuu u00u	*,*,*,* *,wr0,wr0,*
034h	OSCCN0	OSCS[1:0]		DHS[1:0]		DMS[2:0]			CUPS	0000 0000	uuuu uuuu	*,*,*,*,*,*,*,*
035h	OSCCN1		LCPS	DADC[1:0]		DTMB[1:0]		TMBS	LCDS	0000 0000	uuuu uuu.	*,*,*,*,*,*,*,-
036h	OSCCN2	DLCD[1:0]		ENXT	XTS[1:0]		-	HAOM0	ENHAO	0000 0011	uuuu uu11	*,*,*,*,*,*,*,r
037h	WDTCN	ENBZ	BZS	BZ[1:0]		ENWDT	DWDT[2:0]			0000 0000	uuuu $000	-,*,*,* rw1,*,*,*
038h	TMACN	ENTMA	TMACL	TMAS	DTMA[2:0]			-	-	0000 00..	u0uu uu..	*,rw1,*,*,*,-,-
039h	TMAR	TMA counter Register								0000 0000	uuuu uuuu	rw0,rw0,rw0,rw0 rw0,rw0,rw0,rw0
03Ah	AD1H	ADC1 conversion high byte data register								..00 0000	..uu uuuu	-,-,*,*,*,*,*,*
03Bh	AD1M	ADC1 conversion middle byte data register								0000 0000	uuuu uuuu	*,*,*,*,*,*,*,*
03Ch	AD1L	ADC1 conversion low byte data register								0000 0000	uuuu uuuu	*,*,*,*,*,*,*,*
03Dh	AD1CN0	ENAD1	-	-	OSR[3:0]				CMFR	000. 0000	uuu. uuuu	*,*,*,*,*,*,*,*
03Eh	AD1CN1	-	-	VREGN	PGAGN[1:0]		ADGN[2:0]			xxxx xxxx	uuuu uuuu	*,*,*,*,*,*,*,*
03Fh	AD1CN2	-	-	-	-	DCSET[3:0]				xxxx xxxx	uuuu uuuu	*,*,*,*,*,*,*,*
040h	AD1CN3	-	-	INP[1:0]		-	-	INN[1:0]		xxxx xxxx	uuuu uuuu	*,*,*,*,*,*,*,*
041h	AD1CN4	-	VRH[0]	-	-	INX[1:0]		-	INIS	0010 0000	uuuu uuuu	*,*,*,*,*,*,*,*
042h	AD1CN5	-	-	-	-	-	-	ENTPS	TPSCH	0000 0000	uuuu uuuu	*,*,*,*,*,*,*,*

表 5-1 資料記憶體列表

"-"no use,"*"read/write,"w"write,"r"read,"r0"only read 0,"r1"only read 1,"w0"only write 0,"w1"only write 1
"$"for event status,"."unimplemented bit,"x"unknown,"u"unchanged,"d"depends on condition

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	ARST	IRST	R/W
043h	CSFCN0	SKRST	x	HAOTR[5:0]						0	....u	-,-,-,- -,-,-,*
045h	LVDCN	-	-	PWRS	LVDS[3:0]				LVDO	0000 0000	uuuu uuuu	*,*,*,*,*,*,*,*
04Eh	TB1Flag	-	-	PWM6A	PWM5A	PWM4A	PWM3A	PWM2A	PWM1A	..00 0000	..uu uuuu	-,-,r,r r,r,r,r
04Fh	TB1CN0	ENTB1	TB1M[1:0]		TB1RT[1:0]		TB1CL	-	-	0000 0000	uuuu u0uu	*,*,*,*,rw1,*,*
050h	TB1CN1	PA1IV	PWMA1[2:0]			PA0IV	PWMA0[2:0]			0000 0000	uuuu uuuu	*,*,*,*,*,*,*,*
051h	TB1RH	TimerB1 counter Register [15:8]								xxxx xxxx	uuuu uuuu	r,r,r,r r,r,r,r
052h	TB1RL	TimerB1 counter Register [7:0]								xxxx xxxx	uuuu uuuu	r,r,r,r r,r,r,r
053h	TB1C0H	TimerB1 counter Condition Register [15:8]								xxxx xxxx	uuuu uuuu	*,*,*,*,*,*,*,*
054h	TB1C0L	TimerB1 counter Condition Register [7:0]								xxxx xxxx	uuuu uuuu	*,*,*,*,*,*,*,*
055h	TB1C1H	TimerB1 counter Condition Register [15:8]								xxxx xxxx	uuuu uuuu	*,*,*,*,*,*,*,*
056h	TB1C1L	TimerB1 counter Condition Register [7:0]								xxxx xxxx	uuuu uuuu	*,*,*,*,*,*,*,*
057h	TB1C2H	TimerB1 counter Condition Register [15:8]								xxxx xxxx	uuuu uuuu	*,*,*,*,*,*,*,*
058h	TB1C2L	TimerB1 counter Condition Register [7:0]								xxxx xxxx	uuuu uuuu	*,*,*,*,*,*,*,*
059h	TCCN0	-	TC1S[1:0]		-	-	-	-	-	0000 0000	uuuu uuuu	*,*,*,*,*,*,*,*
05Eh	SSPCN0	ENSSP	CKP	CKE	SMP	-	-	SSPM[1:0]		0000 ..00	uuuu ..uu	*,*,*,*,-,-,*,*
05Fh	SSPSTA	SSPBY	SSPOV	-	-	-	-	-	BF	00.. ...0	uu.. ...u	*,*,-,- -,-,-,*
060h	SSPBUF	SSP Receive/Transmit Buffer Register								xxxx xxxx	uuuu uuuu	*,*,*,*,*,*,*,*
061h	CFG	-	-	-	-	-	I2CRST	ENI2CT	ENI2C	0000 0000	.... .uuu	-,-,-,- -,*,*,*
062h	ACT	SLAVE	ADR10	SLAVE24	I2CER	START	STOP	I2CINT	ACK	0000 0000	uuuu uuuu	*,*,*,*,*,*,*,*
063h	STA	MACTF	SACTF	RDBF	RWF	DFF	ACKF	GCF	ARBF	0001 0000	uuuu uuuu	*,*,*,*,*,*,*,*
064h	CRG	CRG[7:0]								0000 0000	uuuu uuuu	*,*,*,*,*,*,*,*
065h	TOC	I2CTF	DI2C[2:0]			I2CTLT[3:0]				0000 0000	uuuu uuuu	*,*,*,*,*,*,*,*
066h	RDB	RDB[7:1]							RDB[0]	xxxx xxxx	uuuu uuuu	*,*,*,*,*,*,*,*
067h	TDB0	TDB0[7:1]							TDB0[0]	xxxx xxxx	uuuu uuuu	*,*,*,*,*,*,*,*
068h	SID0	SID0[7:1],The corresponding address of the 7-bit mode or address 10-bit mode 15-9bit							SID0V[0]	0000 0000	uuuu uuuu	*,*,*,*,*,*,*,*
069h	UR0CN	ENSP	ENTX	TX9	TX9D	PARITY	-	-	WUE	0000 0..0	uuuu u..u	*,*,*,*,-,-,*
06Ah	UR0STA	-	RC9D	PERR	FERR	OERR	RCIDL	TRMT	ABDOVF	.000 0010	.uuu uuuu	-,r,r,r r,r,r,rw0
06Bh	BA0CN	-	-	-	-	ENCR	RC9	ENADD	ENABD	 0000	.... uuuu	-,-,-,- *,*,*,*
06Ch	BG0RH	-	-	-	Baud Rate Generator Register High Byte					...x xxxx	...u uuuu	-,-,-,*,*,*,*,*
06Dh	BG0RL	Baud Rate Generator Register Low Byte								xxxx xxxx	uuuu uuuu	*,*,*,*,*,*,*,*
06Eh	TX0R	UART Transmit Register								xxxx xxxx	uuuu uuuu	*,*,*,*,*,*,*,*
06Fh	RCREG	UART Receive Register								xxxx xxxx	uuuu uuuu	r,r,r,r r,r,r,r
070h	PT1	PT1.7	PT1.6	PT1.5	PT1.4	PT1.3	PT1.2	PT1.1	PT1.0	xxxx xxxx	xxxx xxxx	*,*,*,*,*,*,*,*
071h	TRISC1	TC1.7	TC1.6	TC1.5	TC1.4	TC1.3	TC1.2	TC1.1	TC1.0	0000 0000	uuuu uuuu	*,*,*,*,*,*,*,*
072h	PT1DA	-	-	-	-	-	DA1.2	-	-	0000 0000	uuuu uuuu	*,*,*,*,*,*,*,*
073h	PT1PU	PU1.7	PU1.6	PU1.5	PU1.4	PU1.3	PU1.2	PU1.1	PU1.0	0000 0000	uuuu uuuu	*,*,*,*,*,*,*,*
074h	PT1M1	-	-	-	-	INTEG1[1:0]		INTEG0[1:0]		0000 0000	uuuu uuuu	*,*,*,*,*,*,*,*
075h	PT1M2	-	PM1.7[0]	-	PM1.6[0]	-	PM1.5[0]	-	PM1.4[0]	xxxx xxxx	xxxx xxxx	*,*,*,*,*,*,*,*
076h	PT1INT	INTEG7	INTEG6	INTEG5	INTEG4	INTEG3	INTEG2	-	-	0000 0000	uuuu uuuu	*,*,*,*,*,*,*,*
077h	PT2	-	-	-	-	-	-	PT2.1	PT2.0	0000 0000	uuuu uuuu	*,*,*,*,*,*,*,*
078h	TRISC2	-	-	-	-	-	-	TC2.1	TC2.0	0000 0000	uuuu uuuu	*,*,*,*,*,*,*,*
07Ah	PT2PU	-	-	-	-	-	-	PU2.1	PU2.0	0000 0000	uuuu uuuu	*,*,*,*,*,*,*,*
080h ~ 017Fh		General Purpose Register as 256Byte								uuuu uuuu	uuuu uuuu	*,*,*,*,*,*,*,*
180h	LCDCN1	ENLCP	LCDV[2:0]			ENLB	SEL_PCLK	PWMO1	-	0000 00..	uuuu uu..	*,*,*,*,*,-,-
181h	LCDCN2	S9_2MODE		S13M	S12M	S11M	S10M	LCDBL	LCI	0000 00..	uuuu uu..	*,*,*,*,*,-,-
182h	LED0	Display (LED) and GPIO data register 0								xxxx xxxx	uuuu uuuu	*,*,*,*,*,*,*,*
183h	LED1	Display (LED) and GPIO data register 1								xxxx xxxx	uuuu uuuu	*,*,*,*,*,*,*,*
184h	LED2	Display (LED) and GPIO data register 2								xxxx xxxx	uuuu uuuu	*,*,*,*,*,*,*,*
185h	LED3	Display (LED) and GPIO data register 3								xxxx xxxx	uuuu uuuu	*,*,*,*,*,*,*,*
186h	LED4	Display (LED) and GPIO data register 4								xxxx xxxx	uuuu uuuu	*,*,*,*,*,*,*,*
187h	LED5	Display (LED) and GPIO data register 5								xxxx xxxx	uuuu uuuu	*,*,*,*,*,*,*,*
188h	LED6	Display (LED) data register 6								xxxx xxxx	uuuu uuuu	*,*,*,*,*,*,*,*
189h	LED7	Display (LED) data register 7								xxxx xxxx	uuuu uuuu	*,*,*,*,*,*,*,*

表 5-2 資料記憶體列表(續)

6. 電氣特性

Absolute Maximum Ratings :

Absolute maximum ratings over operating free-air temperature (unless otherwise noted)

Voltage applied at V_{DD} to V_{SS} . . . . −0.2 V to 6.0 V

Voltage applied to any pin . . . . −0.2 V to V_{DD} + 0.3 V

Voltage applied to RST/VPP pin . . . . −0.2 V to 8.5 V

Diode current at any device terminal . . . . ±2 mA

Storage temperature, Tstg: (unprogrammed device) . . . . −55℃ to 125℃

(programmed device) . . . . −40℃ to 85℃

Total power dissipation. 0.5w

Maximum output current sink by any I/O pin. 10mA

6.1. Recommended operating conditions

T_A = -40℃ ~ 85℃,unless otherwise noted

Sym.	Parameter		Test Conditions		Min.	Typ.	Max.	unit
V_{DD}	Supply Voltage		All digital peripherals and CPU		2.2		5.5	V
V_{DDA}	Supply Voltage		Analog peripherals		2.4		4.5	
V_{SS}	Supply Voltage				0		0	
XT	External Oscillator Frequency	Watch crystal	V_{DD} = 2.2V, ENXT[0]=1	XTS[1:0]=0x		32768		Hz
		Ceramic resonator		XTS[1:0]=10	450K		4M	
		Crystal		XTS[1:0]=11	1M		4M	

6.2. Internal RC Oscillator

T_A = 25℃,VDD = 3.0V,unless otherwise noted

Sym.	Parameter	Test Conditions	Min.	Typ.	Max.	unit
HAO	High Speed Oscillator frequency	ENHAO[0]=1, HAOM[1:0]=00	-20%	2	+20%	MHz
		ENHAO[0]=1, HAOM[1:0]=01	-20%	4	+20%	MHz
LPO	Low Power Oscillator frequency	VDD supply voltage be enable LPO	-20%	14.5	+20%	KHz

6.3. Supply current into VDD excluding peripherals current

T_A = 25℃,V_{DD} = 3.3V,OSC_LPO = 14.5KHz,unless otherwise noted

Sym.	Parameter	Test Conditions	Min.	Typ.	Max.	unit
I_{AM1}	Active mode 1	OSC_CY = off, OSC_HAO = 4MHz, CPU_CK = 4MHz		310	620	uA
I_{AM2}	Active mode 2	OSC_CY = off, OSC_HAO = 2MHz, CPU_CK = 2MHz		200	400	uA
I_{AM3}	Active mode 3	OSC_CY = off, OSC_HAO = 2MHz, CPU_CK = 1MHz		150	300	uA
I_{LP1}	Low Power 1	OSC_CY = 32768Hz, OSC_HAO = off, CPU_CK = LPO, Idle state		3	5	uA
I_{LP2}	Low Power 2	OSC_CY = off, OSC_HAO = off, CPU_CK = LPO, Idle state		1.1	2.5	uA
I_{LP3}	Low Power 3	OSC_CY = off, OSC_HAO = off, CPU_CK = off, Sleep state		0.4	1.5	uA

OSC_CY：External Oscillator frequency.
OSC_HAO：Internal High Accuracy Oscillator frequency.
CPU_CK：CPU core work frequency.

T_A = 25℃,V_{DD} = 5.5V,OSC_LPO = 14.5KHz,unless otherwise noted

Sym.	Parameter	Test Conditions	Min.	Typ.	Max.	unit
I_{AM1}	Active mode 1	OSC_CY = off, OSC_HAO = 4MHz, CPU_CK = 4MHz		500	1000	uA
I_{AM2}	Active mode 2	OSC_CY = off, OSC_HAO = 2MHz, CPU_CK = 2MHz		320	640	uA
I_{AM3}	Active mode 3	OSC_CY = off, OSC_HAO = 2MHz, CPU_CK = 1MHz		270	540	uA
I_{LP1}	Low Power 1	OSC_CY = 32768Hz, OSC_HAO = off, CPU_CK = LPO, Idle state		5.5	15	uA
I_{LP2}	Low Power 2	OSC_CY = off, OSC_HAO = off, CPU_CK = LPO, Idle state		2.1	5	uA
I_{LP3}	Low Power 3	OSC_CY = off, OSC_HAO = off, CPU_CK = off, Sleep state		0.5	2	uA

OSC_CY：External Oscillator frequency.
OSC_HAO：Internal High Accuracy Oscillator frequency.
CPU_CK：CPU core work frequency.

6.4. Port 1~2, 6~7

T_A = 25℃,VDD = 3.0V,unless otherwise noted

Sym.	Parameter	Test Conditions	Min.	Typ.	Max.	unit
Input voltage and Schmitt trigger and leakage current and timing						
V_{IH}	High-Level input voltage				0.7*VDD	V
V_{IL}	Low-Level input voltage		0.3*VDD			V
V_{hys}	Input Voltage hysteresis(V_{IH} - V_{IL})			0.3*VDD		V
I_{LKG}	Leakage Current				0.1	uA
R_{PU}	Port pull high resistance			60		kΩ
Output voltage and current and frequency						
V_{OH}	High-level output voltage	VDD<4V, I_{OH}=10mA,	V_{DD} -0.4			V
		VDD>=4V, I_{OH}=15mA,	V_{DD} -0.4			
V_{OL}	Low-level output voltage	VDD<4V, I_{OL}=-10mA			V_{SS} +0.3	
		VDD>=4V, I_{OL}=-15mA			V_{SS} +0.3	
I_{OH}	High-level output source current (SEG and COM port)	VDD=3V, V_{OH} =V_{DD} -0.4			10	mA
		VDD=4V, V_{OH} =V_{DD} -0.4			15	
I_{OL}	Low-level output sink current (SEG port only)	VDD=3V, V_{OL} =V_{SS} +0.3			10	
		VDD=4V, V_{OL} =V_{SS} +0.4			20	
I_{OL}	Low-level output sink current (COM port only)	VDD=3V, V_{OL} =V_{SS} +0.3			20	
		VDD=4V, V_{OL} =V_{SS} +0.4			40	

6.5. Reset(Brownout, Low Voltage Detect)

T_A = 25℃,VDD = 3.0V,unless otherwise noted

Sym.	Parameter	Test Conditions	Min.	Typ.	Max.	unit
BOR	Pulse length needed to accepted reset internally, t_{d-LVR}		2			us
	V_{DD} Start Voltage to accepted reset internally (L➔H),V_{LVR}		1.6	1.85	2.1	V
	Hysteresis, $V_{HYS-LVR}$			30		mV
RST	Pulse length needed as RST/VPP pin to accepted reset internally, t_{d-RST}		2			us
	Input Voltage to accepted reset voltage			1.1		V
	Reset release voltage			2		V
LVD	Operation current, I_{LVD}			10		uA
	External input voltage to compare reference voltage		1.15	1.2	1.25	V
	Compare reference voltage temperature drift	T_A = -40℃ ~ 85 ℃		50		ppm/℃
	Detect V_{DD} voltage rang by user option, V_{SVS} VLDx[3:0]=1110b		-0.1V	4.0	+0.1V	V
	Detect V_{DD} voltage rang by user option, V_{SVS} VLDx[3:0]=1101b			3.6		
	Detect V_{DD} voltage rang by user option, V_{SVS} VLDx[3:0]=1100b			3.3		
	Detect V_{DD} voltage rang by user option, V_{SVS} VLDx[3:0]=1011b			3.0		
	Detect V_{DD} voltage rang by user option, V_{SVS} VLDx[3:0]=1010b			2.9		
	Detect V_{DD} voltage rang by user option, V_{SVS} VLDx[3:0]=1001b			2.8		
	Detect V_{DD} voltage rang by user option, V_{SVS} VLDx[3:0]=1000b			2.7		
	Detect V_{DD} voltage rang by user option, V_{SVS} VLDx[3:0]=0111b			2.6		
	Detect V_{DD} voltage rang by user option, V_{SVS} VLDx[3:0]=0110b			2.5		
	Detect V_{DD} voltage rang by user option, V_{SVS} VLDx[3:0]=0101b			2.4		
	Detect V_{DD} voltage rang by user option, V_{SVS} VLDx[3:0]=0100b			2.3		
	Detect V_{DD} voltage rang by user option, V_{SVS} VLDx[3:0]=0011b			2.2		
	Detect V_{DD} voltage rang by user option, V_{SVS} VLDx[3:0]=0010b			2.1		
	Detect V_{DD} voltage rang by user option, V_{SVS} VLDx[3:0]=0001b			2.0		

BOR：Brownout Reset
LVR：Low Voltage Reset of BOR
LVD：Low Voltage Detect
RST：External Reset pin

6.6. Power System

T_A = 25℃,VDD = 3.0V,unless otherwise noted

Sym.	Parameter	Test Conditions		Min.	Typ.	Max.	unit
VDDA	VDDA operation current, I_{VDDA}	I_L = 0mA	LDOC[2:0]=000b	-5%	12	+5%	uA
	Select VDDA output voltage	I_L = 0.1mA, VDD≧VDDA+0.25V	LDOC [2:0]=000b		2.4		V
			LDOC [2:0]=001b		2.6		V
			LDOC [2:0]=010b		2.9		V
			LDOC [2:0]=011b		3.3		V
			LDOC [2:0]=100b		3.6		V
			LDOC [2:0]=101b		4.0		V
			LDOC [2:0]=110b		4.5		V
	Dropout voltage	I_L = 10mA	LDOC [2:0]=000b	250			mV
	Temperature drift	LDOC [2:0]=000b I_L = 10uA	T_A=-40℃~85℃	50			ppm/℃
	V_{DD} Voltage drift	LDOC [2:0]=000b	V_{DD}=2.2V~5.5V	±0.2			%/V
VDDA：Adjust Voltage Regulator							

6.7. SD18, Power Supply and recommended operating conditions

TA = 25℃,VDD = 3.0V, VDDA=2.4V,unless otherwise noted

Sym.	Parameter	Test Conditions		Min.	Typ.	Max.	unit
V_{SD18}	Supply Voltage at VDDA	ENLDO[0]=0		2.4		4.5	V
f_{SD18}	Modulator sample frequency, ADC_CK			250	500		KHz
	Over Sample Ratio, OSR			64		65536	
I_{SD18}	Operation supply current without PGA	ENAD1 [0]=1	GAIN =16, ADC_CK= 500KHz		200		uA

6.7.1. PGA, Power Supply and recommended operating conditions

T_A = 25℃,V_{DD} = 3.0V, VDDA=2.4V,unless otherwise noted

Sym.	Parameter	Test Conditions		Min.	Typ.	Max.	unit
V_{PGA}	Supply Voltage at VDDA	ENLDO [0]=0		2.4		4.5	V
I_{PGA}	Operation supply current	PGAGN[1:0]=<11>			450		uA
G_{PGA}	Gain temperature drift	T_A = -40℃~ 85℃	GAIN=128		15		ppm/℃

6.7.2. SD18,performance

T_A = 25℃,V_{DD} = 3.6V, VDDA=2.4V,V_{VR}= AI2(short to VDDA)/2,GAIN=16 with PGA=8,fSD18=500KHz,unless otherwise noted

Sym.	Parameter	Test Conditions		Min.	Typ.	Max.	unit
INL	Integral Nonlinearity(INL)	VDDA=2.4V,V_{VR}= AI2/2, ΔSI=±200mV					
		VDDA=2.4V,V_{VR}= AI2/2, ΔSI=±450mV			±0.003	±0.01	%FSR
G_{SD18}	Temperature drift Gain x16	T_A = -40℃~ 85℃			10		ppm/℃
E_{OS}	Offset error of Full Scale Rang input voltage range with PGA=8	ΔAI=0V ΔVR=1.2V DCSET[3:0]=<0000> *ΔAI is external short	GAIN=16			1	%FSR
	Offset error temperature drift with PGA=8		GAIN=16		0.15		uV/℃
CM_{SD18}	Common-mode rejection	V_{CM}=0.7V to 1.7V, V_{VR}= 1.0V,without PGA	V_{SI}=0V, GAIN=16		75		dB
PSRR	DC power supply rejection	VDDA=3.0V,ΔVDDA= ±100mV, V_{VR}=1.0V, V_{SI}=1.2V,V_{SI-}=1.2V,	GAIN=16 PGA=8		75		dB

6.7.3. SD18 Noise Performance

T_A = 25℃,V_{DD} = 3.0V, VDDA=2.4V,unless otherwise noted

HY15P43 針對 SD18 提供了重要的輸入雜訊規格。Table6.8-3(a), Table6.8-3(b) 列出典型的雜訊規格表與 Gain, Output rate, 及單端最大輸入電壓等關係。測試條件設定在外部輸入訊號短路，參考電壓為 1.2V，取樣 1024 筆資料。

ENOB(RMS) with OSR/GAIN at A/D Clock=500Khz, VDDA=2.4V, VREF=1.2V																
Max. Vin(mV) =0.9*VREF (1)	**OSR**					**64**	**128**	**256**	**512**	**1024**	**2048**	**4096**	**8192**	**16384**	**32768**	**65536**
	Output rate(HZ)					**7813**	**3906**	**1953**	**977**	**488**	**244**	**122**	**61**	**31**	**15**	**8**
	Gain	**=**	**PGA**	**×**	**ADGN**											
±67.5	**16**	**=**	**1**	**×**	**16**	9.50	13.96	14.92	15.48	16.03	16.50	16.98	17.49	17.91	18.38	18.87
±33.75	**32**	**=**	**2**	**×**	**16**	9.49	13.45	14.18	14.67	15.20	15.72	16.21	16.67	17.20	17.68	18.04
±16.875	**64**	**=**	**4**	**×**	**16**	9.49	13.14	13.87	14.34	14.85	15.27	15.84	16.31	16.79	17.33	17.75
±8.435	**128**	**=**	**8**	**×**	**16**	9.49	12.69	13.32	13.73	14.27	14.76	15.31	15.79	16.36	16.88	17.24
(1) Max.Vin (mV) is the max. input voltage of single end to ground (VSS).																

Table6.8-3(a) SD18 ENOB Table

RMS Noise(uV) with OSR/GAIN at A/D Clock=500Khz, VDDA=2.4V, VREF=1.2V																
Max. Vin(mV) =0.9*VREF	**OSR**					**64**	**128**	**256**	**512**	**1024**	**2048**	**4096**	**8192**	**16384**	**32768**	**65536**
	Output rate(HZ)					**7813**	**3906**	**1953**	**977**	**488**	**244**	**122**	**61**	**31**	**15**	**8**
	Gain	**=**	**PGA**	**×**	**ADGN**											
±67.5	**16**	**=**	**1**	**×**	**16**	207.05	9.42	4.84	3.28	2.25	1.62	1.16	0.82	0.61	0.44	0.31
±33.75	**32**	**=**	**2**	**×**	**16**	103.99	6.68	4.05	2.88	1.99	1.39	0.99	0.72	0.50	0.36	0.28
±16.875	**64**	**=**	**4**	**×**	**16**	51.99	4.15	2.51	1.81	1.27	0.95	0.64	0.46	0.33	0.23	0.17
±8.435	**128**	**=**	**8**	**×**	**16**	26.11	2.83	1.84	1.38	0.95	0.67	0.46	0.33	0.22	0.16	0.12

Table6.8-3(b) SD18 RMS Noise Table

The RMS noise are referred to the input. The Effective Number of Bits (ENOB(RMS Bit)) is defined as:

$$\text{ENOB(RMS)} = \ln\left(\frac{\text{FSR}}{\text{RMS Noise}}\right) \Big/ \ln(2)$$

$$\text{RMS Noise} = \left(2 \times \text{VREF} \times \sqrt{\sum_{k=1}^{1024}(\text{ADO}[k] - \text{Average})^2}\right) \Big/ 2^{23}$$

$$\text{Where FSR (Full - Scale Range)} = 2 \times \text{VREF/Gain.}$$

$$\text{Average} = \frac{\sum_{k=1}^{1024}(\text{ADO}[k])}{1024}$$

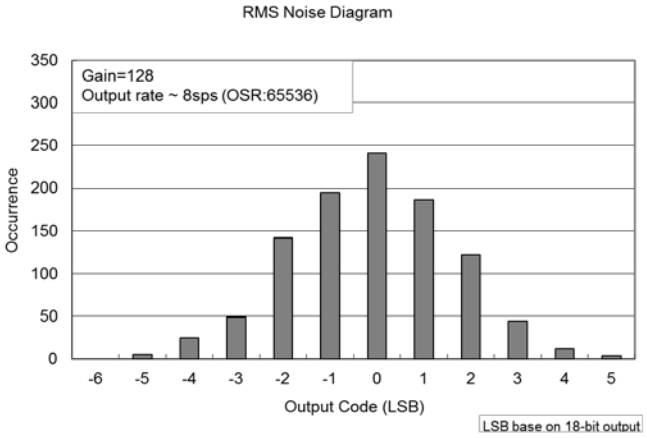


Figure6.8-3(a) RMS Noise Diagram

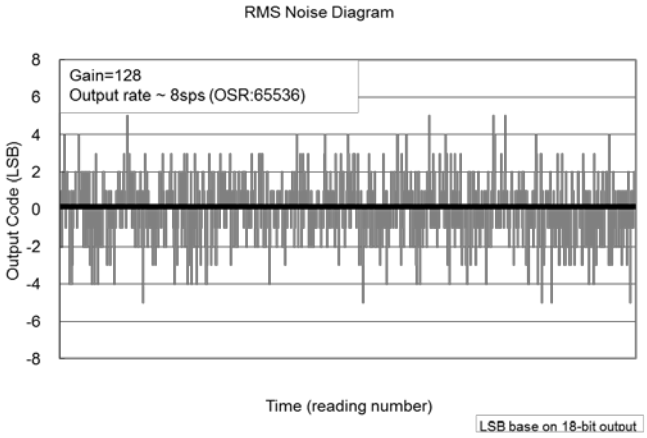


Figure6.8-3(b) Output Code Diagram

6.8. Build-In EPROM(BIE)

T_A = 25℃,V_{DD} = 3.0V, unless otherwise noted

Sym.	Parameter	Test Conditions	Min.	Typ.	Max.	unit
V_{BIE}	Supply Voltage at VPP PIN			8.5	8.75	V
I_{BIE}	Operation supply current			3		mA
V_{SS}	Supply Voltage			0		V
When connecting to the external V_{BIE} power source to program the BIE block, users can use the instruction to program the words one by one into the BIE block.						

6.9. Build-In EPROM(BIE) Low voltage control circuit

T_A = 25℃,V_{DD} = 3.05V, unless otherwise noted

Sym.	Parameter	Test Conditions	Min.	Typ.	Max.	unit
T_O	Operation temperature range		0	25	40	℃
V_{DD}	Operation supply Voltage		2.75		5.5	V
V_{SS}	Supply Voltage			0		V
When the 2.75V low voltage programming control circuit is activated, users can program the BIE block without connecting to the external V_{BIE} power source.						

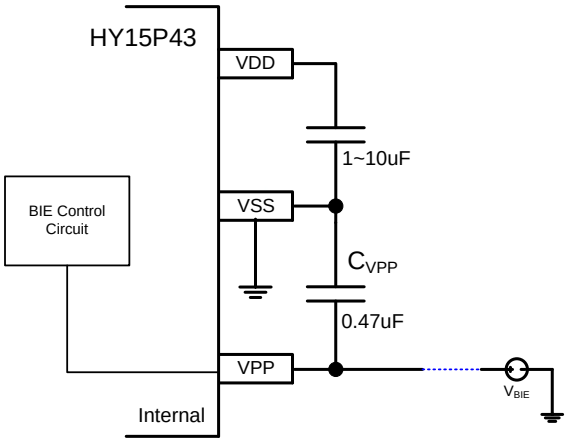


圖 6-1 BIE typical application 方塊圖

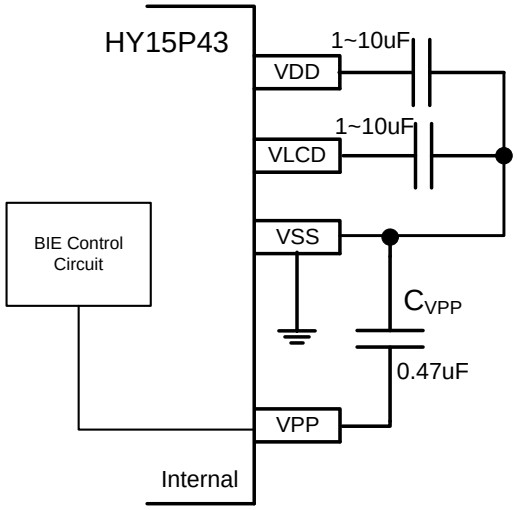


圖 6-2 BIE typical application use low voltage control circuit 方塊圖

7. 訂貨資訊

下單品名[1]	封裝型式	引腳數	封裝型式		程式碼	出貨包裝形式	個裝數量	材料組成	MSL[3]
			描述方式		編號[2]				
HY15P43-D000	Die	-	D	000	000	-	250	Green[4]	-
HY15P43-T028	TSSOP	28	T	028	000	Tube	50	Green[4]	MSL-3
HY15P43-T028	TSSOP	28	T	028	000	Tape & Reel	4000	Green[4]	MSL-3
HY15P43-L048	LQFP	48	L	048	000	Tray	250	Green[4]	MSL-3

[1] **產品名稱 – 封裝型式描述方式 – 程式碼編號（空白片 / 標準品 / 代客燒錄碼）**

例如：您的 HY15P43 代客燒錄服務申請的程式碼編號為 008，且需要的產品是裸片出貨。則下單品名為 HY15P43-D000-008

例如：您的需求是 HY15P43 不帶程式碼的空白片且需要的產品是裸片出貨。則下單品名為 HY15P43-D000

例如：您的需求是 HY15P43 不帶程式碼的空白片且需要的產品是封裝片 LQFP 7x7 48L 出貨，則下單品名為 HY15P43-L048，且需以 Tray 出貨，則除下單品名外，請特別註明出貨包裝形式為 Tray

例如：您的 HY15P43 代客燒錄服務申請的程式碼編號為 009，而需求的產品是封裝片 TSSOP 出貨，則下單品名為 HY15P43-T028-009，且需以 Tape & Reel 出貨，則除下單品名外，請特別註明出貨包裝形式為 Tape & Reel

[2] **程式碼編號**

“001”~“999” 為標準品或代客燒錄申請的程式碼編號，而空白晶片不帶此碼。

[3] **MSL:**

濕度敏感性等級係依據 IPC/JEDEC J-STD-020 的規範加以試驗分級，並參考 IPC/JEDEC J-STD-033 的標準處理、包裝、運輸與使用。

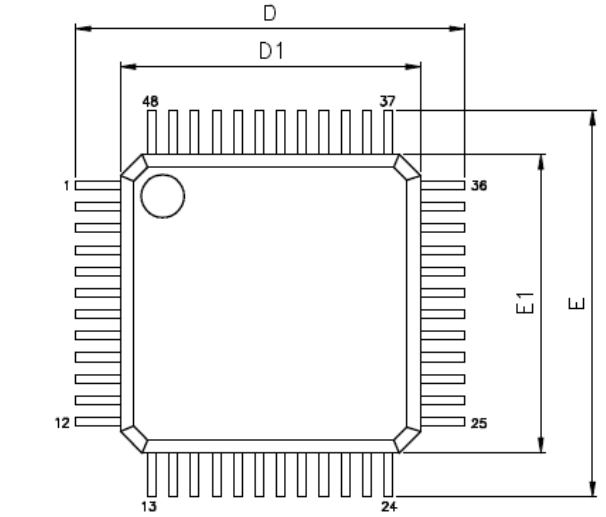
[4] **Green (RoHS & no Cl/Br):**

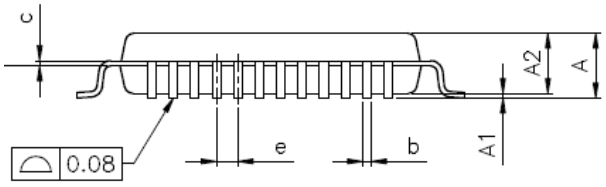
HYCON 產品皆為 Green Product，符合 RoHS 指令以及無鹵素規定。

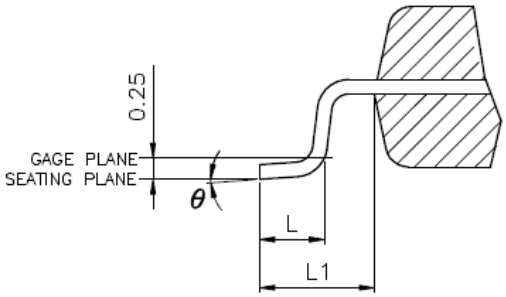
8. 封裝型式資訊

8.1. LQFP 7x7 48L(L048)

8.1.1. Package Dimensions







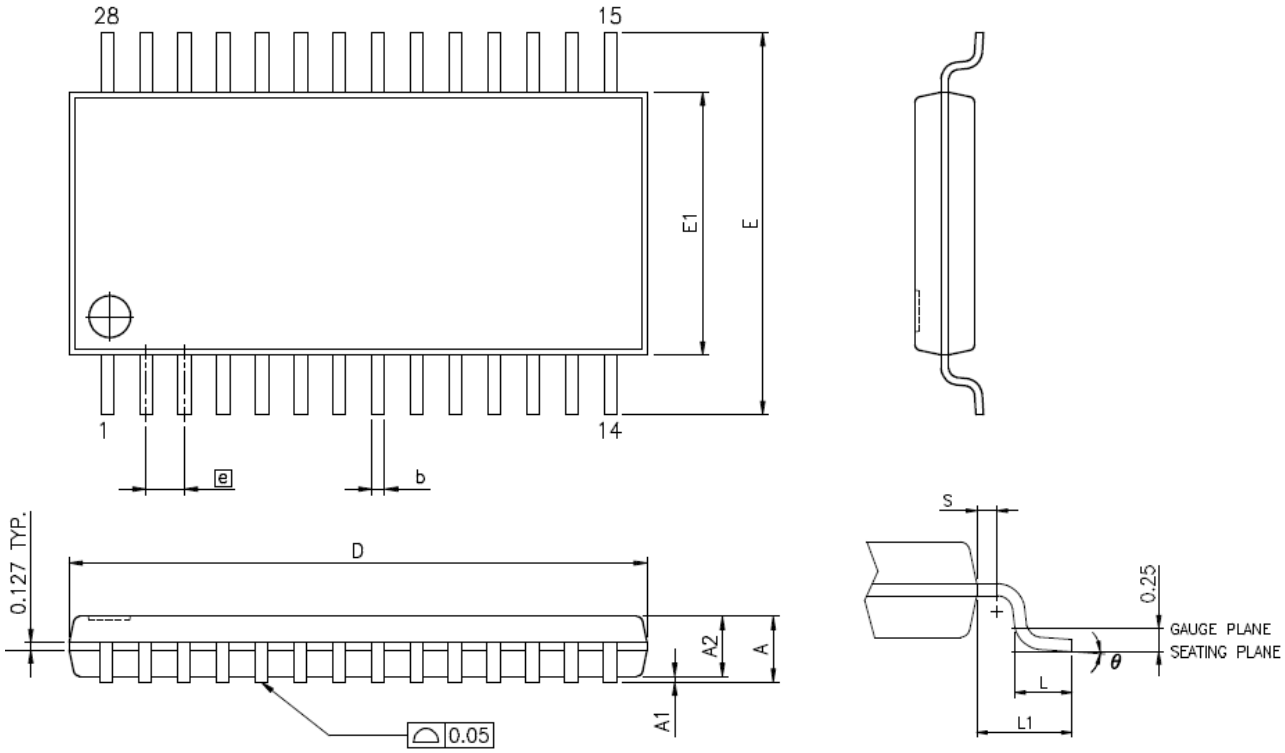
SYMBOLS	MIN.	NOM.	MAX.
A	--	--	1.60
A1	0.05	--	0.15
A2	1.35	1.40	1.45
b	0.17	0.22	0.27
c	0.09	--	0.20
D	9.00 BSC		
D1	7.00 BSC		
E	9.00 BSC		
E1	7.00 BSC		
e	0.50 BSC		
L	0.45	0.60	0.75
L1	1.00 REF		
θ	0°	3.5°	7°

Note:

1. All dimensions refer to JEDEC OUTLINE MS-012.
2. Do not include Mold Flash or Protrusions.
3. Unit: mm.

8.2. TSSOP28(T028)

8.2.1. Package Dimensions

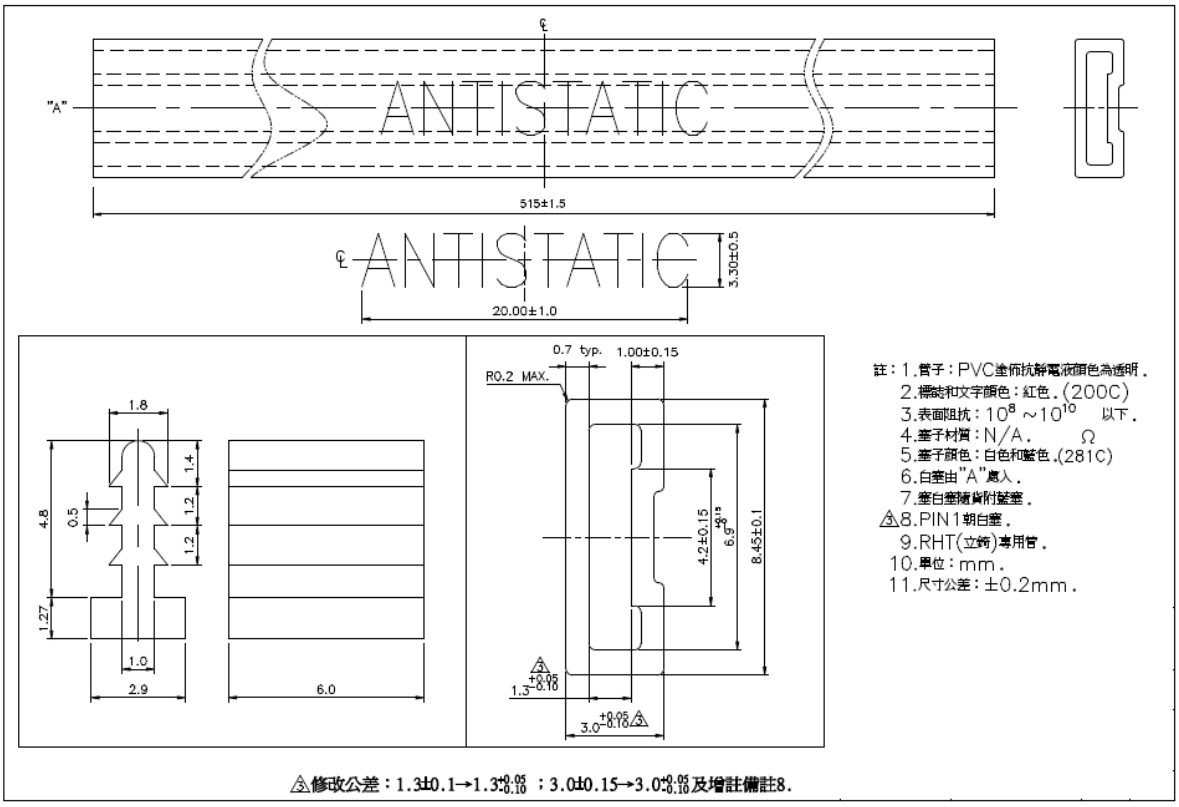


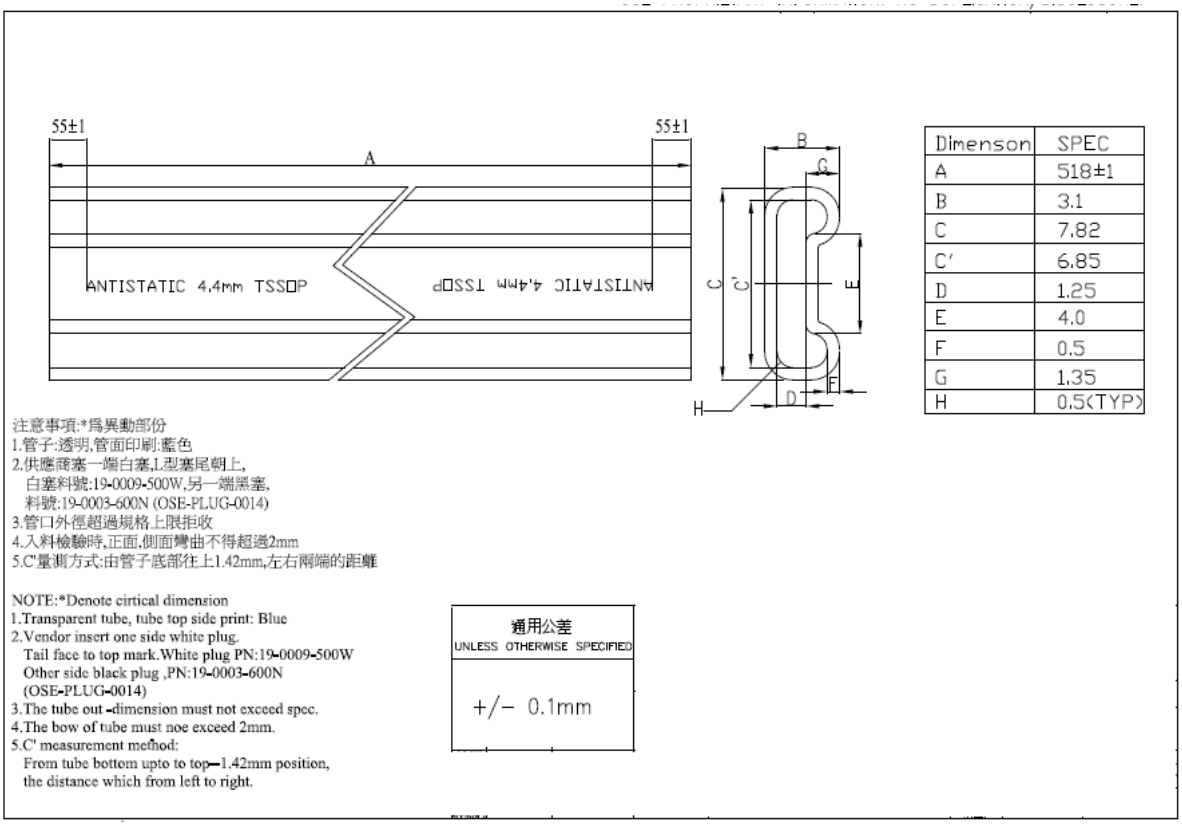
SYMBOLS	MIN.	NOM.	MAX.
A	–	–	1.20
A1	0.00	–	0.15
A2	0.80	1.00	1.05
b	0.19	–	0.30
D	9.60	9.70	9.80
E1	4.30	4.40	4.50
E	6.40 BSC		
e	0.65 BSC		
L1	1.00 REF		
L	0.45	0.60	0.75
S	0.20	–	–
θ	0°	–	8°

Note:

1. All dimensions refer to JEDEC OUTLINE MO-153.
2. Do not include Mold Flash or Protrusions.
3. Unit: mm.

8.2.2. Tube Information

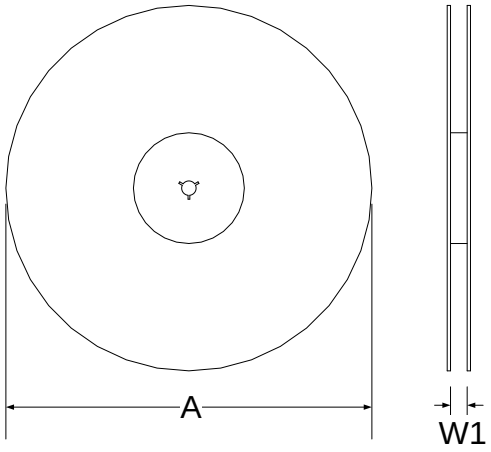




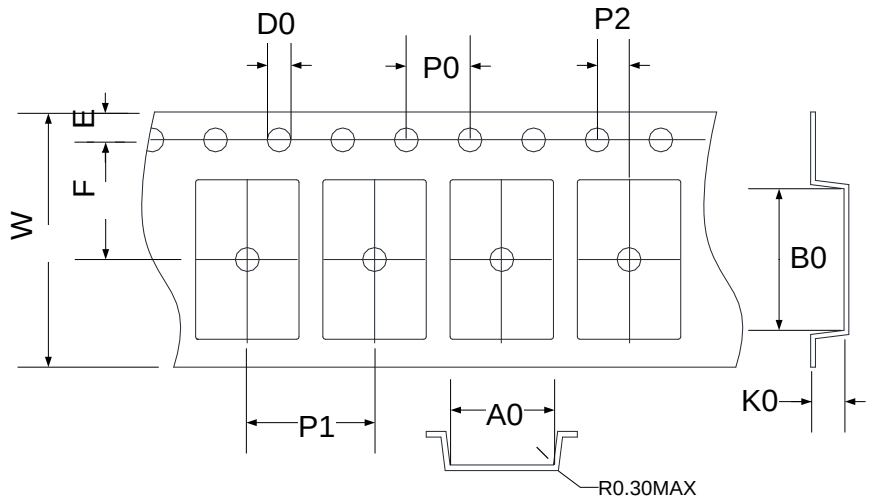
Dimenson	SPEC
A	518±1
B	3.1
C	7.82
C'	6.85
D	1.25
E	4.0
F	0.5
G	1.35
H	0.5(TYP)

8.2.3. Tape & Reel Information

8.2.3.1. Reel Dimensions



8.2.3.2. Carrier Tape Dimensions

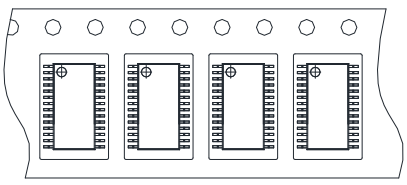


SYMBOLS	Reel Dimensions		Carrier Tape Dimensions									
	A	W1	A0	B0	K0	P0	P1	P2	E	F	D0	W
Spec.	330	16.5	6.80	10.20	1.60	4.00	8.00	2.00	1.75	7.50	1.50	16.00
Tolerance	+6/-3	+1.5/-0	±0.10	±0.10	±0.10	±0.10	±0.10	±0.10	±0.10	±0.10	+0.1/-0	±0.30

Unit : mm

Note: 10 Sprocket hole pitch cumulative tolerance is ±0.20mm.

8.2.3.3. Pin1 direction



9. 附錄 A

9.1. HY15P 系列產品差異比較表

ITEM	HY15P43	HY15P53
Display Mode	LED Mode only	LCD/LED Mode
COM port, sink current (VDD=4V)	40mA	20mA

10. 修訂記錄

以下描述本文件差異較大的地方，而標點符號與字形的改變不在此描述範圍。

版本	頁數	變更摘要	修訂日期
V01	ALL	初版發行	2016/03/30
V02	7	修改 TSSOP28 引腳圖	2016/06/30
	8 ~ 10	修改 TSSOP28 引腳定義與說明	
V03	P15, P17	1. 統一「LCD 倍壓電路控制器」名稱為 ENLCP。 2. 統一「SD18 啓用控制器」名稱為 ENAD1。	2016/08/12
	P17, P29	1. VREGN 只能設為 0b = x1。 2. VRH 只能設為 0b = AI2。	
	P23	統一「電源干擾復位旗標」名稱為 BOR。	