HY11P32
Datasheet

8-Bit RISC-like Mixed Signal Microcontroller
Embedded 4x12 LCD Driver
18-Bit ΣΔADC

目錄

注意：

1、 本說明書中的內容，隨著產品的改進，有可能不經過預告而更改。請客戶及時到本公司網站下載更新 http://www.hycontek.com

2、 本規格書中的圖形、應用電路等，因第三方工業所有權引發的問題，本公司不承擔其責任。

3、 本產品在單獨應用的情況下，本公司保證它的性能、典型應用和功能符合說明書中的條件。當使用在客戶的產品或設備中，以上條件我們不作保證，建議客戶做充分的評估和測試。

4、 請注意輸入電壓、輸出電壓、負載電流的使用條件，使 IC 內的功耗不超過封裝的容許功耗。對於客戶在超出說明書中規定額定值使用產品，即使是瞬間的使用，由此所造成的損失，本公司不承擔任何責任。

5、 本產品雖內置防靜電保護電路，但請不要施加超過保護電路性能的過大靜電。

6、 本規格書中的產品，未經書面許可，不可使用在要求高可靠性的電路中。例如健康醫療器械、防災器械、車輛器械、車載器械及航空器械等對人體產生影響的器械或裝置，不得作為其部件使用。

7、 本公司一直致力於提高產品的品質和可靠度，但所有的半導體產品都有一定的失效概率，這些失效概率可能會導致一些人身事故、火災事故等。當設計產品時，請充分留意冗餘設計，採用安全指標，這樣可以避免事故的發生。

8、 本規格書中內容，未經本公司許可，嚴禁用於其他目的之轉載或複製。

1. 特點

- 8 位元精簡指令集，共有 46 個指令
- 2.2V to 3.6V 工作電壓範圍，-40~85℃工作溫度範圍.
- 內部高精度 RC 震盪器，4 種 CPU 工作時脈切換選擇，可讓使用者達到最佳省電規劃.
  - 運行模式 300uA@2MHz
  - 待機模式 3uA@28KHz
  - 休眠模式 1uA
- 2KWord OTP (One Time Programmable) Type 程式記憶體，128Byte 資料記憶體
- Brownout detector 及 Watch dog Timer，可防止 CPU 進入死機模式.
- 18bit 全差動輸入 ΣΔADC 類比數位轉換器
  - 內置 PGA (Programmable Gain Amplifier) 及可有 1/4、1/2、1. …..128 倍 10 種輸入信號放大倍率選擇
  - 內置輸入零點調整，可針對不同應用增加其量測範圍
- 1.0V 的內部類比電路共地電壓源，具有 Push-Pull 驅動能力，可提供傳感器驅動電壓
- LVD 低電壓檢測功能具 14 段檢測電壓設置與外部輸入電壓檢測功能
- 類比電壓源 VDDA 具 10mA 穩壓電壓源輸出能力
- 4x12 LCD 液晶驅動器
  - 1/4 Duty、1/3 Bias
  - 內建 Charge Pump 穩壓線路，可提供 4 種 LCD 偏壓
- 8-bit Timer A
- Build-In EPROM (BIE)
- Support 6 stack level

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2. 引腳定義

2.1 LQFP44 引腳圖

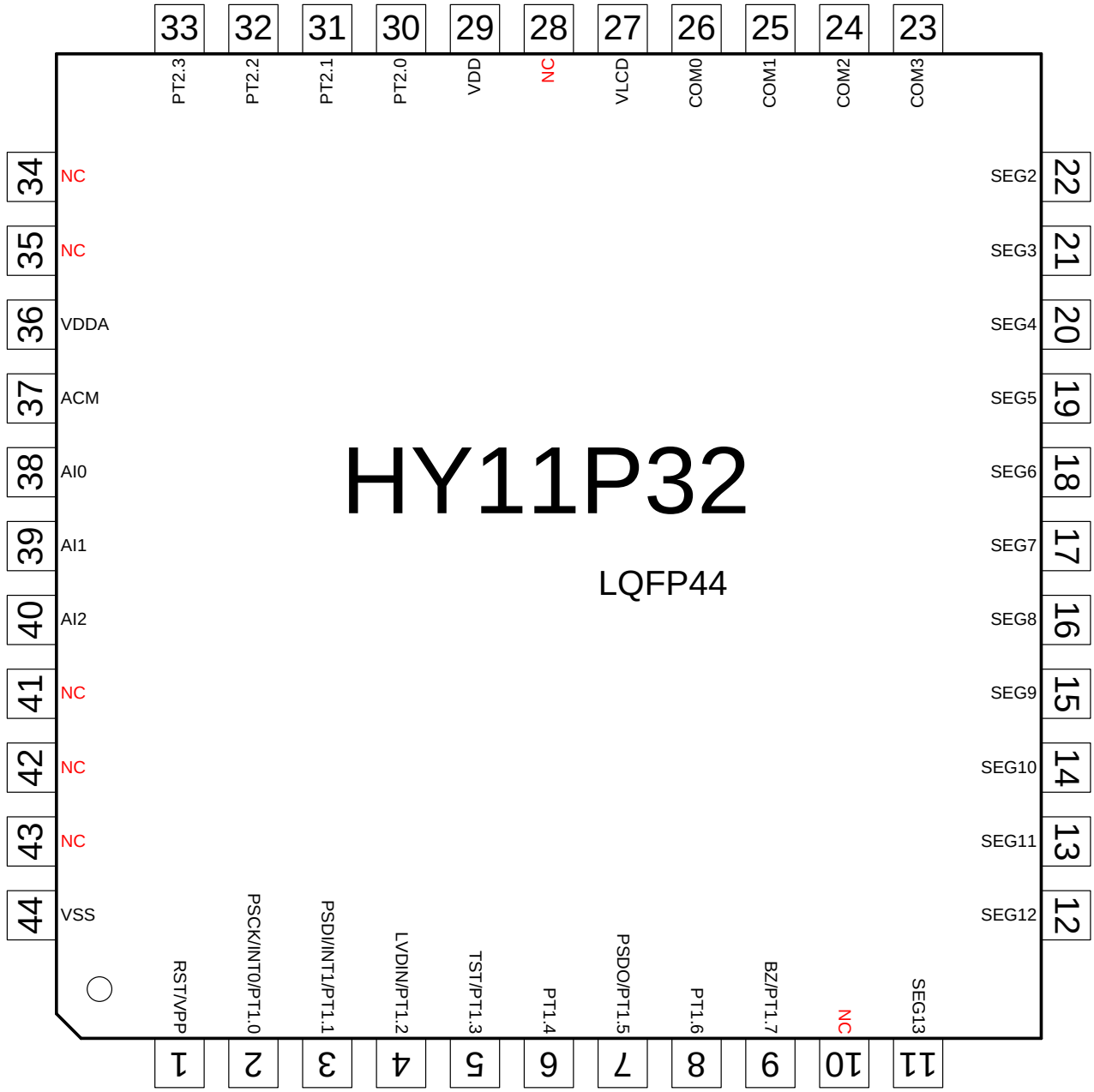


圖 2-1 HY11P32 LQFP44 引腳圖

註 1：VPP 與 RST 復用同一接口，非燒錄 EPROM 時禁止輸入電壓超過 5.8V

註 2：TST 與 PT1.3 復用同一接口，操作時禁止輸入電壓超過 Vdd+0.3V

註 3：若不將 PT1.3 設定成外部引腳按鍵，可以提升抗干擾能力

2.2 LQFP48 引腳圖

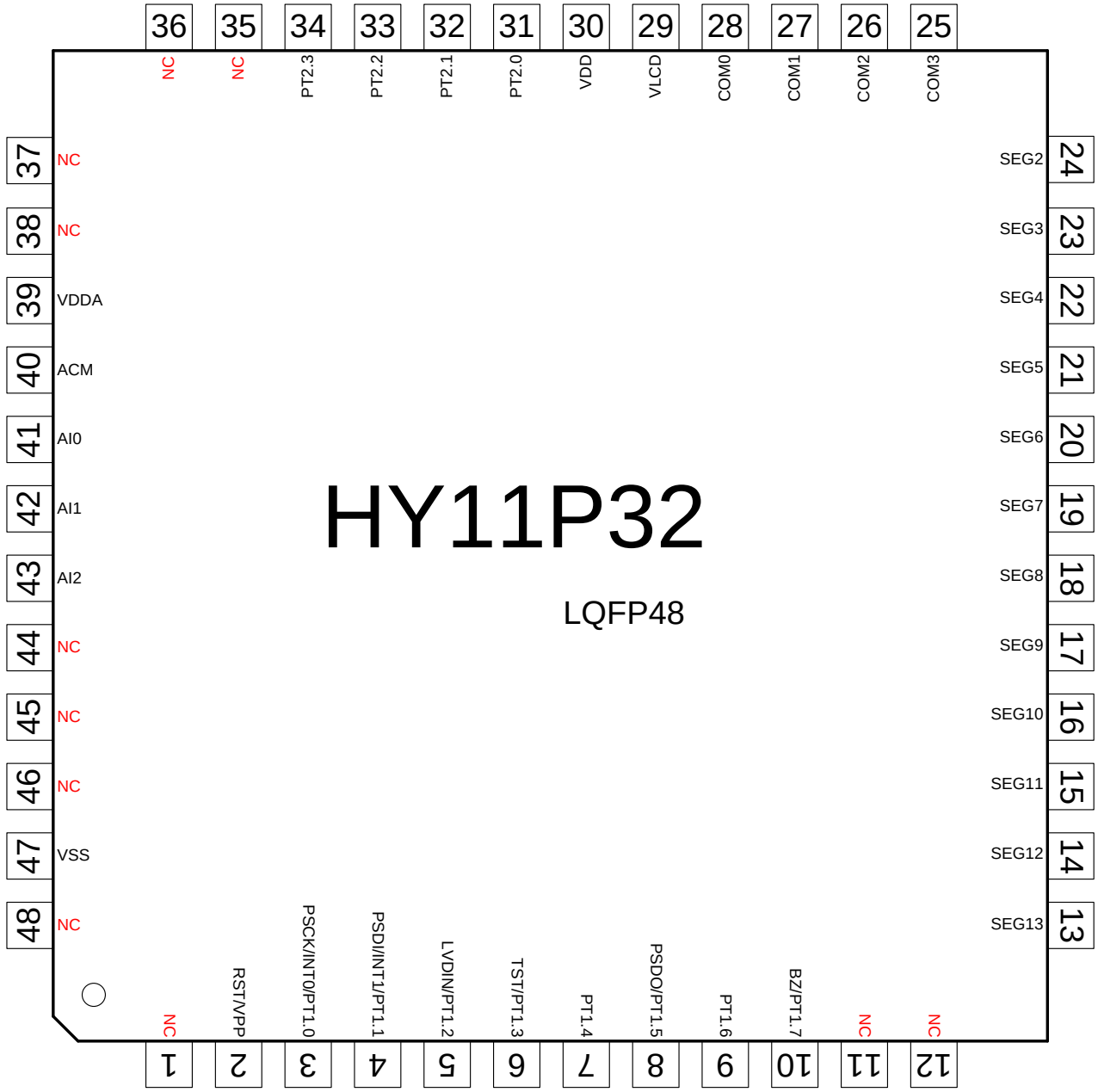


圖 2-1 HY11P32 LQFP48 引腳圖

註 1：VPP 與 RST 復用同一接口，非燒錄 EPROM 時禁止輸入電壓超過 5.8V

註 2：TST 與 PT1.3 復用同一接口，操作時禁止輸入電壓超過 Vdd+0.3V

註 3：若不將 PT1.3 設定成外部引腳按鍵，可以提升抗干擾能力

2.3 I/O 定義與說明(LQFP44)

"I/O"輸入/輸出,"I"輸入,"O"輸出,"S"史密斯觸發,"C"CMOS 特性兼容輸出與輸入,"P"電壓源,"A"類比通道

編號	引腳名稱	引腳特性		功能說明
		格式	緩衝	
1	RST/VPP			
	RST	I	S	復位晶片
	VPP	P	P	EPROM 讀/寫時的電壓源
2	PT1.0/INT0/PSCK			
	PT1.0	I	S	數位輸入
	INT0	I	S	中斷源 INT0
	PSCK	I	S	OTP 讀/寫介面 SCK 接口
3	PT1.1/INT1/PSDI			
	PT1.1	I	S	數位輸入
	INT1	I	S	中斷源 INT1
	PSDI	I	S	OTP 讀/寫介面 SDI 接口
4	PT1.2/LVDIN			
	PT1.2	I	S	數位輸入
	LVDIN	A	A	LVD 外部信號輸入接口
5	PT1.3/TST			
	PT1.3	I	S	數位輸入
	TST	I	S	測試模式致能輸入（未開放）
6	PT1.4	I/O	S	數位輸入/輸出
7	PT1.5/PSDO			
	PT1.5	I/O	S	數位輸入/輸出
	PSDO	O	C	OTP 讀/寫介面 SDO 接口
8	PT1.6	I/O	S	數位輸入/輸出
9	PT1.7/BZ			
	PT1.7	I/O	S	數位輸入/輸出
	BZ	O	C	蜂鳴器輸出端
10	NC	-	-	未使用
11	SEG13	O	A	LCD 的 Segment 輸出
12	SEG12	O	A	LCD 的 Segment 輸出
13	SEG11	O	A	LCD 的 Segment 輸出
14	SEG10	O	A	LCD 的 Segment 輸出
15	SEG9	O	A	LCD 的 Segment 輸出
16	SEG8	O	A	LCD 的 Segment 輸出

17	SEG7	O	A	LCD 的 Segment 輸出
18	SEG6	O	A	LCD 的 Segment 輸出
19	SEG5	O	A	LCD 的 Segment 輸出
20	SEG4	O	A	LCD 的 Segment 輸出
21	SEG3	O	A	LCD 的 Segment 輸出
22	SEG2	O	A	LCD 的 Segment 輸出
23	COM3	O	A	LCD 的 COM 輸出
24	COM2	O	A	LCD 的 COM 輸出
25	COM1	O	A	LCD 的 COM 輸出
26	COM0	O	A	LCD 的 COM 輸出
27	VLCD	P	P	LCD 的電壓源
28	NC	-	-	未使用
29	VDD	P	P	晶片工作電壓源
30	PT2.0	I/O	S	數位輸入/輸出
31	PT2.1	I/O	S	數位輸入/輸出
32	PT2.2	I/O	C	數位輸入/輸出
33	PT2.3	I/O	S	數位輸入/輸出
34	NC	-	-	未使用
35	NC	-	-	未使用
36	VDDA	P	P	穩壓器輸出，類比電路電壓源
37	ACM	P	P	內部類比電路共地引腳
38	AI0	A	A	類比輸入通道
39	AI1	A	A	類比輸入通道
40	AI2	A	A	類比輸入通道
41	NC	-	-	未使用
42	NC	-	-	未使用
43	NC	-	-	未使用
44	VSS	P	P	晶片工作電壓源接地端

表 2-1 引腳定義與功能說明

3. 應用電路

3.1 橋式感測器 I

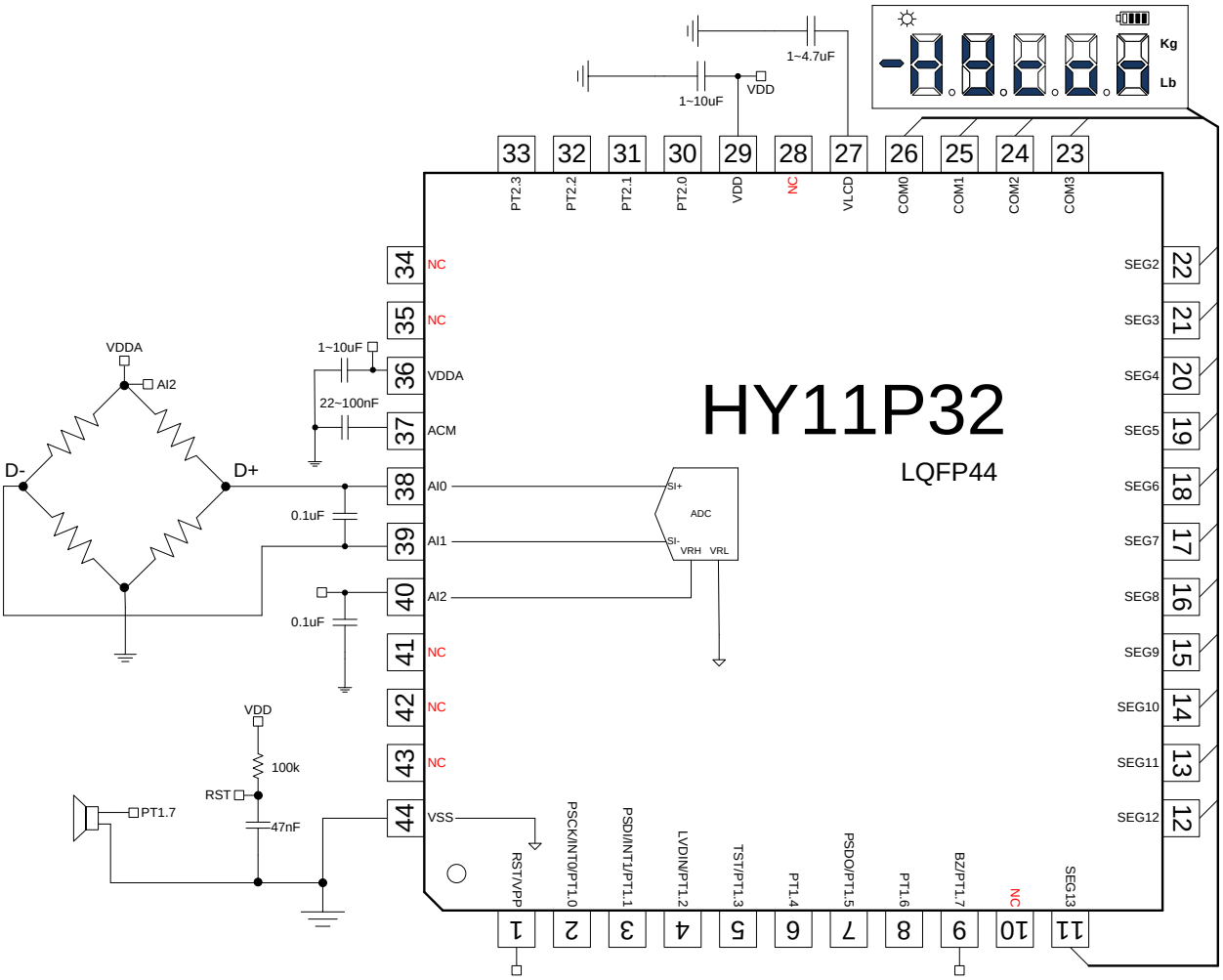


圖 3-1 橋式感測器應用電路

註：Load Cell 零點電壓位置可透過 DCSET[2:0] 進行偏壓調整。

4. 功能概述

4.1 內部方塊圖

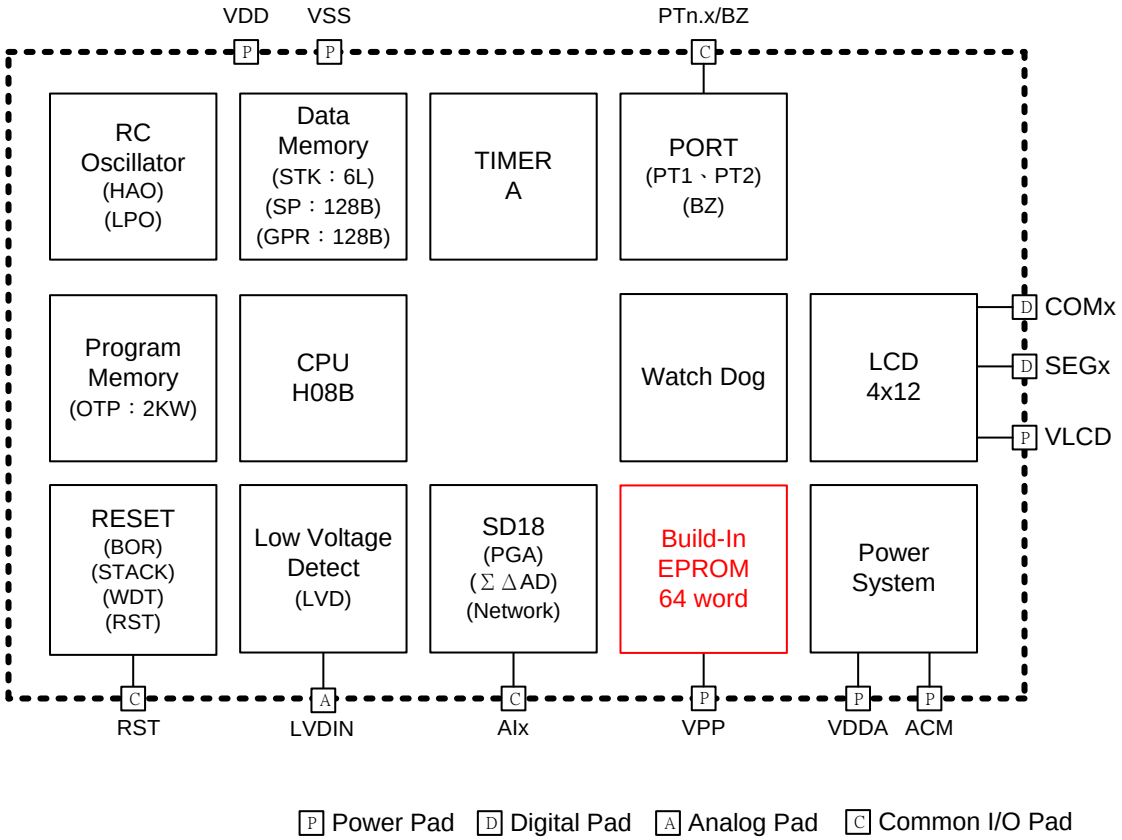


圖 4-1 HY11P32 內部方塊圖

4.2 相關說明與支援文件

晶片功能相關使用說明書

DS-HY11P32-Vxx	HY11P32 說明書
UG-HY11S14-Vxx	HY11Pxx 系列使用說明書
APD-CORE003-Vxx	H08B 指令說明書

開發工具相關使用說明書

APD-HYIDE006-Vxx	HY11xxx 系列開發工具軟體使用說明書
APD-HYIDE005-Vxx	HY11xxx 系列開發工具硬體使用說明書
APD-OTP001-Vxx	OTP 產品燒錄引腳說明書

產品生產相關使用說明書

APD-HYIDE004-Vxx	HY1xxxx 系列生產線專用燒錄器說明書
BDI-HY11P32-Vxx	HY11P32 個別產品的裸片打線資訊

4.3 SD18 Network

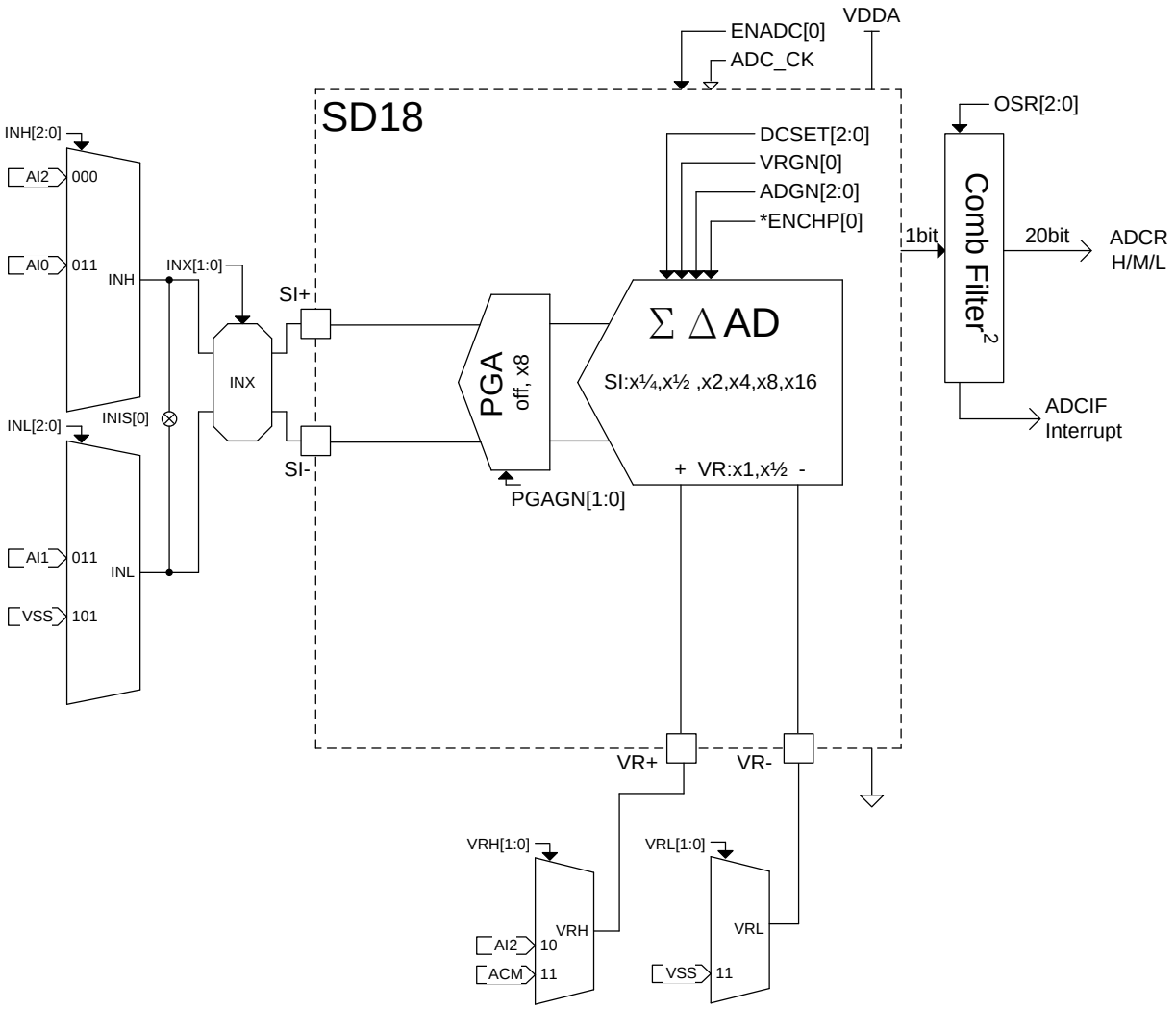


圖 4-2 SD18 Network

5. 暫存器列表

Register File Summary for H08B

"-"no use,"*"read/write,"w"write,"r"read,"r0"only read 0,"r1"only read 1,"w0"only write 0,"w1"omly write 1
"."unimplemented bit,"x"unknown,"u"unchanged,"d"depends on condition

Address	File Name	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	A-RESET	i-RESET	R/W
00H	INDF0	Contents of FSR0 to address data memory -value of FSR0 not changed								N/A	N/A	*,*,*,*,*,*,*,*
10H	FSR0L	Indirect Data Memory Address Pointer 0 Low Byte,FSR0[7:0]								xxxx xxxx	uuuu uuuu	*,*,*,*,*,*,*,*
18H	STKPTR	STKFL	STKUN	STKOV			STKPRT[2:0]			000. .000	000. .000	r,rw0,rw0,- -,r,r,r
1AH	PCLATH						PC[10]	PC[9]	PC[8]	.... .000	.... .000	-,-,-,- -,*,*,*
1BH	PCLATL	PC Low Byte for PC<7:0>								0000 0000	0000 0000	*,*,*,*,*,*,*,*
1CH	BIECTRL					VPP_HIGH		BIEWR	BIERD	1000 d000	1000 d000	-,-,-,- *,r0,*,*
1EH	BIEPTRL	0	0	BIE_ADDR[5:0]						0000 0000	0000 0000	w0,w0,*,*,*,*,*,*
1FH	BIEDH	BIE_DATA[15:8]								xxxx xxxx	xxxx xxxx	*,*,*,*,*,*,*,*
20H	BIEDL	BIE_DATA[7:0]								xxxx xxxx	xxxx xxxx	*,*,*,*,*,*,*,*
23H	INTE1	GIE	ADCIE			TMAIE	WDTIE	E1IE	E0IE	0000 0000	0000 0000	*,*,r0,r0 *,*,*,*
26H	INTF1		ADCIF			TMAIF	WDTIF	E1IF	E0IF	.000 0000	.000 0000	-,*,r0,r0 *,*,*,*
29H	WREG	Working Register								xxxx xxxx	uuuu uuuu	*,*,*,*,*,*,*,*
2BH	STATUS				C				Z	xxxx xxxx	xxxx xxxx	-,-,-,* -,-,-,*
2CH	Pstatus	PD	TO	IDLEB	BOR		SKERR			000d xxxx	000d xxxx	rw0,rw0,rw0,rw0 x,x,x,x
2DH	LVDCN		LVDFG	LVD	LVDON	**VLDX[3:0]**				x000 0000	x000 0000	x,*,r,r *,*,*,*
30H	PWRCN	ENVDDA	**VDDAX[1:0]=11**		ENACM					0xx0 xxxx	0xx0 xxxx	*,r,r,* x,x,x,x
31H	MCKCN1	ADCS[2:0]			ADCCK			ENXT=0	ENHAO	0000 0001	0000 0001	*,*,*,* r0,r0,r0,*
32H	MCKCN2			**LSCK=0**	**HSCK=0**	**HSS[1:0]=00**		CPUCK[1:0]		..00 0000	..00 0000	r0,r0,r0,r0 r0,r0,*,*
33H	MCKCN3	LCDS[2:0]				PERCK	BZS[2:0]			000. 0000	000. 0000	*,*,*,r0 *,*,*,*
39H	ADCRH	ADC conversion memory HighByte								xxxx xxxx	uuuu uuuu	r,r,r,r r,r,r,r
3AH	ADCRM	ADC conversion memory Middle Byte								xxxx xxxx	uuuu uuuu	r,r,r,r r,r,r,r
3BH	ADCRL	ADC conversion memory Low Byte								xxxx xxxx	uuuu uuuu	r,r,r,r r0,r0,r0,r0
3CH	ADCCN1	ENADC		ENCHP	**PGAGN[1:0]=00 or 11**		ADGN[2:0]			0000 0000	0000 0000	*,r0,*,*,*,*,*,*
3DH	ADCCN2			INBUF=0	VRBUF=0	VREGN	DCSET[2:0]			0000 0000	0000 0000	r0,r0,r0,r0 *,*,*,*
3EH	ADCCN3	OSR[2:0]								0000 0000	0000 0000	*,*,*,r0 r0,r0,r0,r0
3FH	AINET1	**INH[2:0]=XX0 or XX1(AI2 or AI0)**			**INL[2:0]=0XX or 1XX(AI1 or VSS)**			INIS		xx00 xx0x	xx00 xx0x	x,x,*,* x,x,*,x
40H	AINET2		**VRH[1:0]=X0 or X1(AI2 or ACM)**		INX[1:0]		**VRL[1:0]=11(VSS)**			xx00 0xxx	xx00 0xxx	x,x,*,* *,x,x,x
41H	TMACN	ENTMA	TMACK	TMAS[1:0]		ENWDT	WDTS[2:0]			0000 0000	0000 0000	*,*,*,* w1,*,*,*
42H	TMAR	TimerA data register								xxxx xxxx	uuuu uuuu	r,r,r,r r,r,r,r
52H	LCDCN1	ENLCD	LCDPR	VLCDX[1:0]		LCDBF	**LCDBI[1:0]=10**			0000 0xxx	0000 0xxx	*,*,*,* *,x,x,x
53H	LCDCN2	LCDBL	**LCDMX[1:0]=11**							0xxx xxxx	0xxx xxxx	*,x,x,x x,x,x,x
54H	LCD0	Segment SEG2@[3:0] and SEG3@[7:4] data register of LCD0								xxxx xxxx	uuuu uuuu	*,*,*,*,*,*,*,*
55H	LCD1	Segment SEG4@[3:0] and SEG5@[7:4] data register of LCD1								xxxx xxxx	uuuu uuuu	*,*,*,*,*,*,*,*
56H	LCD2	Segment SEG6@[3:0] and SEG7@[7:4] data register of LCD2								xxxx xxxx	uuuu uuuu	*,*,*,*,*,*,*,*
57H	LCD3	Segment SEG8@[3:0] and SEG9@[7:4] data register of LCD3								xxxx xxxx	uuuu uuuu	*,*,*,*,*,*,*,*
58H	LCD4	Segment SEG10@[3:0] and SEG11@[7:4] data register of LCD4								xxxx xxxx	uuuu uuuu	*,*,*,*,*,*,*,*
59H	LCD5	Segment SEG12@[3:0] and SEG13@[7:4] data register of LCD5								xxxx xxxx	uuuu uuuu	*,*,*,*,*,*,*,*
6DH	PT1	PT1.7	PT1.6	PT1.5	PT1.4	PT1.3	PT1.2	PT1.1	PT1.0	xxxx xxxx	uuuu uuuu	*,*,*,* r,r,r,r
6EH	TRISC1	TC1.7	TC1.6	TC1.5	TC1.4					0000 0000	0000 0000	*,*,*,* r0,r0,r0,r0
70H	PT1PU	PU1.7	PU1.6	PU1.5	PU1.4	PU1.3	PU1.2	PU1.1	PU1.0	0000 0000	0000 0000	*,*,*,*,*,*,*,*
71H	PT1M1					INTEG1[1:0]		INTEG0[1:0]		0000 0000	0000 0000	r0,r0,r0,r0 *,*,*,*
72H	PT1M2		PM1.7[0]							0000 0000	0000 0000	r0,*,r0,r0 r0,r0,r0,r0
74H	PT2					PT2.3	PT2.2	PT2.1	PT2.0	 xxxx	.... uuuu	x,x,x,x *,*,*,*
75H	TRISC2					TC2.3	TC2.2	TC2.1	TC2.0	 0000	 0000	x,x,x,x *,*,*,*
77H	PT2PU					PU2.3	PU2.2	PU2.1	PU2.0	 0000	 0000	x,x,x,x *,*,*,*
80H ~ FFH		GENERAL PURPOSE REGISTER @ 128Byte								xxxx xxxx	uuuu uuuu	*,*,*,*,*,*,*,*

圖 5-1 HY11P32 暫存器列表

6. 電氣特性

Absolute maximum ratings over operating free-air temperature (unless otherwise noted)

Voltage applied at V_{DD} to V_{SS} . . . . −0.2 V to 4.0 V

Voltage applied to any pin . . . . −0.2 V to V_{DD} + 0.3 V

Voltage applied to RST/VPP pin . . . . −0.2 V to 6.9 V

Voltage applied to TST/PT1.3 pin . . . . −0.2 V to V_{DD} + 1 V

Diode current at any device terminal . . . . ±2 mA

Storage temperature, Tstg: (unprogrammed device) . . . . −55℃ to 150℃

(programmed device) . . . . −40℃ to 85℃

Total power dissipation. 0.5w

Maximum output current sink by any PORT1 to PORT2 I/O pin. 25mA

6.1 Recommended operating conditions

T_A = -40℃ ~ 85℃,unless otherwise noted

Sym.	Parameter	Test Conditions	Min.	Typ.	Max.	unit
V_{DD}	Supply Voltage	All digital peripherals and CPU	2.2		3.6	V
		Analog peripherals	2.4		3.6	
V_{SS}	Supply Voltage		0		0	

6.2 Internal RC Oscillator

T_A = 25℃,V_{DD} = 3.0V,unless otherwise noted

Sym.	Parameter	Test Conditions	Min.	Typ.	Max.	unit
HAO	High Speed Oscillator frequency	ENHAO[0]=1	1.6	2.0	2.4	MHz
LPO	Low Power Oscillator frequency	V_{DD} supply voltage be enable LPO	22	28	35	KHz

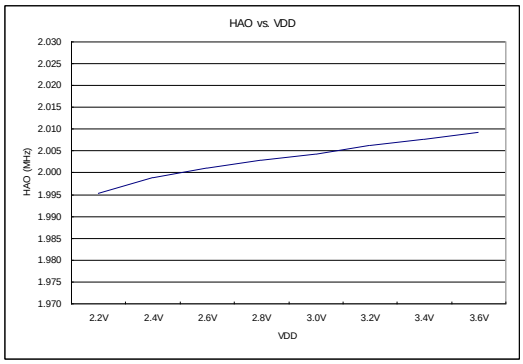


Figure 6.2-1 HAO vs. VDD

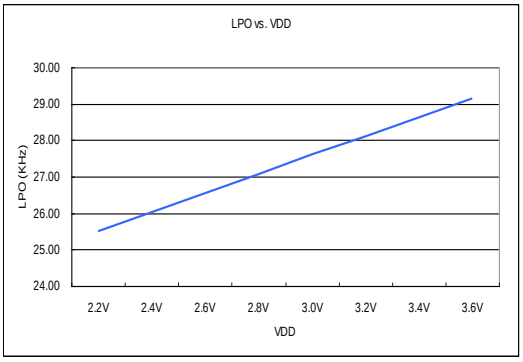


Figure 6.2-2 LPO vs. VDD

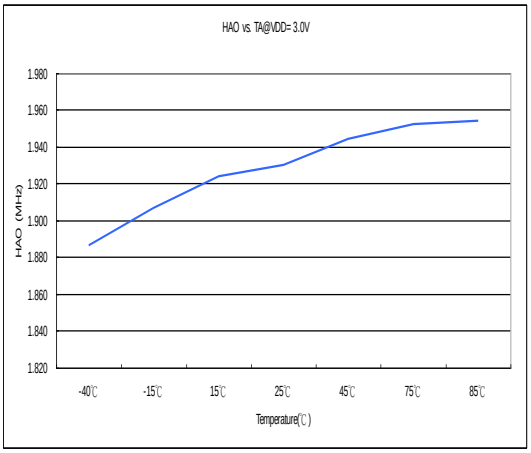


Figure 6.2-3 HAO vs. Temperature

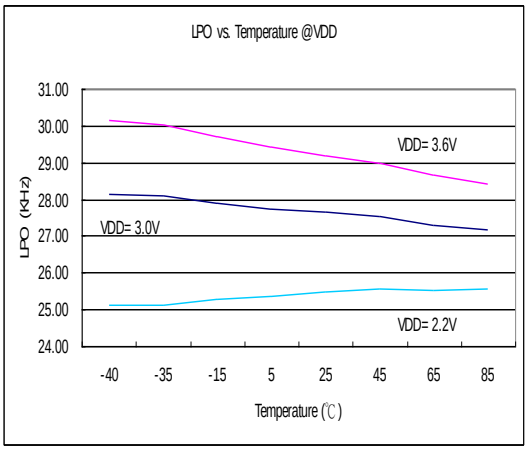


Figure 6.2-4 LPO vs. Temperature

6.3 Supply current into VDD excluding peripherals current

T_A = 25℃,V_{DD} = 3.0V,OSC_LPO = 28KHz,unless otherwise noted

Sym.	Parameter	Test Conditions	Min.	Typ.	Max.	unit
I_{AM2}	Active mode 2	OSC_CY = off, OSC_HAO = 2MHz, CPU_CK = 2MHz		0.28	0.55	mA
I_{AM3}	Active mode 3	OSC_CY = off, OSC_HAO = 2MHz, CPU_CK = 1MHz		0.165	0.3	mA
I_{LP2}	Low Power 2	OSC_CY = off, OSC_HAO = off, CPU_CK = LPO, Idle state		1.65	3	uA
I_{LP3}	Low Power 3	OSC_CY = off, OSC_HAO = off, CPU_CK = off, Sleep state		0.65	1.2	uA

OSC_HAO：Internal High Accuracy Oscillator frequency.

CPU_CK：CPU core work frequency.

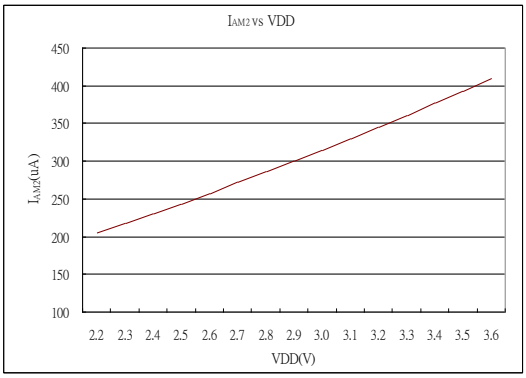


Figure 6.3-1 I_{AM2} vs. VDD

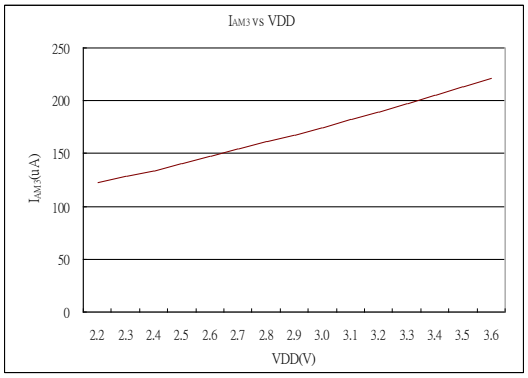


Figure 6.3-2 I_{AM3} vs. VDD

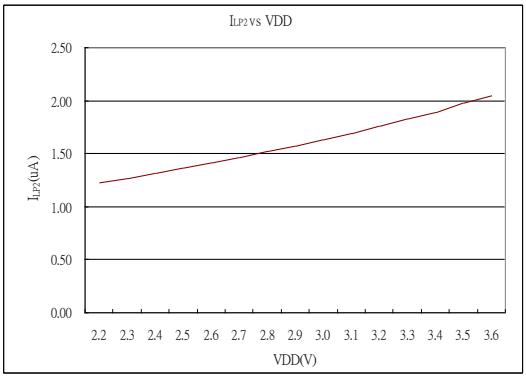


Figure 6.3-3 I_{LP2} vs. VDD

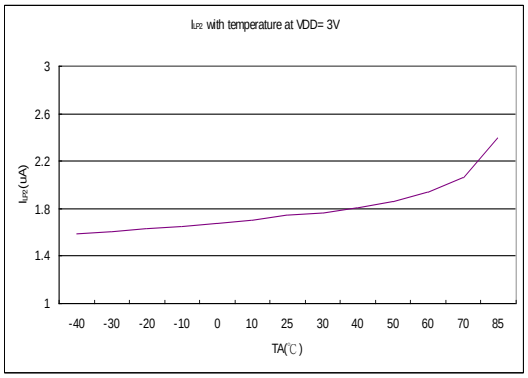


Figure 6.3-4 I_{LP2} vs. Temperature

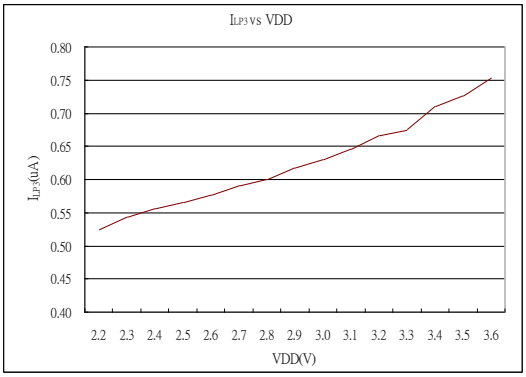


Figure 6.3-5 I_{LP3} vs. VDD

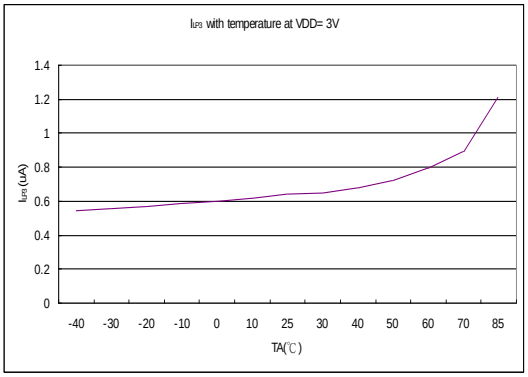


Figure 6.3-6I_{LP3} vs. Temperature

6.4 Port1~2

T_A = 25℃,V_{DD} = 3.0V,unless otherwise noted

Sym.	Parameter	Test Conditions	Min.	Typ.	Max.	unit
Input voltage and Schmitt trigger and leakage current and timing						
V_{IH}	High-Level input voltage				2.1	V
V_{IL}	Low-Level input voltage		0.9			
V_{hys}	Input Voltage hysteresis(VIH - VIL)			0.8		V
I_{LKG}	Leakage Current				0.1	uA
R_{PU}	Port pull high resistance			180		kΩ
Output voltage and current and frequency						
V_{OH}	High-level output voltage	I_{OH}=10mA	V_{DD} -0.3			V
V_{OL}	Low-level output voltage	I_{OL}=-10mA			VSS +0.3	

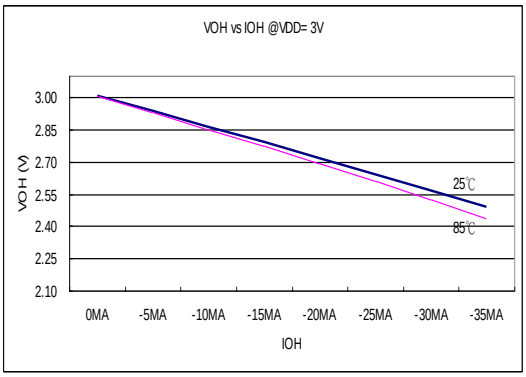


Figure 6.4-1 V_{OH} vs. I_{OH} @VDD=3.0V

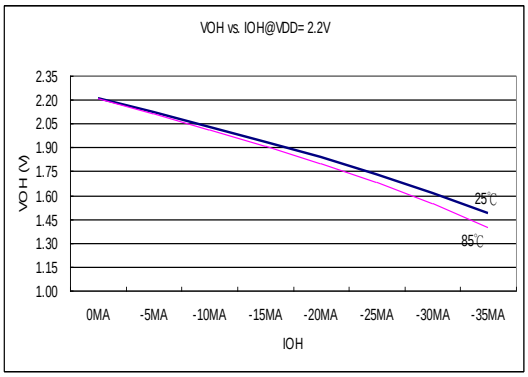


Figure 6.4-2 V_{OH} vs. I_{OH} @VDD=2.2V

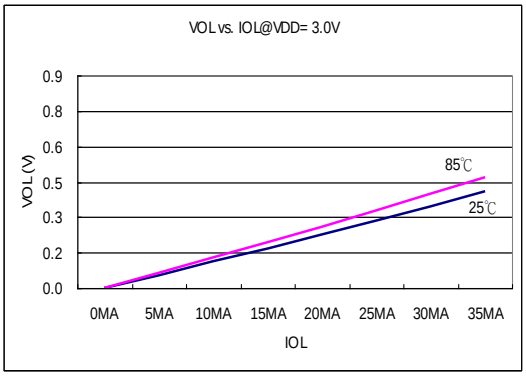


Figure 6.4-3 V_{OL} vs. I_{OL}@VDD=3.0V

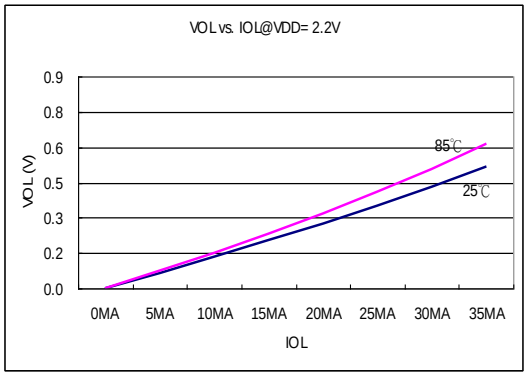


Figure 6.4-4 V_{OL} vs. I_{OL}@VDD=2.2V

6.5 Reset(Brownout, External RST pin, Low Voltage Detect)

T_A = 25℃,V_{DD} = 3.0V,unless otherwise noted

Sym.	Parameter	Test Conditions	Min.	Typ.	Max.	unit
BOR	Pulse length needed to accepted reset internally, t_{d-LVR}		2			us
	V_{DD} Start Voltage to accepted reset internally (L➔H),V_{LVR}		1.6	1.85	2.1	V
	Hysteresis, $V_{HYS-LVR}$			70		mV
RST	Pulse length needed as RST/VPP pin to accepted reset internally, t_{d-RST}		2			us
	Input Voltage to accepted reset internally		0.9			V
	Hysteresis, $V_{HYS-RST}$			0.8		V
LVD	Operation current, I_{LVD}			10	15	uA
	External input voltage to compare reference voltage			1.2		V
	Compare reference voltage temperature drift	T_A = -40℃ ~ 85 ℃		100		ppm/℃
	Detect V_{DD} voltage rang by user option, V_{SVS} VLDx[3:0]=1110b			3.3		V
	Detect V_{DD} voltage rang by user option, V_{SVS} VLDx[3:0]=1101b			3.2		
	Detect V_{DD} voltage rang by user option, V_{SVS} VLDx[3:0]=1100b			3.1		
	Detect V_{DD} voltage rang by user option, V_{SVS} VLDx[3:0]=1011b			3.0		
	Detect V_{DD} voltage rang by user option, V_{SVS} VLDx[3:0]=1010b			2.9		
	Detect V_{DD} voltage rang by user option, V_{SVS} VLDx[3:0]=1001b			2.8		
	Detect V_{DD} voltage rang by user option, V_{SVS} VLDx[3:0]=1000b			2.7		
	Detect V_{DD} voltage rang by user option, V_{SVS} VLDx[3:0]=0111b			2.6		
	Detect V_{DD} voltage rang by user option, V_{SVS} VLDx[3:0]=0110b			2.5		
	Detect V_{DD} voltage rang by user option, V_{SVS} VLDx[3:0]=0101b			2.4		
	Detect V_{DD} voltage rang by user option, V_{SVS} VLDx[3:0]=0100b			2.3		
	Detect V_{DD} voltage rang by user option, V_{SVS} VLDx[3:0]=0011b			2.2		
	Detect V_{DD} voltage rang by user option, V_{SVS} VLDx[3:0]=0010b			2.1		
	Detect V_{DD} voltage rang by user option, V_{SVS} VLDx[3:0]=0001b			2.0		

BOR：Brownout Reset

LVR：Low Voltage Reset of BOR

LVD：Low Voltage Detect

RST：External Reset pin

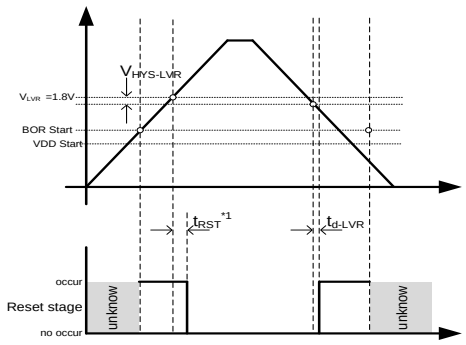


Figure6.5-1 BOR reset diagram

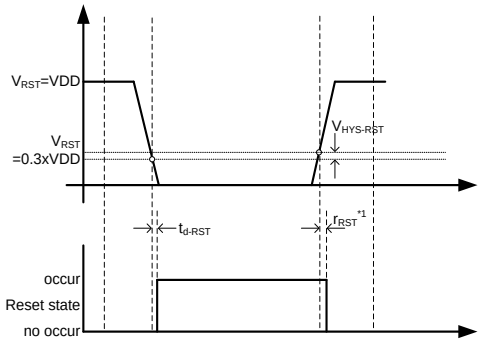


Figure6.5-2 RST reset diagram

*1 r_{RST}：Please see BOR Introduce of HY11Pxx series User's Guide (UG-HY11S14-Vxx).

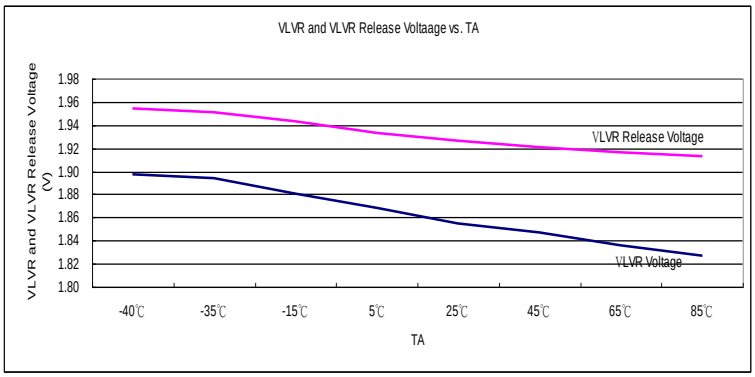


Figure6.5-3 LVR vs. Temperature

6.6 Power System

T_A = 25℃,V_{DD} = 3.0V,unless otherwise noted

Sym.	Parameter	Test Conditions		Min.	Typ.	Max.	unit
VDDA	VDDA operation current, I_{VDDA}	I_L = 0mA	VDDAX[1:0]=00b		22		uA
	Select VDDA output voltage	I_L = 0.1mA, VDD≧ VDDA+0.2V	VDDAX [1:0]=11b		2.4		V
	Dropout voltage	I_L = 10mA	VDDAX [1:0]=11b		180		mV
	Temperature drift	VDDAX [1:0]=11b	T_A=-40℃~85℃		50		ppm/℃
	V_{DD} Voltage drift	I_L = 0.1mA	V_{DD}=2.5V~3.6V		±0.2		%/V
ACM	ACM operation current, I_{ACM}	I_L = 0mA			20		uA
	Output voltage ,V_{ACM}	ENACM[0]=1	I_L = 0uA		1.0		V
	Output voltage with Load		I_L = ±200uA	0.98		1.02	V_{ACM}
	Temperature drift	ENACM[0]=1,	T_A=-40℃~85℃		50		ppm/℃
	VDDA Voltage drift	I_L = 10uA			100		uV/V
VDDA：Adjust Voltage Regulator ACM：Analog Common Mode Voltage							

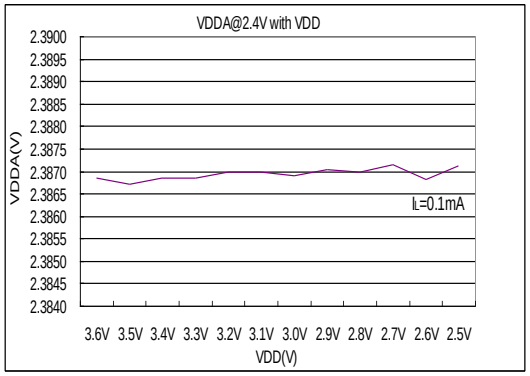


Figure6.6-1 VDDA I_L=0.1mA vs. VDD

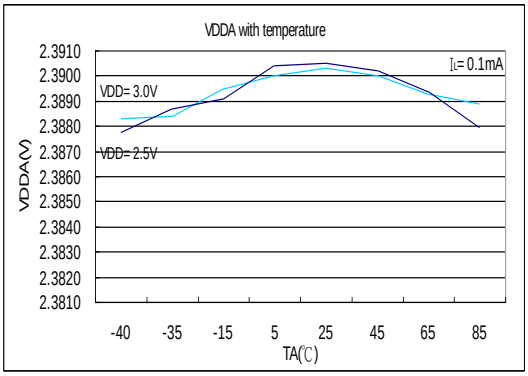


Figure6.6-2 VDDA I_L=0.1mA vs. Temperature

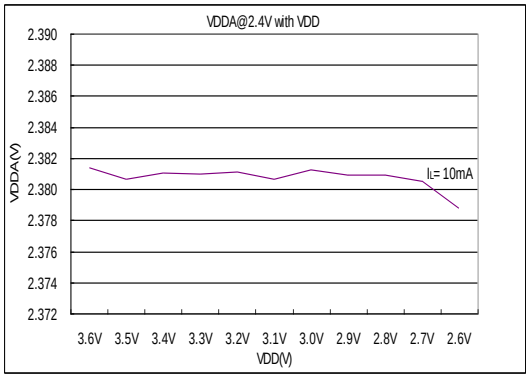


Figure6.6-3 VDDA I_L=10mA vs. VDD

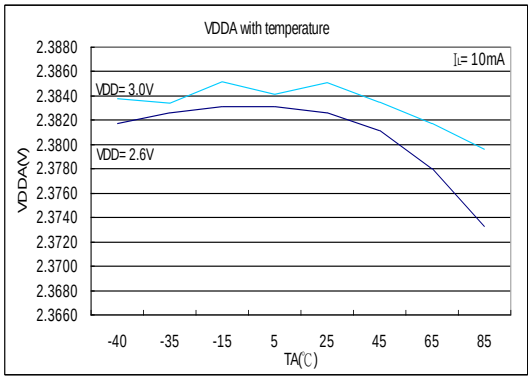


Figure6.6-4 VDDA I_L=10mA vs. Temperature

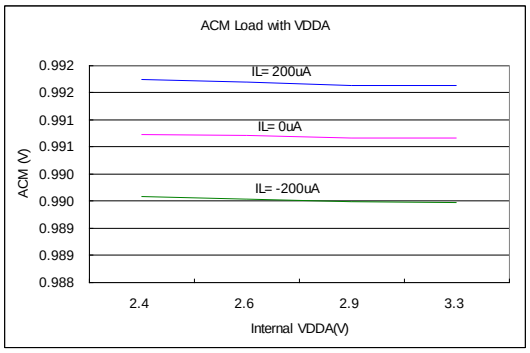


Figure6.6-5 ACM Load vs. VDDA

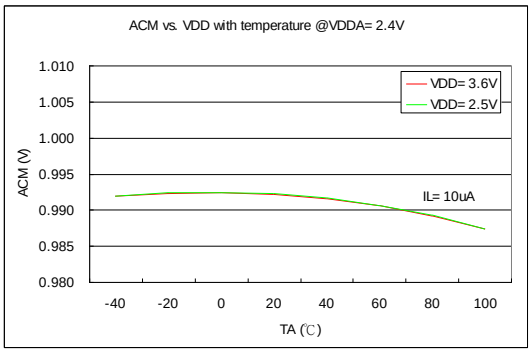


Figure6.6-6 ACM vs. Temperature

6.7 LCD

T_A = 25℃,V_{DD} = 3.0V, C_{VLCD} =4.7uF,unless otherwise noted.

Sym.	Parameter	Test Conditions		Min.	Typ.	Max.	unit
I_{LCD}	Operation supply current without output buffer.(all segment turn on)	LCDPR[0]=1	V_{DD} = 2.2V		20		uA
			V_{DD} = 3.0V				
VLCD	Supply Voltage at VLCD pin	LCDPR[0]=0		2.2		3.6	V
	Embedded Charge Pump output voltage at VLCD pin	V_{DD} = 2.2V, LCDPR[0]=1, C_{VLCD} =4.7uF	VLCDX[1:0]=11b	2.295	2.55	2.805	V
			VLCDX[1:0]=10b	2.52	2.8	3.08	
			VLCDX[1:0]=01b	2.745	3.05	3.355	
			VLCDX[1:0]=00b	2.97	3.3	3.63	
Z_{LCD}	Output impedance with LCD buffer	f_{LCD} =128Hz,VLCD=3.05V			10		kΩ

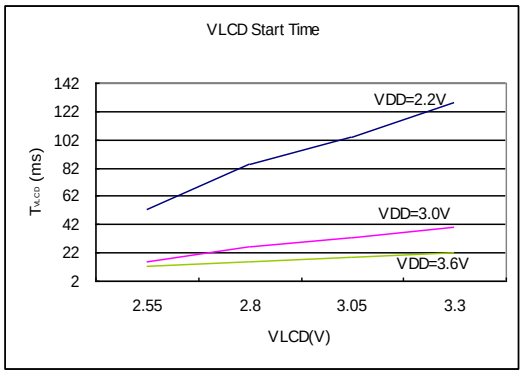


Figure6.7-1 LCD start time

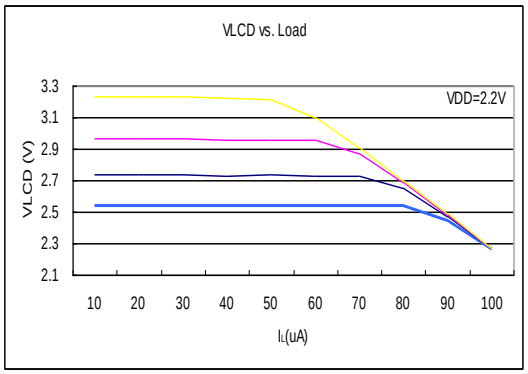


Figure6.7-2 VLCD vs. I_L @VDD=2.2V

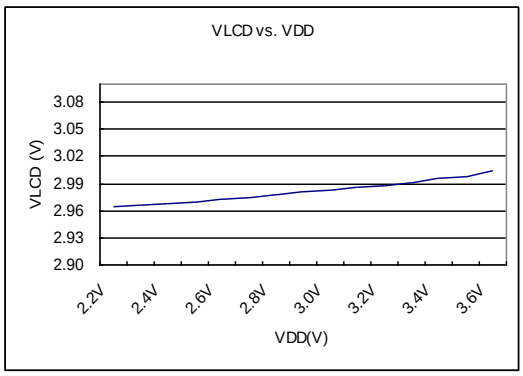


Figure6.7-3 VLCD vs. VDD

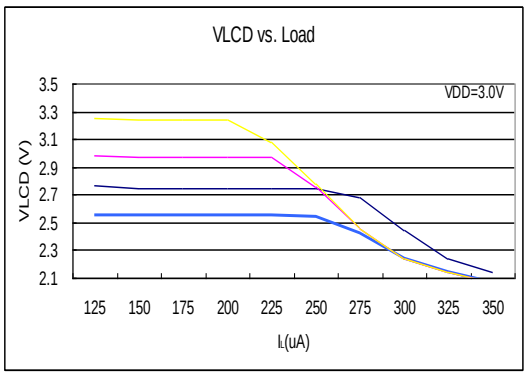


Figure6.7-4 VLCD vs. I_L @VDD=3.0V

6.8 SD18,Power Supply and recommended operating conditions

T_A = 25℃,V_{DD} = 3.0V, VDDA=2.4V,unless otherwise noted

Sym.	Parameter	Test Conditions		Min.	Typ.	Max.	unit
V_{SD18}	Supply Voltage at VDDA	ENVDDA[0]=0		2.4		3.6	V
f_{SD18}	Modulator sample frequency, ADC_CK			25	250	300	KHz
	Over Sample Ratio, OSR			256		32768	
I_{SD18}	Operation supply current without PGA	ENADC[0]=1 INBUF[0]=0,VRBUF[0]=0	GAIN =4, ADC_CK=250KHz		120		uA

6.8.1 PGA,Power Supply and recommended operating conditions

T_A = 25℃,V_{DD} = 3.0V, VDDA=2.4V,unless otherwise noted

Sym.	Parameter	Test Conditions		Min.	Typ.	Max.	unit
V_{PGA}	Supply Voltage at VDDA	ENVDDA[0]=0		2.4		3.6	V
I_{PGA}	Operation supply current	PGAGN[1:0]=<11>			320		uA
G_{PGA}	Gain temperature drift	T_A = -40℃~ 85℃	GAIN=128		15		ppm/℃

6.8.2 SD18,performanceⅡ(fSD18=250KHz)

T_A = 25℃,V_{DD} = 3.0V, VDDA=2.9V,V_{VR}=1.0V,GAIN=1 without PGA, unless otherwise noted

Sym.	Parameter	Test Conditions			Min.	Typ.	Max.	unit
INL	Integral Nonlinearity(INL)	VDDA=2.4V,V_{VR}=1.0V,ΔSI=±200mV				±0.003	±0.01	%FSR
		VDDA=2.4V,V_{VR}=1.0V,ΔSI=±450mV						
	No Missing Codes[3]	ADC_CK=250KHz,OSR[2:0]=010b			19			Bits
G_{SD18}	Temperature drift **Gain 1~x16 (INBUF[0]=0b,)**	INBUF[0]=0b,VRBUF[0]=0b		T_A = -40℃~ 85℃		10		ppm/℃
E_{OS}	Offset error of Full Scale Rang input voltage range with Chopper without PGA	ΔAI=0V ΔVR=0.9V DCSET[2:0]=<000> *ΔAI is external short		Gain=2			1	%FSR
	Offset error temperature drift with chopper without PGA			GAIN=1		2		uV/℃
				GAIN=2		1		
				GAIN=4		0.5		
				GAIN=16		0.15		
CM_{SD18}	Common-mode rejection	V_{CM}=0.7V to 1.7V, V_{VR}=1.0V,without PGA		V_{SI}=0V, GAIN=1		90		dB
		V_{CM}=0.7V to 1.7V, V_{VR}=1.0V, without PGA		V_{SI}=0V, GAIN=16		75		

PSRR	DC power supply rejection	VDDA=3.0V,ΔVDDA=±100mV, V_{VR}=1.0V, V_{SI}=1.2V,V_{SI-}=1.2V,	GAIN=1 PGA=off	75	dB
			GAIN=16 PGA=8		

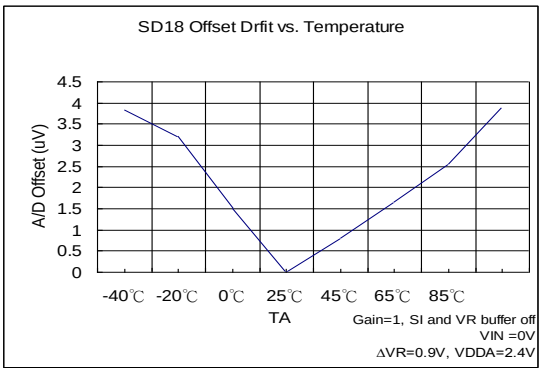


Figure6.8-1(a) SD18 Offset Temperature drift

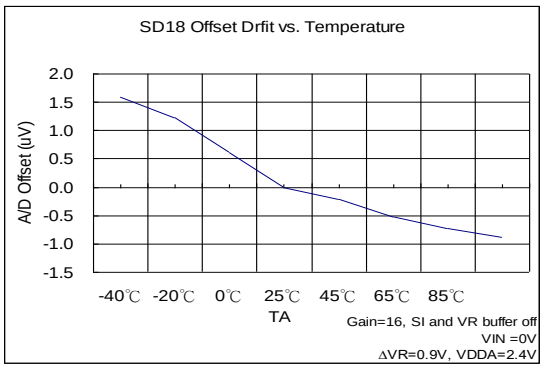


Figure6.8-1(b) SD18 Offset Temperature drift

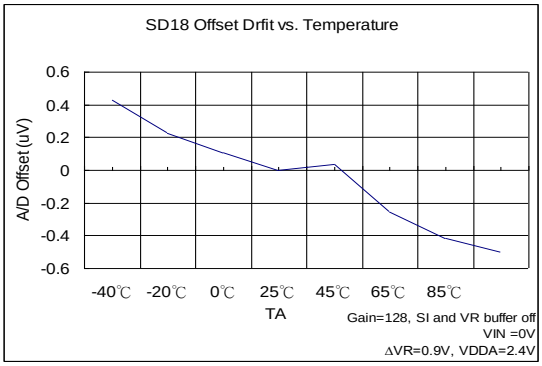


Figure6.8-1(c) SD18 Offset Temperature drift

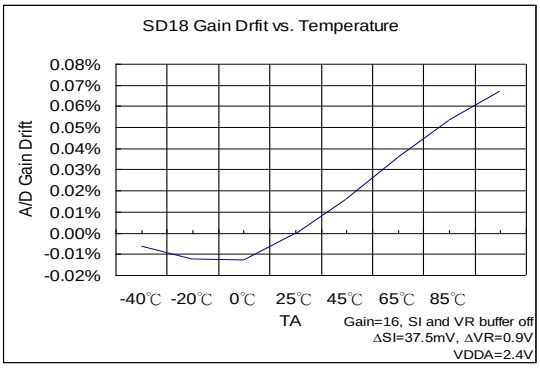


Figure6.8-2(a) SD18 Gain drift with temperature

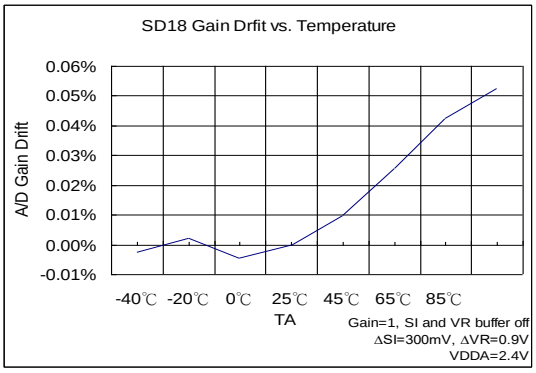


Figure6.8-2(b) SD18 Gain drift with temperature

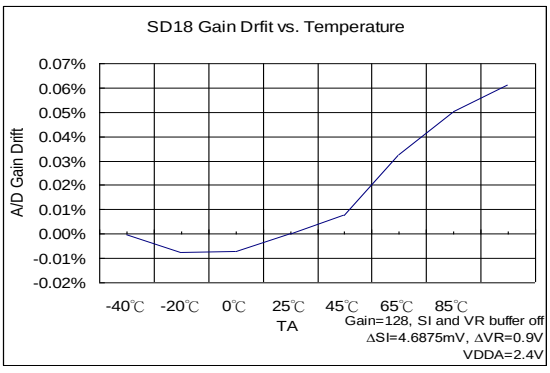


Figure6.8-2(c) SD18 Gain drift with temperature

6.8.3 SD18 Noise Performance

T_A = 25℃,V_{DD} = 3.0V, VDDA=2.4V,unless otherwise noted

HY11P32 針對 SD18 提供了重要的輸入雜訊規格。Table6.8-3(a), Table6.8-3(b) 列出典型的雜訊規格表與 Gain, Output rate, 及單端最大輸入電壓等關係。測試條件設定在外部輸入訊號短路，參考電壓為 1.2V，取樣 1024 筆資料。

ENOB(RMS) with OSR/GAIN at A/D Clock=250Khz, VDDA=2.4V, VREF=1.2V													
Max. Vin(mV) =0.9*VREF (1)	**OSR**					**256**	**512**	**1024**	**2048**	**4096**	**8192**	**16384**	**32768**
	Output rate(HZ)					**977**	**488**	**244**	**122**	**61**	**31**	**15**	**8**
	Gain	**=**	**PGA**	**×**	**ADGN**								
±2400	**0.25**	**=**	**1**	**×**	**0.25**	16.14	17.41	18.04	18.47	18.80	19.06	19.23	19.31
±2160	**0.5**	**=**	**1**	**×**	**0.5**	16.15	17.41	18.03	18.42	18.75	19.13	19.24	19.30
±1080	**1**	**=**	**1**	**×**	**1**	16.12	17.35	17.98	18.37	18.74	19.02	19.24	19.34
±540	**2**	**=**	**1**	**×**	**2**	16.06	17.18	17.80	18.20	18.64	18.98	19.17	19.32
±270	**4**	**=**	**1**	**×**	**4**	15.97	16.97	17.57	17.98	18.44	18.79	19.05	19.20
±135	**8**	**=**	**1**	**×**	**8**	15.79	16.66	17.20	17.70	18.16	18.50	18.85	19.10
±68	**16**	**=**	**1**	**×**	**16**	15.53	16.30	16.79	17.36	17.79	18.26	18.60	18.87
±8	**128**	**=**	**8**	**×**	**16**	13.84	14.35	14.87	15.33	15.85	16.38	16.85	17.28

(1) Max.Vin (mV) is the max. input voltage of single end to ground (VSS).

Table6.8-3(a) SD18 ENOB Table

RMS Noise(uV) with OSR/GAIN at A/D Clock=250Khz, VDDA=2.4V, VREF=1.2V													
Max. Vin(mV) =0.9*VREF	**OSR**					**256**	**512**	**1024**	**2048**	**4096**	**8192**	**16384**	**32768**
	Output rate(HZ)					**977**	**488**	**244**	**122**	**61**	**31**	**15**	**8**
	Gain	**=**	**PGA**	**×**	**ADGN**								
±2400	**0.25**	**=**	**1**	**×**	**0.25**	133.39	55.79	35.80	26.52	21.22	17.56	15.68	14.77
±2160	**0.5**	**=**	**1**	**×**	**0.5**	66.41	27.72	18.10	13.82	11.01	8.37	7.75	7.45
±1080	**1**	**=**	**1**	**×**	**1**	33.93	14.45	9.32	7.11	5.51	4.53	3.88	3.62
±540	**2**	**=**	**1**	**×**	**2**	17.68	8.15	5.28	4.00	2.96	2.32	2.04	1.84
±270	**4**	**=**	**1**	**×**	**4**	9.42	4.69	3.10	2.34	1.69	1.32	1.11	1.00
±135	**8**	**=**	**1**	**×**	**8**	5.33	2.91	2.00	1.41	1.03	0.81	0.64	0.54
±68	**16**	**=**	**1**	**×**	**16**	3.17	1.87	1.33	0.90	0.66	0.48	0.38	0.31
±8	**128**	**=**	**8**	**×**	**16**	1.28	0.90	0.63	0.46	0.32	0.22	0.16	0.12

Table6.8-3(b) SD18 RMS Noise Table

The RMS noise are referred to the input. The Effective Number of Bits (ENOB(RMS Bit)) is defined as:

$$ENOB(RMS) = \ln\left(\frac{FSR}{RMS\,Noise}\right) \Big/ \ln(2)$$

$$RMS\,Noise = \left(2 \times VREF \times \sqrt{\sum_{k=1}^{1024}(ADO[k] - Average)^2}\right) \Big/ 2^{23}$$

$$Where\,FSR\,(Full\text{-}Scale\,Range) = 2 \times VREF/Gain.$$

$$Average = \frac{\sum_{k=1}^{1024}(ADO[k])}{1024}$$

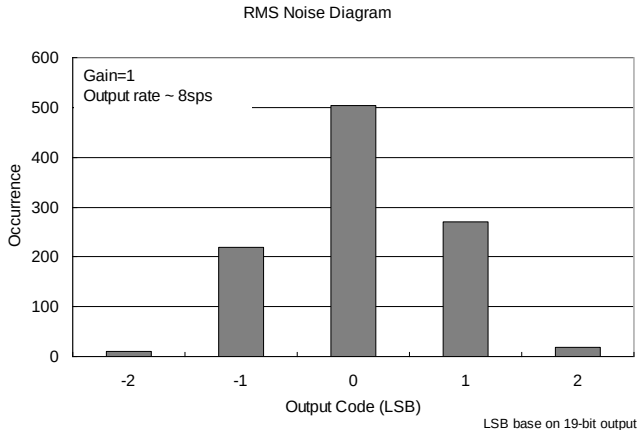


Figure6.8-3(a) RMS Noise Diagram

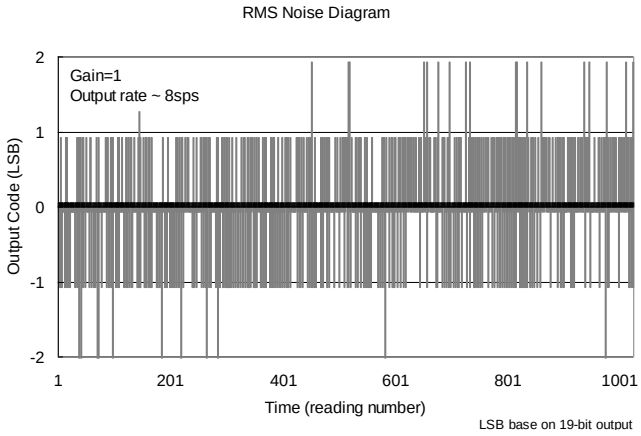


Figure6.8-3(b) Output Code Diagram

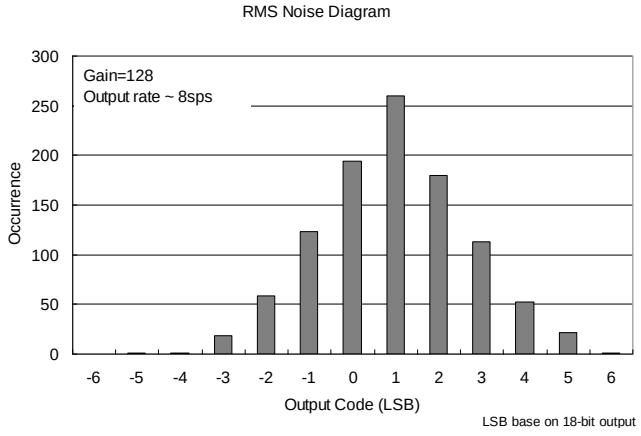


Figure6.8-3(c) RMS Noise Diagram

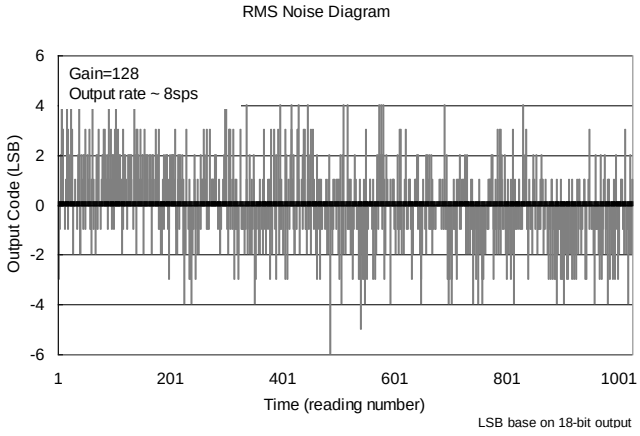


Figure6.8-3(d) Output Code Diagram

6.9 Build-In EPROM(BIE)

T_A = 25℃,V_{DD} = 3.0V, unless otherwise noted

Sym.	Parameter	Test Conditions	Min.	Typ.	Max.	unit
V_{BIE}	Supply Voltage			6.0	6.5	V
I_{BIE}	Operation supply current			5		mA
V_{SS}	Supply Voltage			0		V

7. 訂貨資訊

下單品名 [1]	封裝型式	引腳數	封裝型式描述方式		程式碼編號 [2]	出貨包裝形式	個裝數量	材料組成	MSL[3]
HY11P32-D000	Die	-	D	000	000	-	250	Green[4]	-
HY11P32-L044	LQFP	44	L	044	000	Tray	160	Green[4]	MSL-3
HY11P32-L048	LQFP	48	L	048	000	Tray	250	Green[4]	MSL-3

[1] **產品名稱 – 封裝型式描述方式 – 程式碼編號 (空白片 / 標準品 / 代客燒錄碼)**

例如：您的代客燒錄服務申請的程式碼編號為 008，且需要的產品是裸片出貨。則下單品名為 HY11P32-D000-008

例如：您的需求是不帶程式碼的空白片且需要的產品是裸片出貨。則下單品名為 HY11P32-D000

例如：您的需求是不帶程式碼的空白片且需要的產品是封裝片 LQFP44 出貨，則下單品名為 HY11P32-L044，且需以 Tray 出貨，則除下單品名外，請特別註明出貨包裝形式為 Tray

例如 : 您的代客燒錄服務申請的程式碼編號為 009，而需求的產品是封裝片 LQFP48 出貨，則下單品名為 HY11P32-L048-009，且需以 Tray 出貨，則除下單品名外，請特別註明出貨包裝形式為 Tray

[2] **程式碼編號**

“001”~“999” 為標準品或代客燒錄申請的程式碼編號，而空白晶片不帶此碼。

[3] **MSL:**

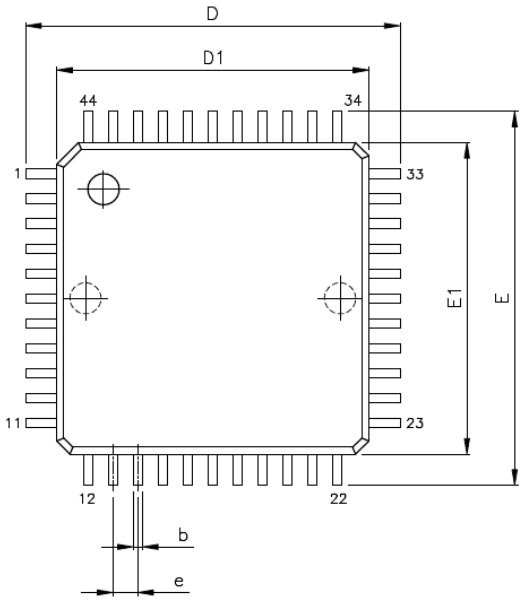
濕度敏感性等級係依據 IPC/JEDEC J-STD-020 的規範加以試驗分級，並參考 IPC/JEDEC J-STD-033 的標準處理、包裝、運輸與使用。

[4] **Green (RoHS & no Cl/Br):**

HYCON 產品皆為 Green Product，符合 RoHS 指令以及無鹵素規定(Br/Cl<0.1%)

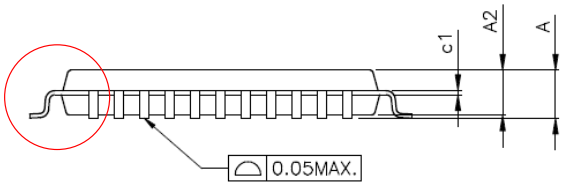
8. 封裝型式資訊

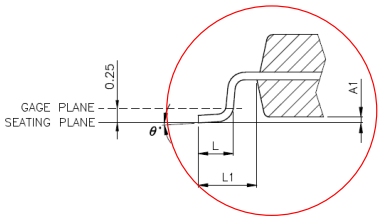
8.1 LQFP44(L044)



VARIATIONS (ALL DIMENSIONS SHOWN IN MM)

SYMBOLS	MIN.	NOM.	MAX.
A	—	—	1.60
A1	0.05	—	0.15
A2	1.35	1.40	1.45
c1	0.09	—	0.16
D		12.00 BSC	
D1		10.00 BSC	
E		12.00 BSC	
E1		10.00 BSC	
e		0.80 BSC	
b	0.30	0.37	0.45
L	0.45	0.60	0.75
L1		1.00 REF	
θ°	0°	3.5°	7°





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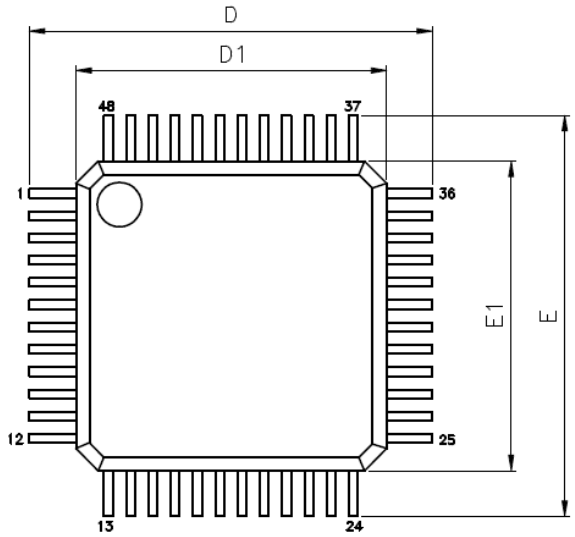
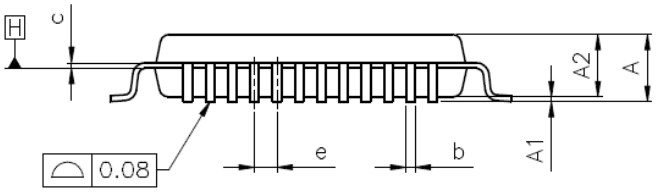
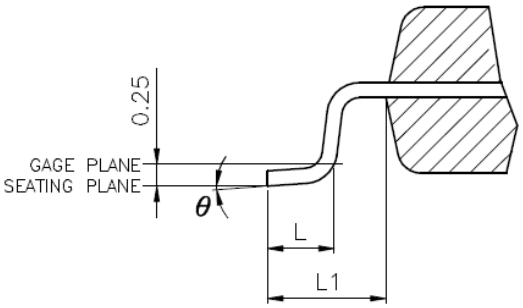
8.2 LQFP48(L048)



VARIATIONS (ALL DIMENSIONS SHOWN IN MM)

SYMBOLS	MIN.	NOM.	MAX.
A	--	--	1.60
A1	0.05	--	0.15
A2	1.35	1.40	1.45
b	0.17	0.22	0.27
c	0.09	--	0.20
D	9.00 BSC		
D1	7.00 BSC		
E	9.00 BSC		
E1	7.00 BSC		
e	0.50 BSC		
L	0.45	0.60	0.75
L1	1.00 REF		
θ	0°	3.5°	7°





JEDEC MS-026 compliant

9. 修訂記錄

以下描述本文件差異較大的地方，而標點符號與字形的改變不在此描述範圍。

版本	頁次	變更摘要
V01	ALL	初版發行
V02	6	修訂 2.2 內容
	8	修訂應用電路
	10	修訂暫存器列表資料
	20	修訂 6.8 內容
	22	新增 Build-In EPROM 規格
V03	9	修改方塊圖，說明 WDT reset 為 40H
	10	修訂暫存器列表資料
	20	Gain=1=>10ppm/℃
		Gain=128=>15ppm/℃
V04	10	新增 SD18 Network
V05	1	修訂標題文字
	5	修訂引腳圖文字
	22	修訂 Figure6.8 內容
V06	9	修改方塊圖，刪除 XTI 與 XTO
	13	HAO=>2MHz±20%
	22	圖片排序調整
V07	4	新增外部輸入電壓檢測功能
	5	新增 PT1.2 的 LVDIN 功能
	6	新增 PT1.2 的 LVDIN 功能
	8	新增 PT1.2 的 LVDIN 功能
	9	修正方塊圖內容，WDT reset 為 00H
	11	修正暫存器內容，新增 PT1.2 的 LVDIN 功能
	16	新增 PT1.2 的 LVDIN 功能
V08	5	增加註 3 內容說明
	8	修訂應用電路圖
V09	9	修改圖 4-1 內容
	18	修訂 Power System 溫飄規格
	23~24	增加 SD18 Noise Performance 章節
V10	4	修改 1.特點內容
	12	修改 6.電氣特性內容

	24	修改 RMS Noise Diagram
V11	6	增加 LQFP48 引腳圖
	27	增加訂貨資訊
	29	增加封裝型式資訊
V12	10	修改開發工具相關使用說明書編號
	27	增加訂貨資訊內容