HY11P13
Datasheet

8-Bit RISC-like Mixed Signal Microcontroller
Embedded 4x20 LCD Driver
Low Noise Amplifier
18-Bit ΣΔADC

Table of Contents

注意：

1、 本說明書中的內容，隨著產品的改進，有可能不經過預告而更改。請客戶及時到本公司網站下載更新 http://www.hycontek.com。

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8、 本規格書中內容，未經本公司許可，嚴禁用於其他目的之轉載或複製。

1. 特點

- 8 位元加強型精簡指令集，共有 66 個指令包含硬體乘法指令及查表指令
- 2.2V to 3.6V工作電壓範圍，-40℃~85℃工作溫度範圍
- 外部石英震盪器及內部高精度RC震盪器，6 種CPU工作時脈切換選擇，可讓使用者達到最佳省電規劃
  - 運行模式 300uA@2MHz
  - 待機模式 3uA@32KHz
  - 休眠模式 1uA
- 4KWord OTP (One Time Programmable) Type程式記憶體，256Byte資料記憶體
- Brownout and Watch dog Timer，可防止CPU進入死機模式
- 18bit全差動輸入ΣΔADC類比數位轉換器
  - 內置PGA (Programmable Gain Amplifier) 及可有 1/4、1/2、1. .....128 倍 10 種輸入信號放大倍率選擇
  - 內置輸入零點調整，可針對不同應用增加其量測範圍
  - 內置高阻抗輸入緩衝器(32 以上輸入倍率不適用)
  - 內置絕對溫度感測器
- 超低輸入雜訊(<1uVpp)運算放大器，可提供高輸出阻抗小訊號的放大及小電流的電壓轉換
- 1.0V的內部類比電路共地電壓源，具有Push-Pull驅動能力，可提供傳感器驅動電壓
- LVD低電壓檢測功能具 14 段檢測電壓設置與外部輸入電壓檢測功能
- 類比電壓源VDDA可選擇 4 種不同輸出電壓，具 10mA穩壓電壓源輸出能力
- 4x20 LCD液晶驅動器
  - Static、1/2、1/3、1/4 Duty及 1/3 Bias 軟體選擇
  - 內建Charge Pump穩壓線路，提供 4 種LCD偏壓
- 8-bit Timer A
- 16-bit Timer B模組具Capture/Compare 功能
- 8-bit Timer C 模組具PWM/PFD波形產生功能
- 串列通訊SPI模組
- Support 6 stack level

功能列表

Model No.	VDD	System Clock	Program Memory (word)	SRAM (byte)	ADC ENOB (bit x ch)	Sample Rate (sps)	TPS / RTC / Serial Interface	OPAMP (type x ch.)	I/O	LCD (com x seg) / Timer (bit x ch) / PWM (bit x ch)	Package
HY11P13	2.2V~3.6V	28KHz~2MHz	4K	256	20-bit x 8	8~977	Yes / Y / SPI	LAN x1	4xI + 10xIO	4 x 20 / 8-bit x 2 16-bit x 1 / 8-bit x 1	LQFP64

2. 引腳定義

2.1. LQFP64 引腳圖

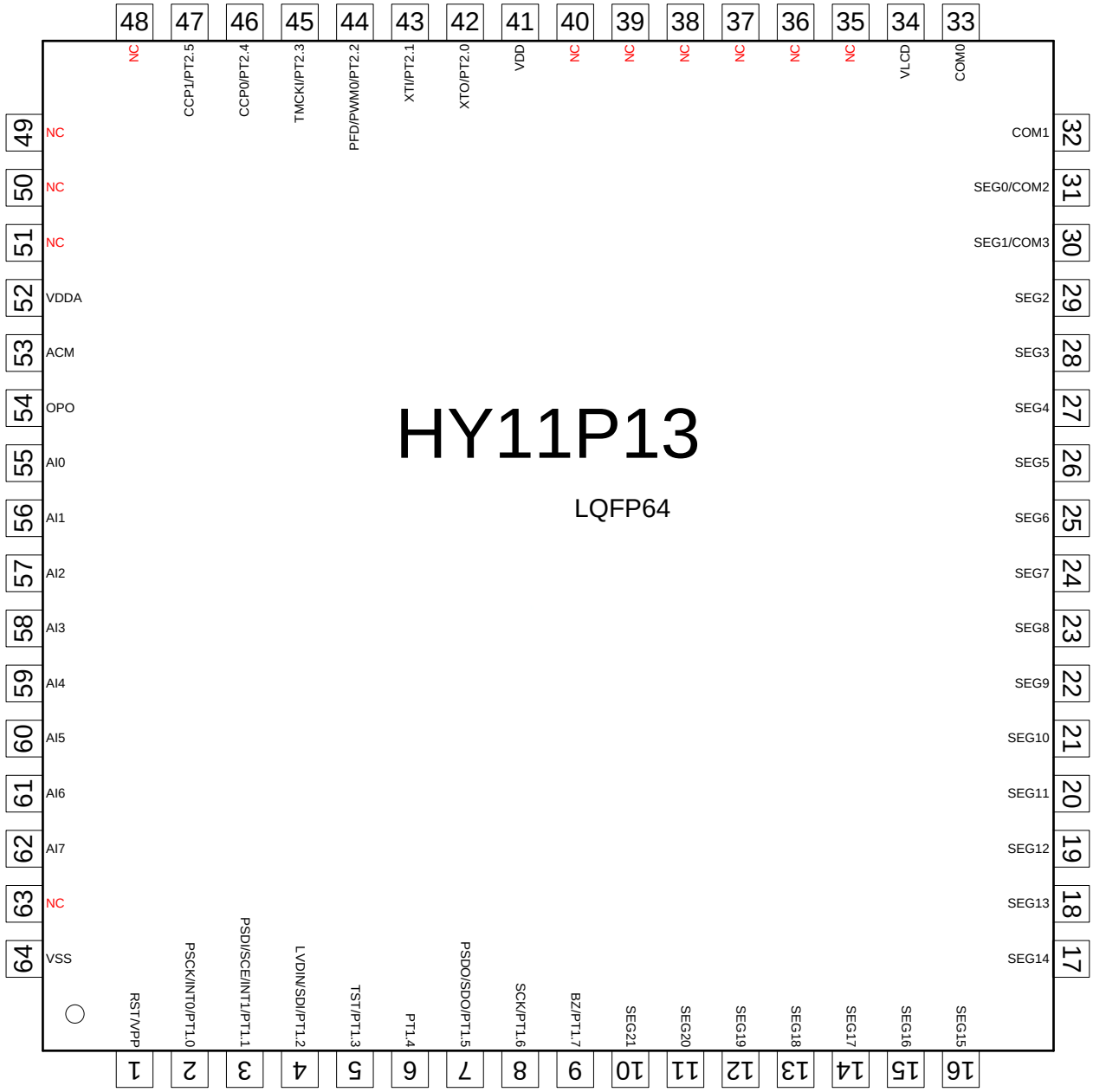


圖 2-1 HY11P13 LQFP64 引腳圖

註 1：VPP 與 RST 復用同一接口，非燒錄 EPROM 時禁止輸入電壓超過 5.8V

註 2：TST 與 PT1.3 復用同一接口，操作時禁止輸入電壓超過 VDD+0.3V

註 3：若不將 PT1.3 設定成外部引腳按鍵，可以提升抗干擾能力

2.2. I/O 引腳定義

"I/O"輸入/輸出,"I"輸入,"O"輸出,"S"史密斯觸發,"C"CMOS 特性兼容輸出與輸入,"P"電壓源,"A"類比通道

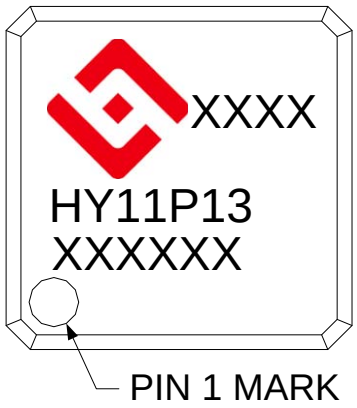
編號	引腳名稱	引腳特性		功能說明
		格式	緩衝	
1	RST/VPP			
	RST	I	S	復位晶片
	VPP	P	P	EPROM讀/寫時的電壓源
2	PT1.0/INT0/PSCK			
	PT1.0	I	S	數位輸入
	INT0	I	S	中斷源INT0
	PSCK	I	S	OTP讀/寫介面SCK接口
3	PT1.1/INT1/PSDI/SCE			
	PT1.1	I	S	數位輸入
	INT1	I	S	中斷源INT1
	PSDI	I	S	OTP讀/寫介面SDI接口
	SCE	I	S	SPI通訊介面SCE接口
4	PT1.2/SDI/LVDIN			
	PT1.2	I	S	數位輸入
	SDI	I/O	S	SPI通訊介面SDI接口
	LVDIN	A	A	LVD外部信號輸入接口
5	PT1.3/TST			
	PT1.3	I	S	數位輸入
	TST	I	S	測試模式致能輸入（未開放）
6	PT1.4	I/O	S	數位輸入/輸出
7	PT1.5/PSDO/SDO			
	PT1.5	I/O	S	數位輸入/輸出
	PSDO	O	C	OTP讀/寫介面SDO接口
	SDO	I/O	S	SPI通訊介面SDO接口
8	PT1.6/SCK			
	PT1.6	I/O	S	數位輸入/輸出
	SCK	I/O	S	SPI通訊介面SCK接口
9	PT1.7/BZ			
	PT1.7	I/O	S	數位輸入/輸出
	BZ	O	C	蜂鳴器輸出端
10	SEG21	O	A	LCD的Segment輸出
11	SEG20	O	A	LCD的Segment輸出
12	SEG19	O	A	LCD的Segment輸出

13	SEG18	O	A	LCD的Segment輸出
14	SEG17	O	A	LCD的Segment輸出
15	SEG16	O	A	LCD的Segment輸出
16	SEG15	O	A	LCD的Segment輸出
17	SEG14	O	A	LCD的Segment輸出
18	SEG13	O	A	LCD的Segment輸出
19	SEG12	O	A	LCD的Segment輸出
20	SEG11	O	A	LCD的Segment輸出
21	SEG10	O	A	LCD的Segment輸出
22	SEG9	O	A	LCD的Segment輸出
23	SEG8	O	A	LCD的Segment輸出
24	SEG7	O	A	LCD的Segment輸出
25	SEG6	O	A	LCD的Segment輸出
26	SEG5	O	A	LCD的Segment輸出
27	SEG4	O	A	LCD的Segment輸出
28	SEG3	O	A	LCD的Segment輸出
29	SEG2	O	A	LCD的Segment輸出
30	COM3/SEG1	O	A	LCD的COM與Segment共用輸出
31	COM2/SEG0	O	A	LCD的COM與Segment共用輸出
32	COM1	O	A	LCD的COM輸出
33	COM0	O	A	LCD的COM輸出
34	VLCD	P	P	LCD的電壓源
35	NC	-	-	未使用
36	NC	-	-	未使用
37	NC	-	-	未使用
38	NC	-	-	未使用
39	NC	-	-	未使用
40	NC	-	-	未使用
41	VDD	P	P	晶片工作電壓源
42	PT2.0/XTO PT2.0 XTO	 I/O A	 S A	 數位輸入/輸出 外接振盪器輸出端
43	PT2.1/XTI PT2.1 XTI	 I/O A	 S A	 數位輸入/輸出 外接振盪器輸入端
44	PT2.2/PWM0/PFD PT2.2	 I/O	 C	 數位輸入/輸出

	PWM0	O	C	PWM 輸出接口
	PFD	O	C	PFD 輸出接口
45	PT2.3/TMCKI			
	PT2.3	I/O	S	數位輸入/輸出
	TMCKI	I	S	TIMERC 時脈源輸入接口
46	PT2.4/CCP0			
	PT2.4	I/O	S	數位輸入/輸出
	CCP0	I	S	捕捉/比較模式信號接口
47	PT2.5/CCP1			
	PT2.5	I/O	S	數位輸入/輸出
	CCP1	I	S	捕捉/比較模式信號接口
48	NC	-	-	未使用
49	NC	-	-	未使用
50	NC	-	-	未使用
51	NC	-	-	未使用
52	VDDA	P	P	穩壓器輸出，類比電路電壓源
53	ACM	P	P	內部類比電路共地引腳
54	OPO	A	A	運算放大器輸出
55	AI0	A	A	類比輸入通道
56	AI1	A	A	類比輸入通道
57	AI2	A	A	類比輸入通道
58	AI3	A	A	類比輸入通道
59	AI4	A	A	類比輸入通道
60	AI5	A	A	類比輸入通道
61	AI6	A	A	類比輸入通道
62	AI7	A	A	類比輸入通道
63	NC	-	-	未使用
64	VSS	P	P	晶片工作電壓源接地端

表 2-1 引腳定義與功能說明

2.2.1. LQFP 封裝片標記信息



→ 紘康 Logo + 生產識別碼

→ 產品名稱 ：HY11P13

→ 產品批號

3. 應用電路

3.1. 橋式感測器 I

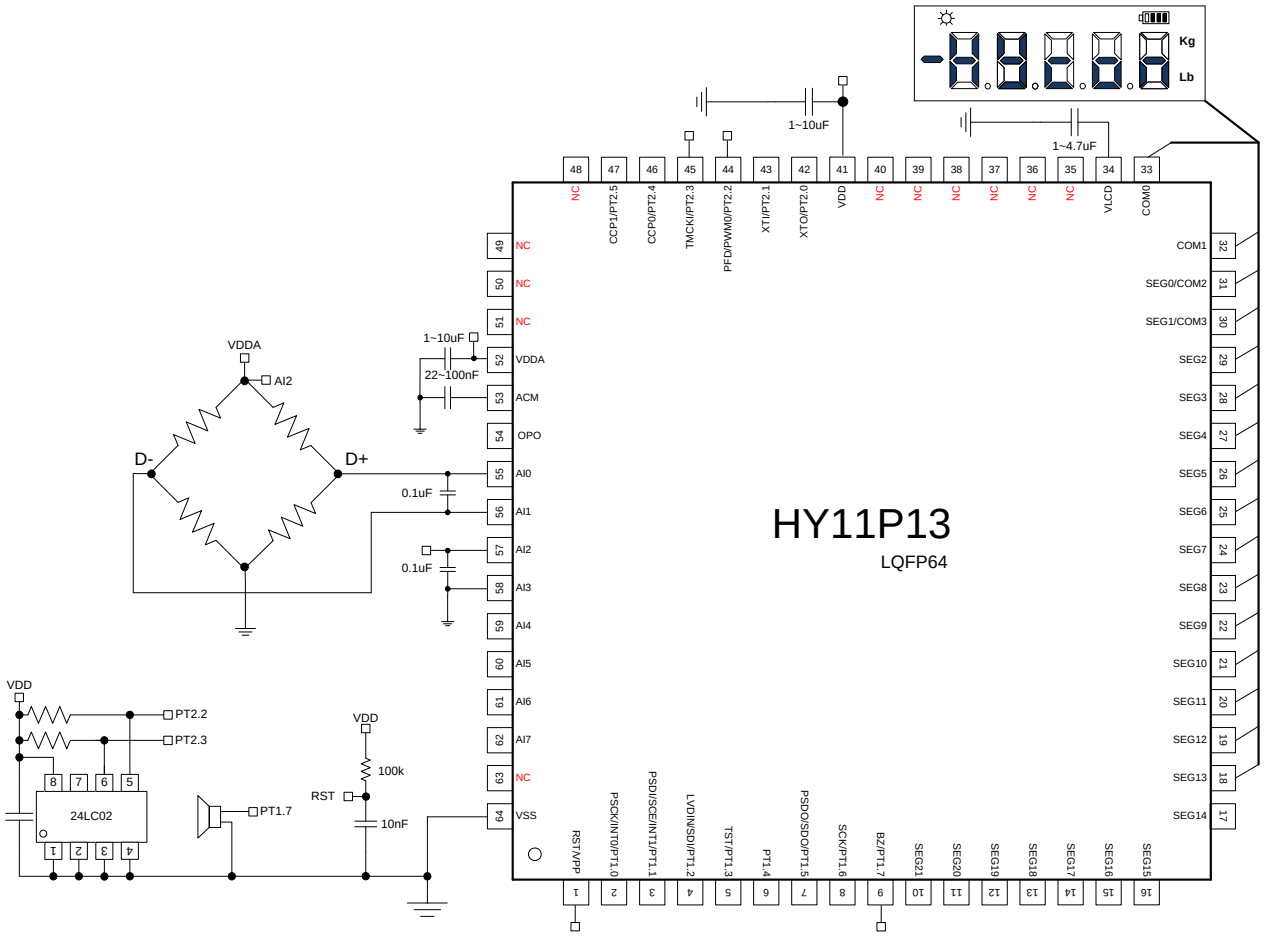


圖 3-1 橋式感測器應用電路

註：Load Cell 零點電壓位置可透過 DCSET[2:0]進行偏壓調整

3.2. 橋式感測器 Ⅱ

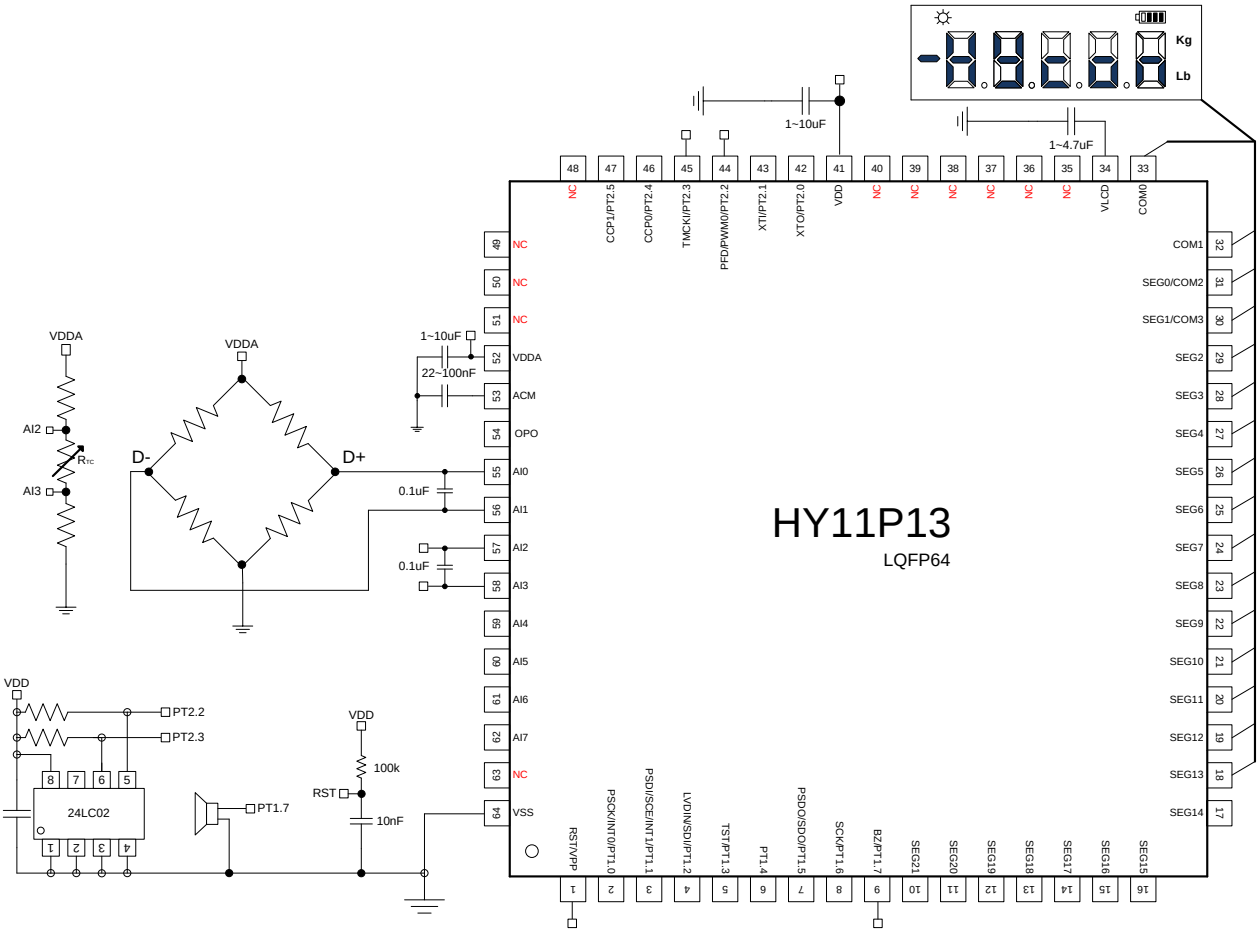


圖 3-2 具溫度補償的橋式感測器應用電路

註：使用溫度補償電阻 NTC 基本線路

註：Load Cell 零點電壓位置可透過 DCSET[2:0]進行偏壓調整

3.3. 橋式感測器(Pressure Sensor)

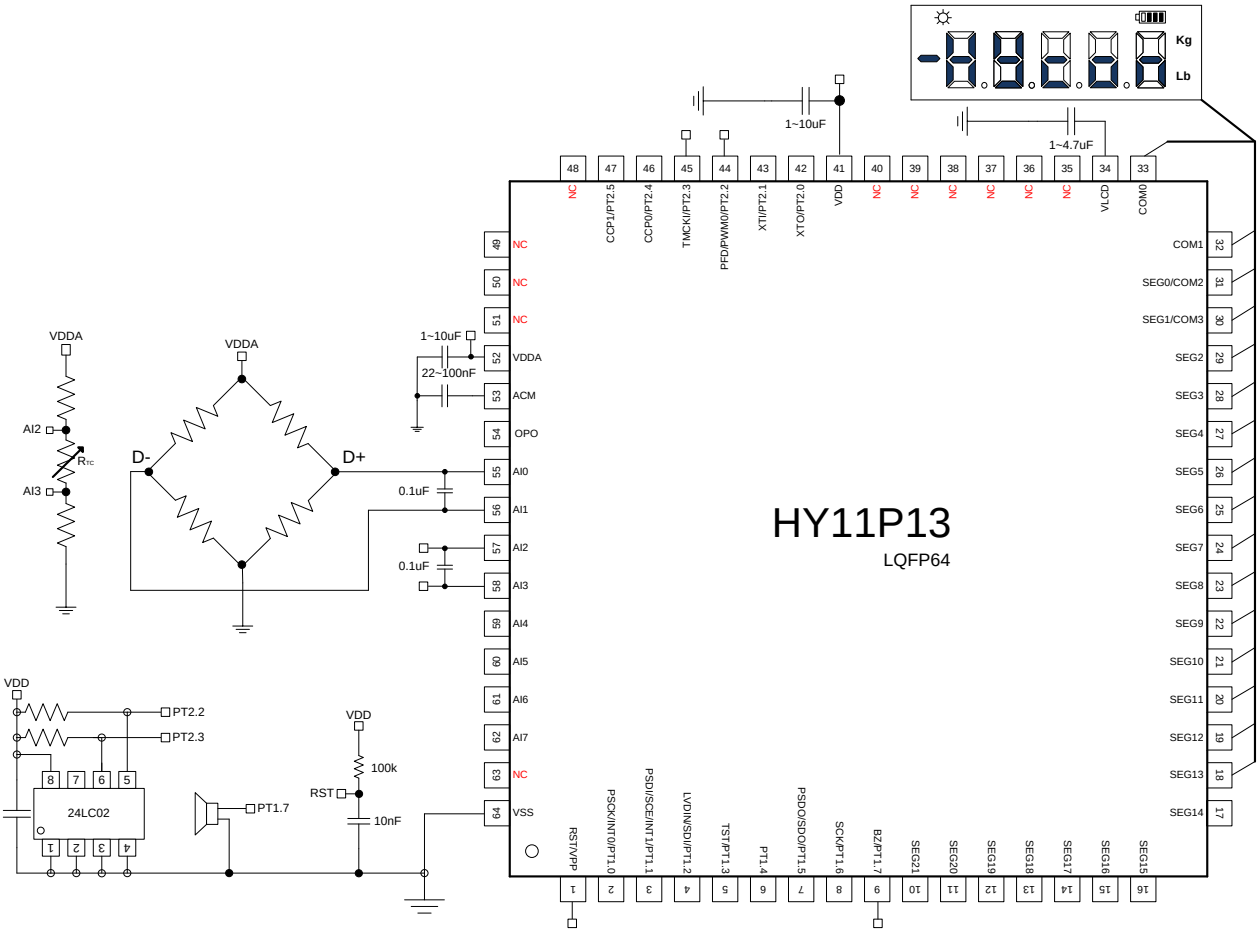


圖 3-3 具溫度補償的橋式感測器應用電路(不使用內部 PGA 放大)

註：使用溫度補償電阻 NTC 基本線路

註：Pressure sensor 零點電壓位置可透過 DCSET[2:0]進行偏壓調整

3.4. 紅外線感測器

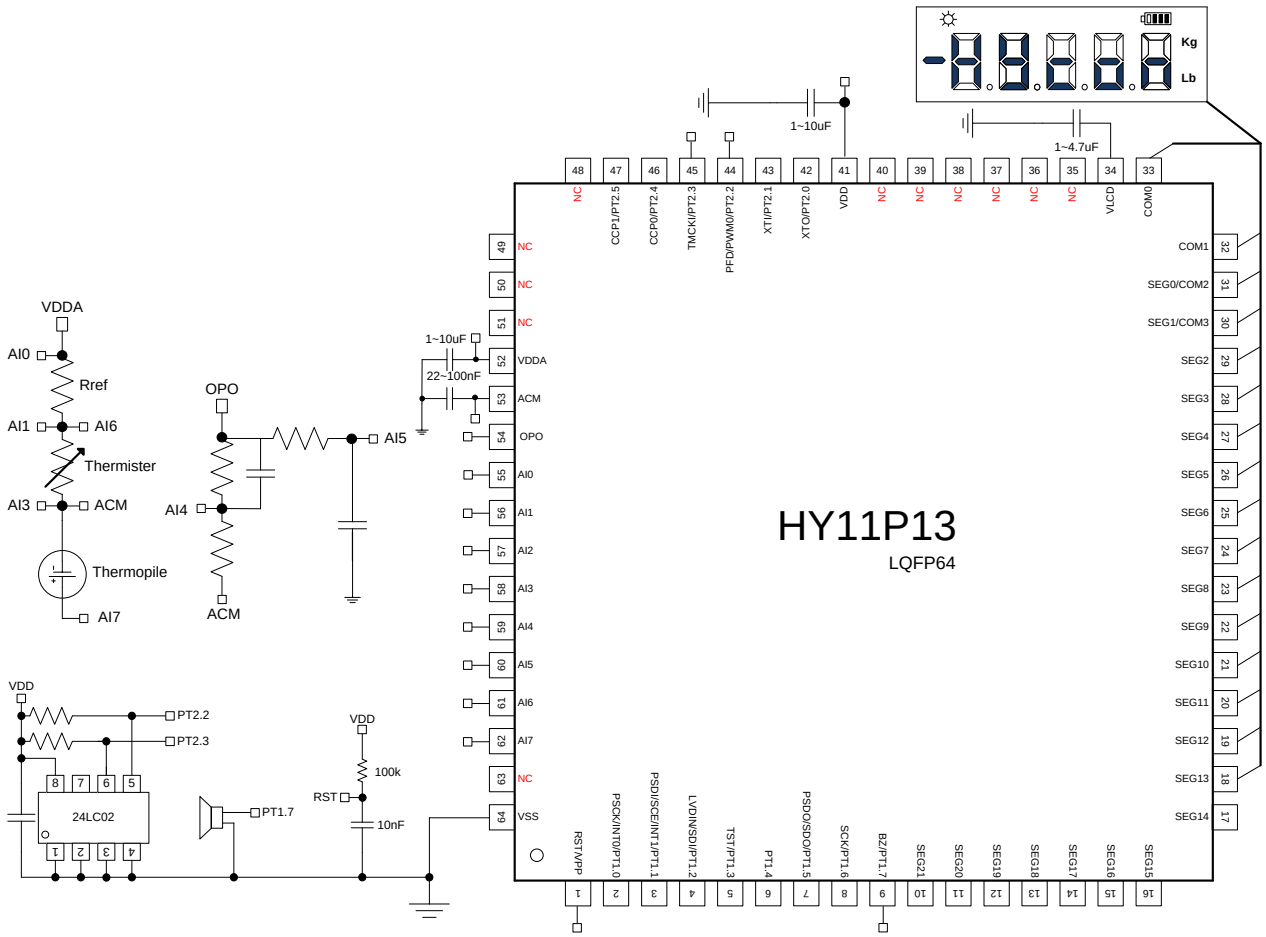


圖 3-4 紅外線感測器應用電路

3.5. 4-20mA 電流錶頭(兩線式)

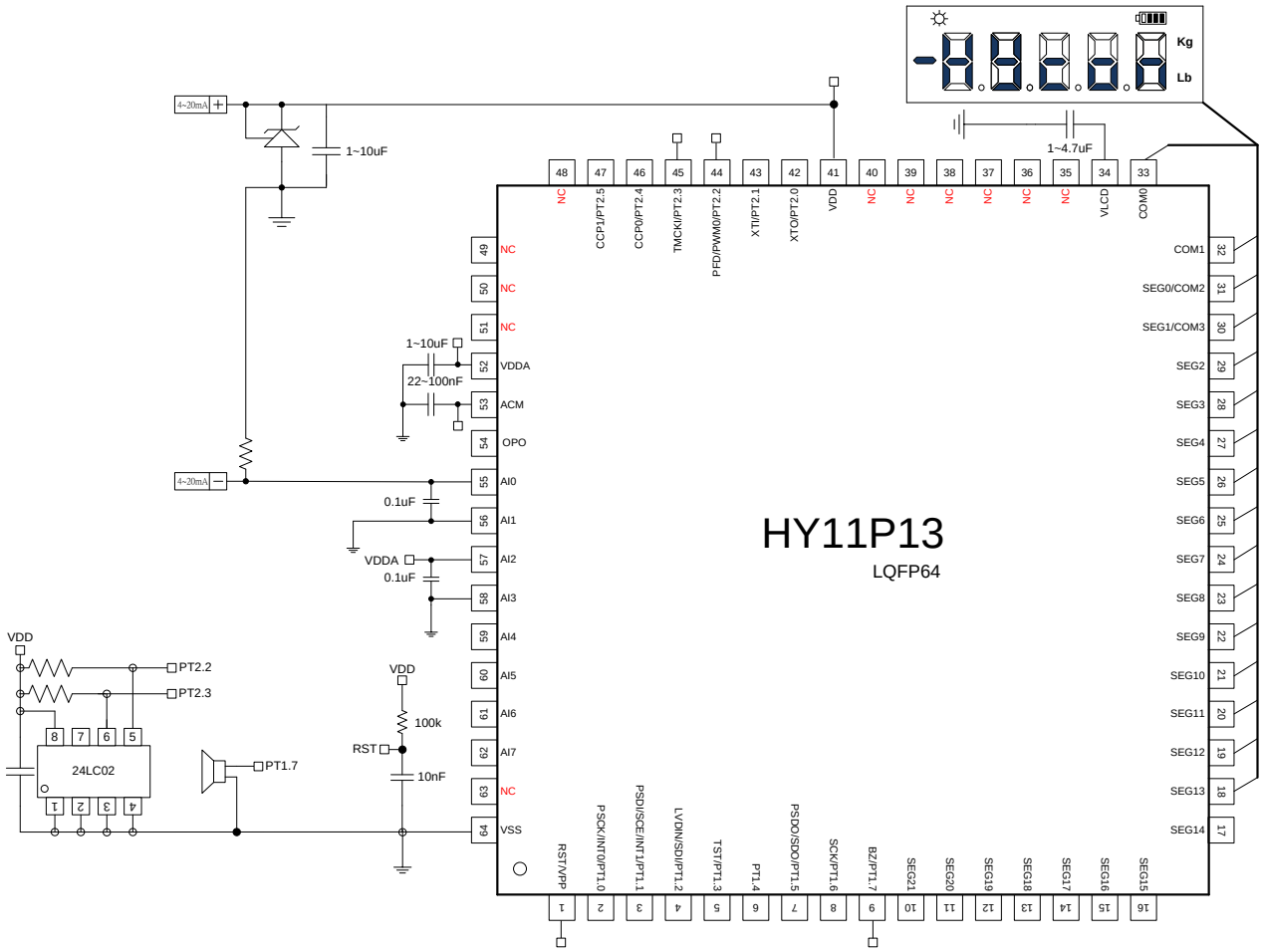


圖 3-5 無需外接電源的 4-20mA 錶頭

4. 功能概述

4.1. 內部方塊圖

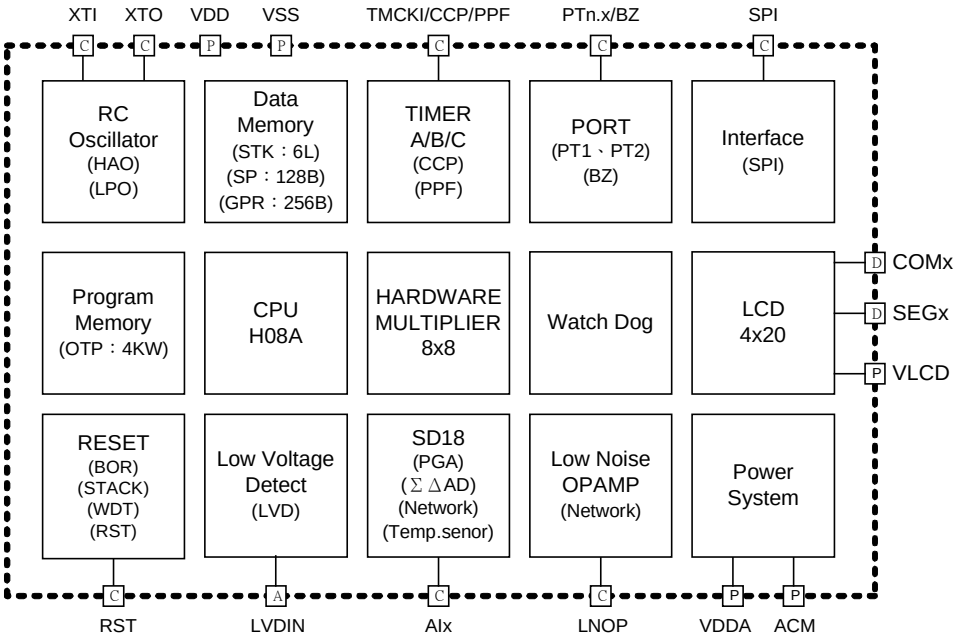


圖 4-1 HY11P13 內部方塊圖

4.2. 相關說明與支援文件

晶片功能相關使用說明書

DS-HY11P13-Vxx	HY11P13 說明書
UG-HY11S14-Vxx	HY11Pxx 系列使用說明書
APD-CORE002-Vxx	H08A 指令說明書

開發工具相關使用說明書

APD-HYIDE006-Vxx	HY11xxx 系列開發工具軟體使用說明書
APD-HYIDE005-Vxx	HY11xxx 系列開發工具硬體使用說明書
APD-OTP001-Vxx	OTP 產品燒錄引腳說明書

產品生產相關使用說明書

APD-HYIDE004-Vxx	HY1xxxx 系列生產線專用燒錄器說明書
BDI-HY11P13-Vxx	HY11P13 個別產品的裸片打線資訊

4.3. SD18 Network

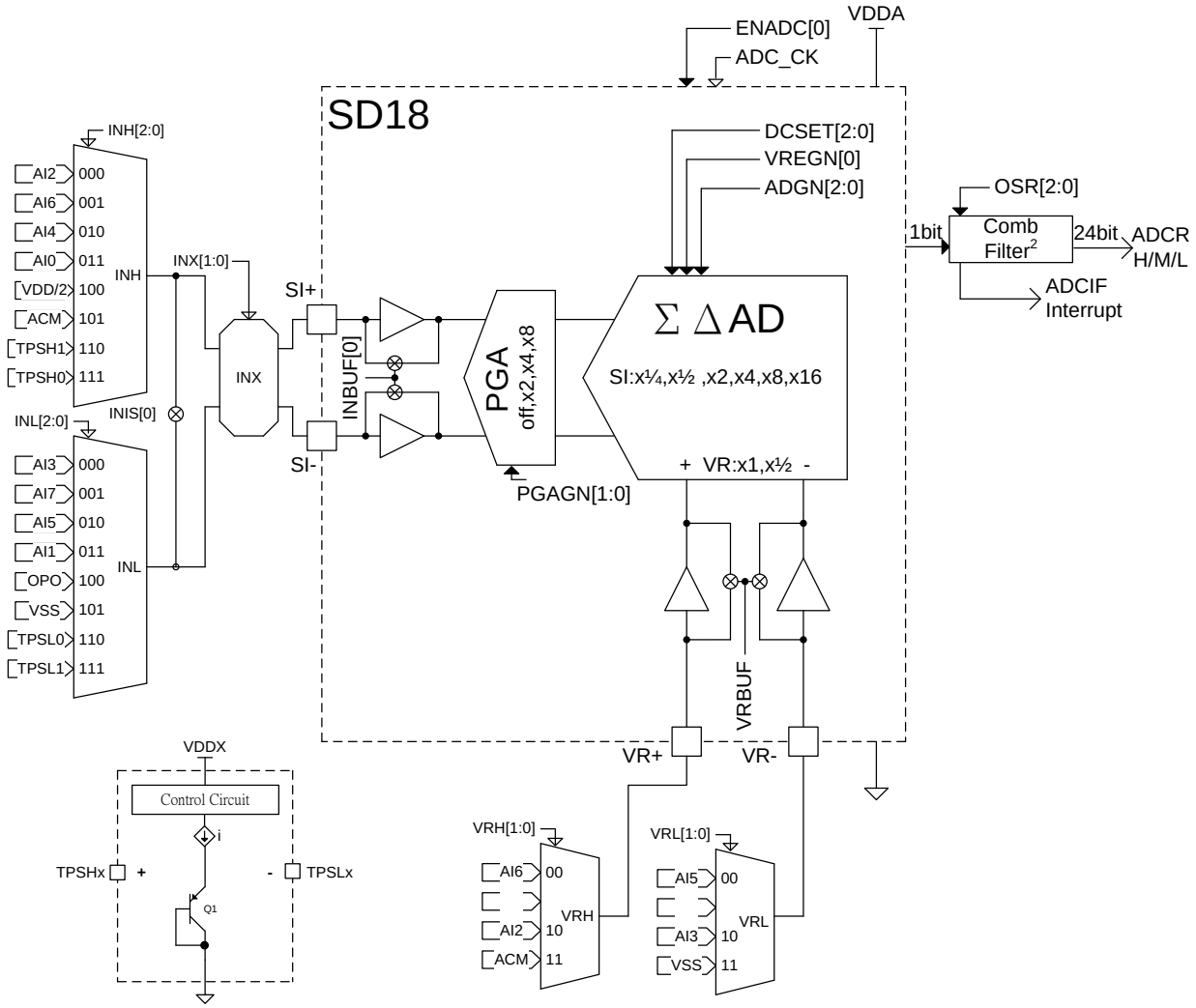


圖 4-2 SD18 Network

4.4. Low Noise OPAMP Network

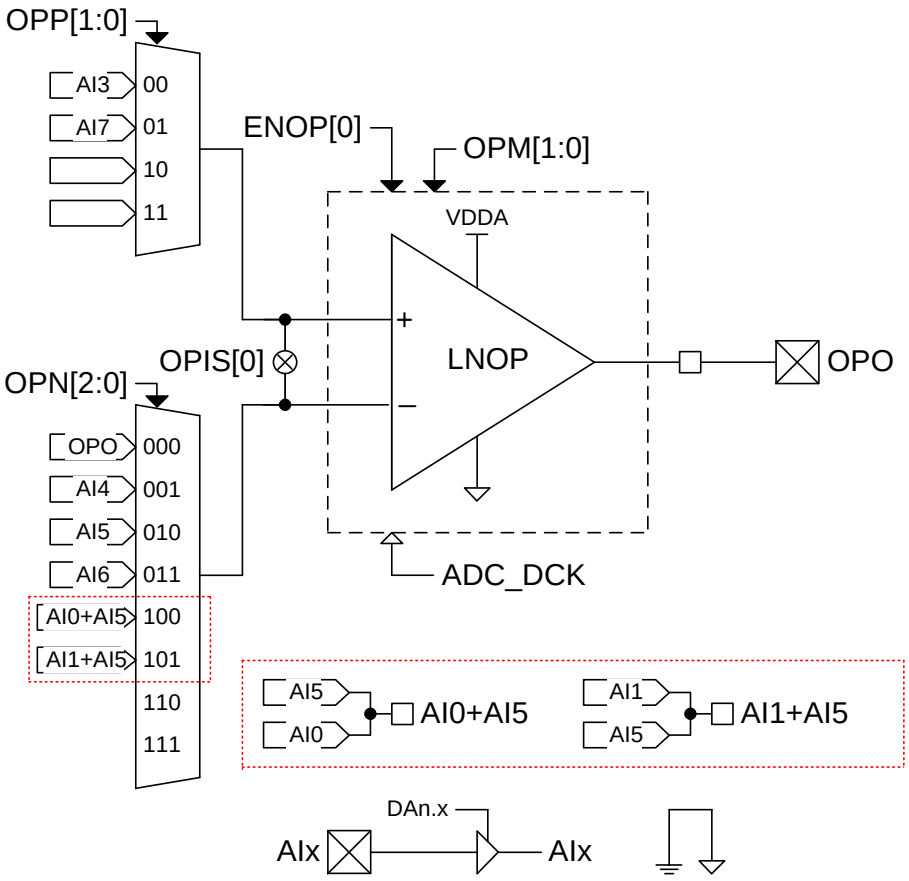


圖 4-3 Low Noise OPAMP Network

5. 暫存器列表

“-”no use,“*”read/write,“w”write,“r”read,“r0”only read 0,“r1”only read 1,“w0”only write 0,“w1”omly write 1												
“.”unimplemented bit,“x”unknown,“u”unchanged,“d”depends on condition												
Address	**File Name**	**Bit7**	**Bit6**	**Bit5**	**Bit4**	**Bit3**	**Bit2**	**Bit1**	**Bit0**	**A-RESET**	**i-RESET**	**R/W**
00H	INDF0	Contents of FSR0 to address data memory value of FSR0 not changed								N/A	N/A	*,*,*,*,*,*,*,*
01H	POINC0	Contents of FSR0 to address data memory value of FSR0 post-incremented								N/A	N/A	*,*,*,*,*,*,*,*
02H	PODEC0	Contents of FSR0 to address data memory value of FSR0 post-decremented								N/A	N/A	*,*,*,*,*,*,*,*
03H	PRINC0	Contents of FSR0 to address data memory value of FSR0 pre-incremented								N/A	N/A	*,*,*,*,*,*,*,*
04H	PLUSW0	Contents of FSR0 to address data memory value of FSR0 offset by W								N/A	N/A	*,*,*,*,*,*,*,*
05H	INDF1	Contents of FSR1 to address data memory value of FSR0 not changed								N/A	N/A	*,*,*,*,*,*,*,*
06H	POINC1	Contents of FSR1 to address data memory value of FSR0 post-incremented								N/A	N/A	*,*,*,*,*,*,*,*
07H	PODEC1	Contents of FSR1 to address data memory value of FSR0 post-decremented								N/A	N/A	*,*,*,*,*,*,*,*
08H	PRINC1	Contents of FSR1 to address data memory value of FSR0 pre-incremented								N/A	N/A	*,*,*,*,*,*,*,*
09H	PLUSW1	Contents of FSR1 to address data memory value of FSR0 offset by W								N/A	N/A	*,*,*,*,*,*,*,*
0FH	FSR0H								FSR0[8]	x	....u	-,-,-,- -,-,-,*
10H	FSR0L	Indirect Data Memory Address Pointer 0 Low Byte,FSR0[7:0]								xxxx xxxx	uuuu uuuu	*,*,*,*,*,*,*,*
11H	FSR1H								FSR1[8]	x	....u	'-,-,-,- -,-,-,*
12H	FSR1L	Indirect Data Memory Address Pointer 1 Low Byte,FSR1[7:0]								xxxx xxxx	uuuu uuuu	*,*,*,*,*,*,*,*
16H	TOSH					TOS[11]	TOS[10]	TOS[9]	TOS[8]	 0000	 0000	-,-,-,- *,*,*,*
17H	TOSL	Top-of-Stack Low Byte (TOS<7:0>)								0000 0000	0000 0000	*,*,*,*,*,*,*,*
18H	STKPTR	STKFL	STKUN	STKOV			STKPRT[2:0]			000. .000	000. .000	r,rw0,rw0,- -,r,r,r
1AH	PCLATH					PC[11]	PC[10]	PC[9]	PC[8]	 0000	 0000	-,-,-,- *,*,*,*
1BH	PCLATL	PC Low Byte for PC<7:0>								0000 0000	0000 0000	*,*,*,*,*,*,*,*
1DH	TBLPTRH					TBLPTR[11]	TBLPTR[10]	TBLPTR[9]	TBLPTR[8]	 0000	 0000	-,-,-,- *,*,*,*
1EH	TBLPTRL	Program Memory Table Pointer Low Byte (TBLPTR<7:0>)								0000 0000	0000 0000	*,*,*,*,*,*,*,*
1FH	TBLDH	Program Memory Table Latch High Byte								0000 0000	0000 0000	*,*,*,*,*,*,*,*
20H	TBLDL	Program Memory Table Latch Low Byte								0000 0000	0000 0000	*,*,*,*,*,*,*,*
21H	PRODH	Product Register of Multiply High Byte								xxxx xxxx	uuuu uuuu	r,r,r,r r,r,r,r
22H	PRODL	Product Register of Multiply Low Byte								xxxx xxxx	uuuu uuuu	r,r,r,r r,r,r,r
23H	INTE1	GIE	ADCIE	TMCIE	TMBIE	TMAIE	WDTIE	E1IE	E0IE	0000 0000	0000 0000	*,*,*,*,*,*,*,*
24H	INTE2	TXIE	RCIE				SSPIE	CCP1IE	CCP0IE	.... .000	.... .000	-,-,-,- -,*,*,*
26H	INTF1		ADCIF	TMCIF	TMBIF	TMAIF	WDTIF	E1IF	E0IF	.000 0000	.000 0000	-,*,*,*,*,*,*,*
27H	INTF2						SSPIF	CCP1IF	CCP0IF	.... .000	.... .000	-,-,-,- -,*,*,*
29H	WREG	Working Register								xxxx xxxx	uuuu uuuu	*,*,*,*,*,*,*,*
2AH	BSRCN								BSR[0]	0	0	-,-,-,- -,-,-,*
2BH	STATUS				C	DC	N	OV	Z	...x xxxx	...u uuuu	-,-,-,*,*,*,*,*
2CH	PSTATUS	PD	TO	IDLEB	BOR		SKERR			000d .0..	uduu .d..	rw0,rw0,rw0,rw0 -,rw0,-,-
2DH	LVDCN		LVDFG	LVD	LVDON	VLDX[3:0]				.000 0000	.000 uuuu	-,*,r,r *,*,*,*
30H	PWRCN	ENVDDA	VDDAX[1:0]		ENACM					0000	0000	*,*,*,* -,-,-,-
31H	MCKCN1	ADCS[2:0]			ADCCK	XTHSP	XTSP	ENXT	ENHAO	0000 0001	0000 0001	*,*,*,*,*,*,*,*
32H	MCKCN2			LSCK	HSCK	HSS[1:0]		CPUCK[1:0]		..00 0000	..00 0000	-,-,*,*,*,*,*,*
33H	MCKCN3	LCDS[2:0]				PERCK	BZS[2:0]			000. 0000	000. 0000	*,*,*,-,*,*,*,*
37H	OPCN1	ENOP	OPM[1:0]		OPP[1:0]		OPN[2:0]			0000 0000	0000 0000	*,*,*,*,*,*,*,*
39H	ADCRH	ADC conversion memory HighByte								xxxx xxxx	uuuu uuuu	r,r,r,r r,r,r,r
3AH	ADCRM	ADC conversion memory Middle Byte								xxxx xxxx	uuuu uuuu	r,r,r,r r,r,r,r
3BH	ADCRL	ADC conversion memory Low Byte								xxxx xxxx	uuuu uuuu	r,r,r,r r,r,r,r
3CH	ADCCN1	ENADC	ENHIGN	ENCHP	PGAGN[1:0]		ADGN[2:0]			0000 0000	0000 0000	*,*,*,*,*,*,*,*
3DH	ADCCN2			INBUF	VRBUF	VREGN	DCSET[2:0]			..00 0000	..00 0000	-,-,*,*,*,*,*,*
3EH	ADCCN3	OSR[2:0]								000.	000.	*,*,*,- -,-,-,-
3FH	AINET1	INH[2:0]			INL[2:0]			INIS	OPIS	0000 0000	0000 0000	*,*,*,*,*,*,*,*
40H	AINET2		VRH[1:0]		INX[1:0]		VRL[1:0]			.000 000.	.000 000.	-,*,*,*,*,*,*,-
41H	TMACN	ENTMA	TMACK	TMAS[1:0]		ENWDT	WDTS[2:0]			0000 0000	0000 0000	*,*,*,* w1,*,*,*
42H	TMAR	TimerA data register								xxxx xxxx	uuuu uuuu	r,r,r,r r,r,r,r
43H	TMBCN	ENTMB	TMBCK	TMBS[1:0]		TMBSYC	TMBR2R			0000 00..	0000 00..	*,*,*,*,*,-,-
44H	TMBRH	TimerB High Byte data register								xxxx xxxx	uuuu uuuu	*,*,*,*,*,*,*,*
45H	TMBRL	TimerB Low Byte data register								xxxx xxxx	uuuu uuuu	*,*,*,*,*,*,*,*
46H	TMCCN	ENTMC	TMCCK[1:0]		TMCS1[2:0]			TMCS0[1:0]		0000 0000	0000 0000	*,*,*,*,*,*,*,*
47H	PRC	TimerC programmable register								1111 1111	1111 1111	*,*,*,*,*,*,*,*
48H	TMCR	TimerC register								0000 0000	0000 0000	r,r,r,r r,r,r,r
49H	CCPCN	CCP1M[3:0]				CCP0M[3:0]				0000 0000	0000 0000	*,*,*,*,*,*,*,*
4AH	CCP0RH	CCP0 High Byte data register								xxxx xxxx	uuuu uuuu	*,*,*,*,*,*,*,*
4BH	CCP0RL	CCP0 Low Byte data register								xxxx xxxx	uuuu uuuu	*,*,*,*,*,*,*,*
4CH	CCP1RH	CCP1 High Byte data register								xxxx xxxx	uuuu uuuu	*,*,*,*,*,*,*,*
4DH	CCP1RL	CCP1 Low Byte data register								xxxx xxxx	uuuu uuuu	*,*,*,*,*,*,*,*
4EH	PASC	PASF		PASCF[1:0]						0.00	0.00	*,-,*,* -,-,-,-
4FH	PWMCN	ENPWM	ENPFD	PWMRL[1:0]						0000	0000	*,*,*,* -,-,-,-
51H	PWMR	PWM MSB Byte register								xxxx xxxx	uuuu uuuu	*,*,*,*,*,*,*,*

表 5-1(a) HY11P13 暫存器列表

“-”no use,“*”read/write,“w”write,“r”read,“r0”only read 0,“r1”only read 1,“w0”only write 0,“w1”omly write 1												
“.”unimplemented bit,“x”unknown,“u”unchanged,“d”depends on condition												
Address	**File Name**	**Bit7**	**Bit6**	**Bit5**	**Bit4**	**Bit3**	**Bit2**	**Bit1**	**Bit0**	**A-RESET**	**i-RESET**	**R/W**
52H	LCDCN1	ENLCD	LCDPR	VLCDX[1:0]		LCDBF	LCDBI[1:0]			0000 000.	0000 000.	*,*,*,*,*,*,-
53H	LCDCN2	LCDBL	LCDMX[1:0]							000.	000.	*,*,*,- -,-,-,-
54H	LCD0	Segment SEG2@[3:0] and SEG3@[7:4] data register of LCD								xxxx xxxx	uuuu uuuu	*,*,*,*,*,*,*,*
55H	LCD1	Segment SEG4@[3:0] and SEG5@[7:4] data register of LCD								xxxx xxxx	uuuu uuuu	*,*,*,*,*,*,*,*
56H	LCD2	Segment SEG6@[3:0] and SEG7@[7:4] data register of LCD								xxxx xxxx	uuuu uuuu	*,*,*,*,*,*,*,*
57H	LCD3	Segment SEG8@[3:0] and SEG9@[7:4] data register of LCD								xxxx xxxx	uuuu uuuu	*,*,*,*,*,*,*,*
58H	LCD4	Segment SEG10@[3:0] and SEG11@[7:4] data register of LCD								xxxx xxxx	uuuu uuuu	*,*,*,*,*,*,*,*
59H	LCD5	Segment SEG12@[3:0] and SEG13@[7:4] data register of LCD								xxxx xxxx	uuuu uuuu	*,*,*,*,*,*,*,*
5AH	LCD6	Segment SEG14@[3:0] and SEG15@[7:4] data register of LCD								xxxx xxxx	uuuu uuuu	*,*,*,*,*,*,*,*
5BH	LCD7	Segment SEG16@[3:0] and SEG17@[7:4] data register of LCD								xxxx xxxx	uuuu uuuu	*,*,*,*,*,*,*,*
5CH	LCD8	Segment SEG18@[3:0] and SEG19@[7:4] data register of LCD								xxxx xxxx	uuuu uuuu	*,*,*,*,*,*,*,*
5DH	LCD9	Segment SEG20@[3:0] and SEG21@[7:4] data register of LCD								xxxx xxxx	uuuu uuuu	*,*,*,*,*,*,*,*
5EH	SSPCON1	SSPEN	CKP	CKE	SMP			SSPM<1:0>		0000 ..00	uuuu ..uu	*,*,*,*,-,-,*,*
60H	SSPSTA	SSPBUY	SSPOV						BF	00.. ...0	00.. ...0	r,r,-,-,-,-,-,r
61H	SSPBUF	SSP Receive Buffer/Transmit Register								xxxx xxxx	uuuu uuuu	*,*,*,*,*,*,*,*
6DH	PT1	PT1.7	PT1.6	PT1.5	PT1.4	PT1.3	PT1.2	PT1.1	PT1.0	xxxx xxxx	uuuu uuuu	*,*,*,* r,r,r,r
6EH	TRISC1	TC1.7	TC1.6	TC1.5	TC1.4					0000	0000	*,*,*,*,-,-,-,-
6FH	PT1DA						DA1.2			.... .0..	.... .0..	-,-,-,-,-,-,*,-
70H	PT1PU	PU1.7	PU1.6	PU1.5	PU1.4	PU1.3	PU1.2	PU1.1	PU1.0	0000 0000	0000 0000	*,*,*,*,*,*,*,*
71H	PT1M1					INTEG1[1:0]		INTEG0[1:0]		 0000	 0000	-,-,-,-,*,*,*,*
72H	PT1M2		PM1.7[0]		PM1.6[0]		PM1.5[0]			.0.0 .0..	.0.0 .0..	-,*,-,*,-,*,-,-
74H	PT2			PT2.5	PT2.4	PT2.3	PT2.2	PT2.1	PT2.0	..xx xxxx	..uu uuuu	-,-,*,*,*,*,*,*
75H	TRISC2			TC2.5	TC2.4	TC2.3	TC2.2	TC2.1	TC2.0	..00 0000	..00 0000	-,-,*,*,*,*,*,*
77H	PT2PU			PU2.5	PU2.4	PU2.3	PU2.2	PU2.1	PU2.0	..00 0000	..00 0000	-,-,*,*,*,*,*,*
78H	PT2M1			PM2.2[1]	PM2.2[0]					..00	..00	-,-,*,* -,-,-,-
79H	PT2M2	PWMTR[1]	PWMTR[0]			PM2.5[1]	PM2.5[0]	PM2.4[1]	PM2.4[0]	00.. 0000	00.. 0000	*,*,-,- *,*,*,*
80H ~ FFH	GPR0	General Purpose Register as 128Byte								xxxx xxxx	uuuu uuuu	*,*,*,*,*,*,*,*
100H~17FH	GPR1	General Purpose Register as 128Byte								xxxx xxxx	uuuu uuuu	*,*,*,*,*,*,*,*

表 5-1(b) HY11P13 暫存器列表(續)

6. 電氣特性

Absolute maximum ratings over operating free-air temperature (unless otherwise noted)

Voltage applied at V_{DD} to V_{SS} . . . . . −0.2 V to 4.0 V

Voltage applied to any pin . . . . . −0.2 V to V_{DD} + 0.3 V

Voltage applied to RST/VPP pin . . . . . −0.2 V to 6.9 V

Voltage applied to TST/PT1.3 pin . . . . . −0.2 V to V_{DD} + 1 V

Diode current at any device terminal . . . . . ±2 mA

Storage temperature, Tstg: (unprogrammed device) . . . . . −55℃ to 150℃

(programmed device) . . . . . −40℃ to 85℃

Total power dissipation. 0.5w

Maximum output current sink by any PORT1 to PORT3 I/O pin. 25mA

6.1. Recommended operating conditions

T_A = -40℃ ~ 85℃,unless otherwise noted

Sym.	Parameter		Test Conditions		Min.	Typ.	Max.	unit
V_{DD}	Supply Voltage		All digital peripherals and CPU		2.2		3.6	V
			Analog peripherals		2.4		3.6	
V_{SS}	Supply Voltage				0		0	
XT	External Oscillator Frequency	Watch crystal	V_{DD} = 2.2V, ENXT[0]=1	XTSP[0]=0, XTHSP[0]=0	32.768K			Hz
		Ceramic resonator		XTSP[0]=1, XTHSP[0]=0	450K		8M	
		Crystal		XTSP[0]=1, XTHSP[0]=0	1M		8M	

6.2. Internal RC Oscillator

T_A = 25℃,V_{DD} = 3.0V,unless otherwise noted

Sym.	Parameter	Test Conditions	Min.	Typ.	Max.	unit
HAO	High Speed Oscillator frequency	ENHAO[0]=1	1.8	2.0	2.2	MHz
LPO	Low Power Oscillator frequency	V_{DD} supply voltage be enable LPO	22	28	35	KHz

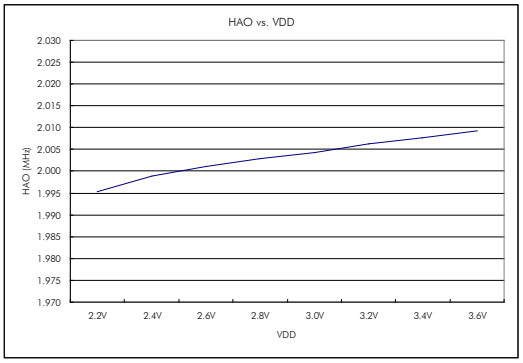


圖 6.2-1 HAO vs. VDD

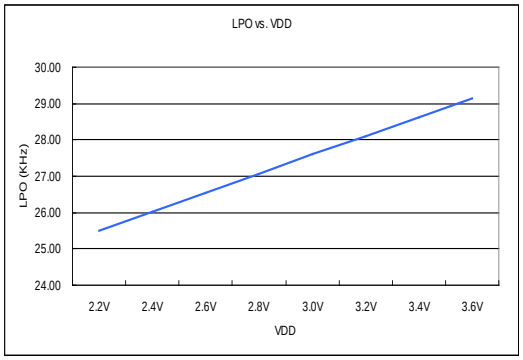


圖 6.2-2 LPO vs. VDD

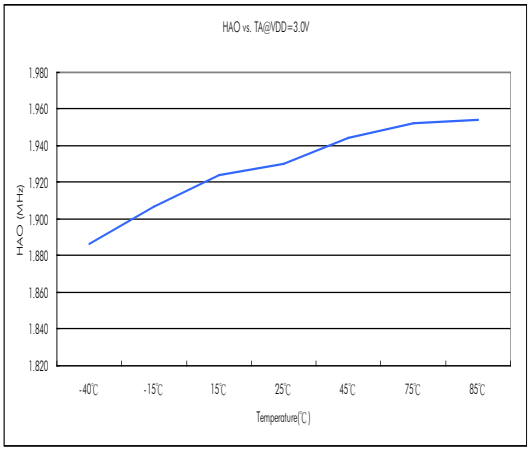


圖 6.2-3 HAO vs. Temperature

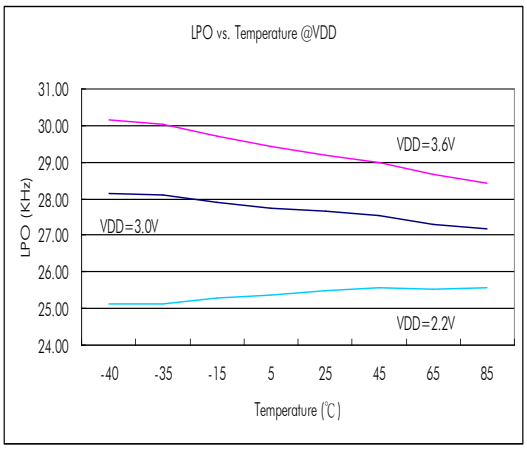


圖 6.2-4 LPO vs. Temperature

6.3. Supply current into VDD excluding peripherals current

T_A = 25℃,V_{DD} = 3.0V,OSC_LPO = 28KHz,unless otherwise noted

Sym.	Parameter	Test Conditions	Min.	Typ.	Max.	unit
I_{AM1}	Active mode 1	OSC_CY = 8MHz, OSC_HAO = off, CPU_CK = 8MHz		1.2	2	mA
I_{AM2}	Active mode 2	OSC_CY = off, OSC_HAO = 2MHz, CPU_CK = 2MHz		0.32	0.55	mA
I_{AM3}	Active mode 3	OSC_CY = off, OSC_HAO = 2MHz, CPU_CK = 1MHz		0.18	0.3	mA
I_{LP1}	Low Power 1	OSC_CY = 32768Hz, OSC_HAO = off, CPU_CK = 16384Hz		7	12	uA
I_{LP2}	Low Power 2	OSC_CY = off, OSC_HAO = off, CPU_CK = LPO, Idle state		1.65	3	uA
I_{LP3}	Low Power 3	OSC_CY = off, OSC_HAO = off, CPU_CK = off, Sleep state		0.65	1.2	uA

OSC_CY：External Oscillator frequency.

OSC_HAO：Internal High Accuracy Oscillator frequency.

CPU_CK：CPU core work frequency.

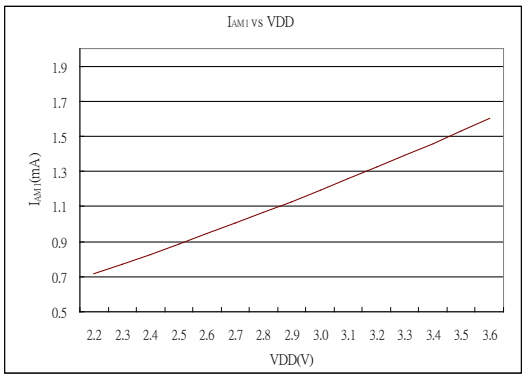


圖 6.3-1 I_{AM1} vs. VDD

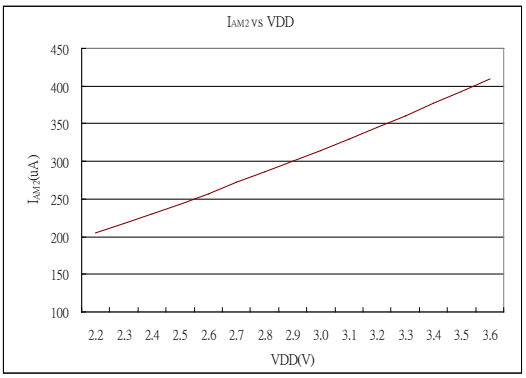


圖 6.3-2 I_{AM2} vs. VDD

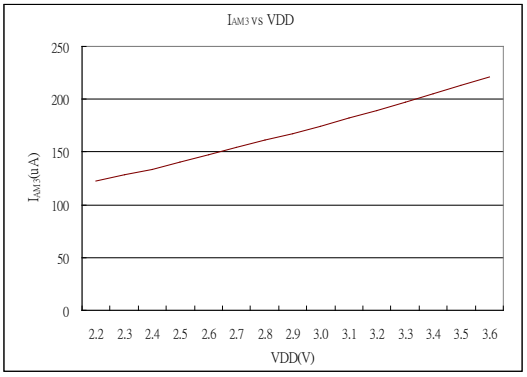


圖 6.3-3 I_{AM3} vs. VDD

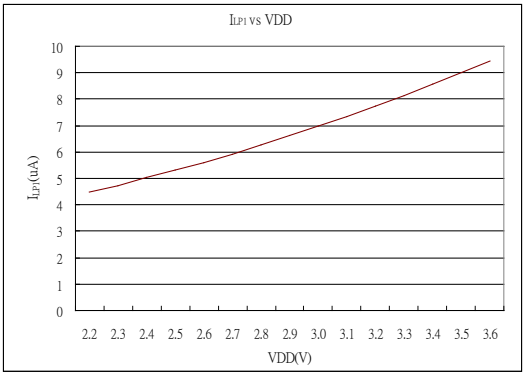


圖 6.3-4 I_{LP1} vs. VDD

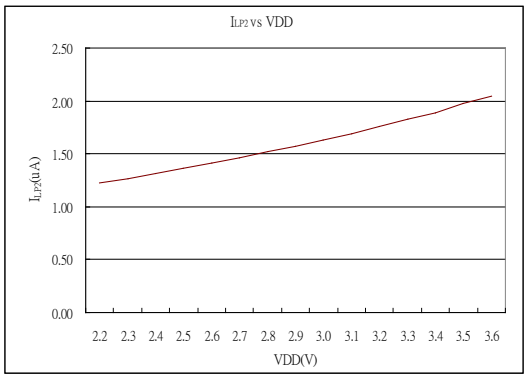


圖 6.3-5 I_{LP2} vs. VDD

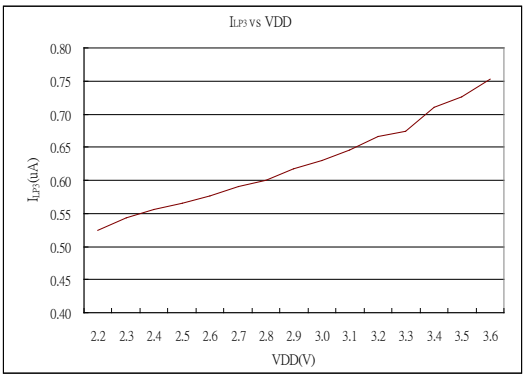


圖 6.3-6 I_{LP3} vs. VDD

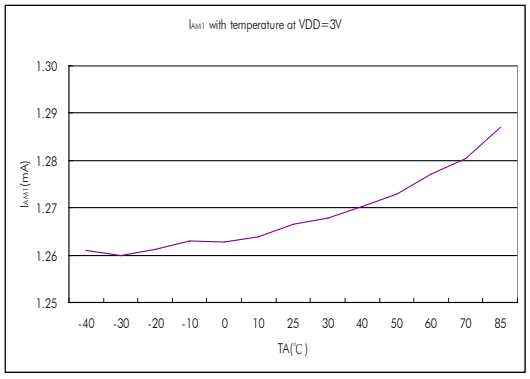


圖 6.3-7 I_{AM1} vs. Temperature

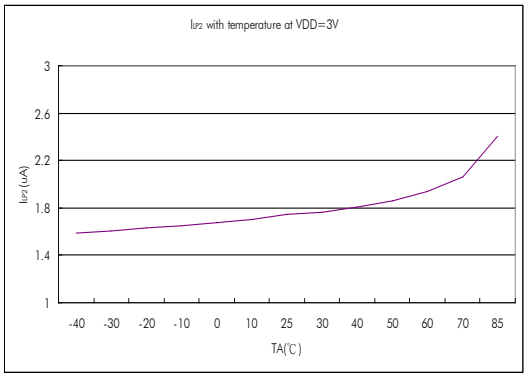


圖 6.3-8 I_{LP2} vs. Temperature

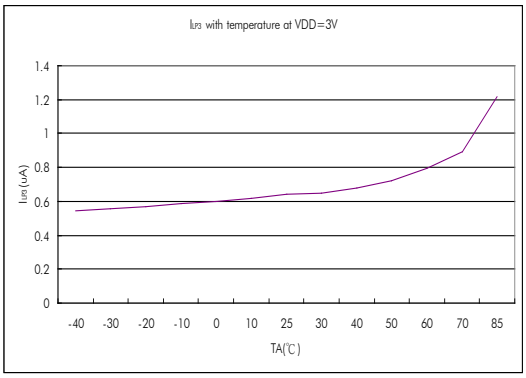


圖 6.3-9 I_{LP3} vs. Temperature

6.4. Port1~2

T_A = 25℃,V_{DD} = 3.0V,unless otherwise noted

Sym.	Parameter	Test Conditions	Min.	Typ.	Max.	unit
Input voltage and Schmitt trigger and leakage current and timing						
V_{IH}	High-Level input voltage				2.1	V
V_{IL}	Low-Level input voltage		0.9			
V_{hys}	Input Voltage hysteresis(VIH - VIL)			0.8		V
I_{LKG}	Leakage Current				0.1	uA
R_{PU}	Port pull high resistance			180		kΩ
Output voltage and current and frequency						
V_{OH}	High-level output voltage	I_{OH}=10mA	V_{DD} -0.3			V
V_{OL}	Low-level output voltage	I_{OL}=-10mA			VSS +0.3	

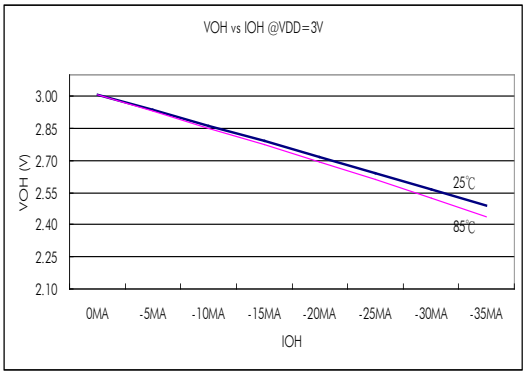


圖 6.4-1 V_{OH} vs. I_{OH} @VDD=3.0V

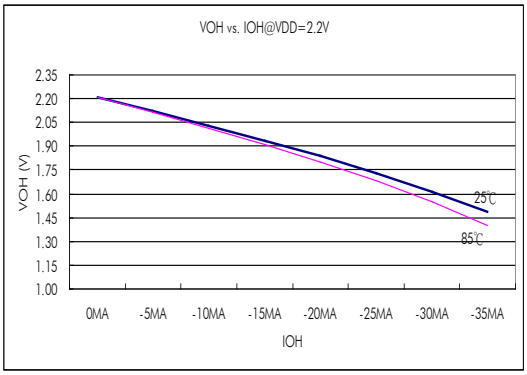


圖 6.4-2 V_{OH} vs. I_{OH} @VDD=2.2V

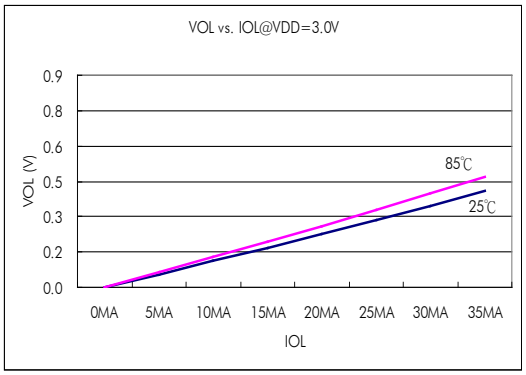


圖 6.4-3 V_{OL} vs. I_{OL}@VDD=3.0V

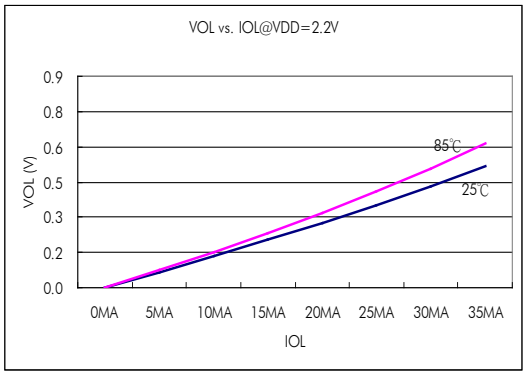


圖 6.4-4 V_{OL} vs. I_{OL}@VDD=2.2V

6.5. Reset(Brownout, External RST pin, Low Voltage Detect)

T_A = 25℃,V_{DD} = 3.0V,unless otherwise noted

Sym.	Parameter	Test Conditions	Min.	Typ.	Max.	unit
BOR	Pulse length needed to accepted reset internally, t_{d-LVR}		2			us
	V_{DD} Start Voltage to accepted reset internally (L➔H),V_{LVR}		1.6	1.85	2.1	V
	Hysteresis, $V_{HYS-LVR}$			70		mV
RST	Pulse length needed as RST/VPP pin to accepted reset internally, t_{d-RST}		2			us
	Input Voltage to accepted reset internally		0.9			V
	Hysteresis, $V_{HYS-RST}$			0.8		V
LVD	Operation current, I_{LVD}			10	15	uA
	External input voltage to compare reference voltage			1.2		V
	Compare reference voltage temperature drift	T_A = -40℃ ~ 85 ℃		100		ppm/℃
	Detect V_{DD} voltage rang by user option, V_{SVS} VLDx[3:0]=1110b			3.3		V
	Detect V_{DD} voltage rang by user option, V_{SVS} VLDx[3:0]=1101b			3.2		
	Detect V_{DD} voltage rang by user option, V_{SVS} VLDx[3:0]=1100b			3.1		
	Detect V_{DD} voltage rang by user option, V_{SVS} VLDx[3:0]=1011b			3.0		
	Detect V_{DD} voltage rang by user option, V_{SVS} VLDx[3:0]=1010b			2.9		
	Detect V_{DD} voltage rang by user option, V_{SVS} VLDx[3:0]=1001b			2.8		
	Detect V_{DD} voltage rang by user option, V_{SVS} VLDx[3:0]=1000b			2.7		
	Detect V_{DD} voltage rang by user option, V_{SVS} VLDx[3:0]=0111b			2.6		
	Detect V_{DD} voltage rang by user option, V_{SVS} VLDx[3:0]=0110b			2.5		
	Detect V_{DD} voltage rang by user option, V_{SVS} VLDx[3:0]=0101b			2.4		
	Detect V_{DD} voltage rang by user option, V_{SVS} VLDx[3:0]=0100b			2.3		
	Detect V_{DD} voltage rang by user option, V_{SVS} VLDx[3:0]=0011b			2.2		
	Detect V_{DD} voltage rang by user option, V_{SVS} VLDx[3:0]=0010b			2.1		
	Detect V_{DD} voltage rang by user option, V_{SVS} VLDx[3:0]=0001b			2.0		

BOR：Brownout Reset

LVR：Low Voltage Reset of BOR

LVD：Low Voltage Detect

RST：External Reset pin

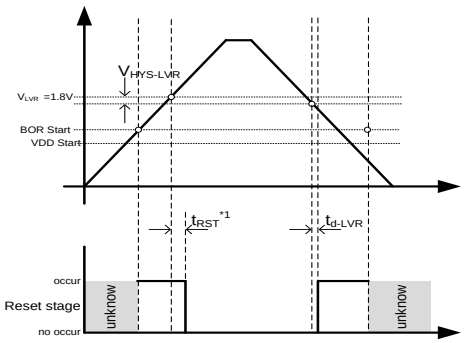


圖 6.5-1 BOR reset diagram

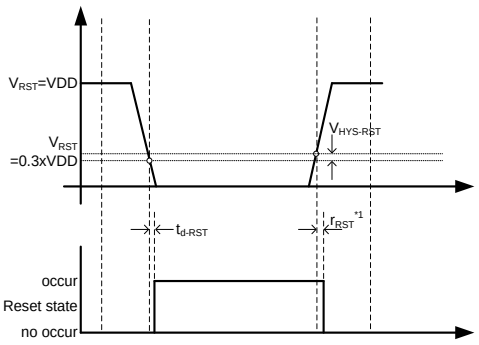


圖 6.5-2 RST reset diagram

*1 r_{RST}：Please see BOR Introduce of HY11Pxx series User's Guide (UG-HY11S14-Vxx).

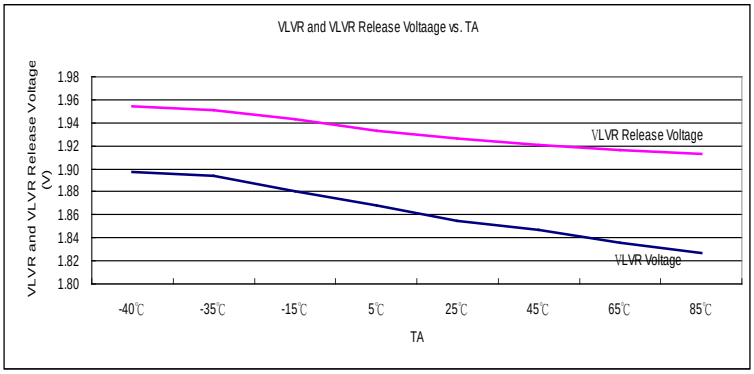


圖 6.5-3 LVR vs. Temperature

6.6. Power System

T_A = 25℃,V_{DD} = 3.0V,unless otherwise noted

Sym.	Parameter	Test Conditions		Min.	Typ.	Max.	unit
VDDA	VDDA operation current, I_{VDDA}	I_L = 0mA	VDDAX[1:0]=00b		22		uA
	Select VDDA output voltage	I_L = 0.1mA, VDD≧VDDA+0.2V	VDDAX[1:0]=00b		3.3		V
			VDDAX[1:0]=01b		2.9		V
			VDDAX[1:0]=10b		2.6		V
			VDDAX[1:0]=11b		2.4		V
	Dropout voltage	I_L = 10mA	VDDAX[1:0]=00b		135		mV
			VDDAX[1:0]=01b		150		mV
			VDDAX[1:0]=10b		165		mV
			VDDAX[1:0]=11b		180		mV
	Temperature drift	VDDAX[1:0]=11b	T_A=-40℃~85℃		50		ppm/℃
	V_{DD} Voltage drift	I_L = 0.1mA	V_{DD}=2.5V~3.6V		±0.2		%/V
ACM	ACM operation current, I_{ACM}	I_L = 0mA			20		uA
	Output voltage ,V_{ACM}	ENACM[0]=1	I_L = 0uA		1.0		V
	Output voltage with Load		I_L = ±200uA	0.98		1.02	V_{ACM}
	Temperature drift	ENACM[0]=1, I_L = 10uA	T_A=-40℃~85℃		50		ppm/℃
	VDDA Voltage drift				100		uV/V

VDDA：Adjust Voltage Regulator

ACM：Analog Common Mode Voltage

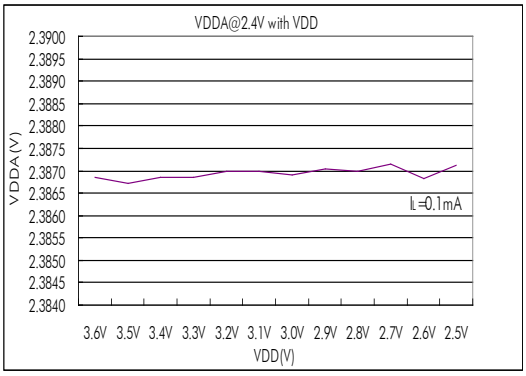


圖 6.6-1 VDDA I_L=0.1mA vs. VDD

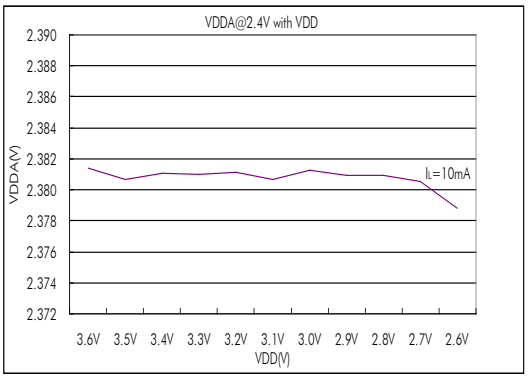


圖 6.6-2 VDDA IL=10mA vs. VDD

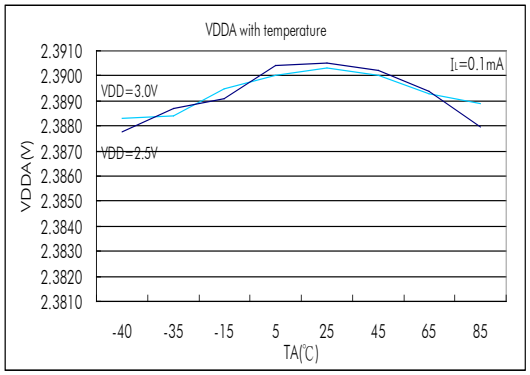


圖 6.6-3 VDDA I_L=0.1mA vs. Temperature

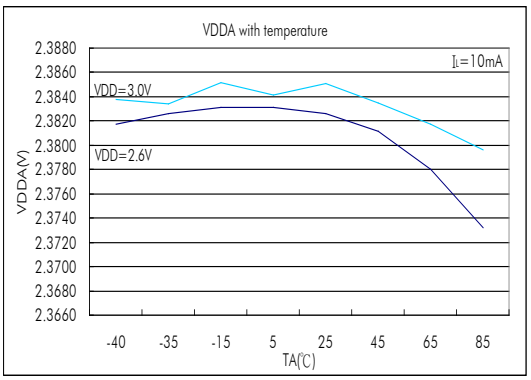


圖 6.6-4 VDDA I_L=10mA vs. Temperature

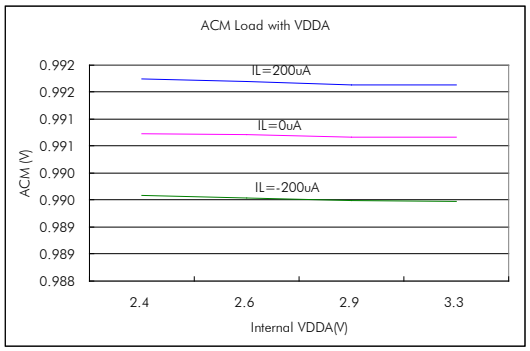


圖 6.6-5 ACM Load vs. VDDA

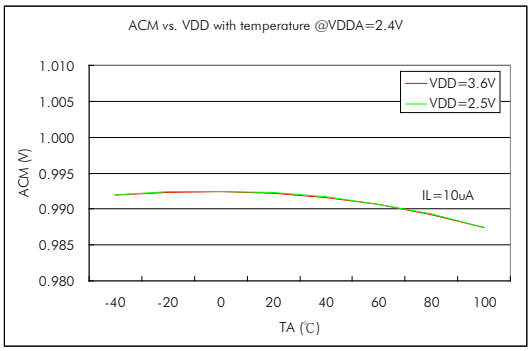


圖 6.6-6 ACM vs. Temperature

6.7. LCD

T_A = 25℃,V_{DD} = 3.0V, C_{VLCD} =4.7uF,unless otherwise noted.

Sym.	Parameter	Test Conditions		Min.	Typ.	Max.	unit
I_{LCD}	Operation supply current without output buffer.(all segment turn on)	LCDPR[0]=1	V_{DD} = 2.2V		10		uA
			V_{DD} = 3.0V				
VLCD	Supply Voltage at VLCD pin	LCDPR[0]=0		2.2		3.6	V
	Embedded Charge Pump output voltage at VLCD pin	V_{DD} = 2.2V, LCDPR[0]=1, C_{VLCD} =4.7uF	VLCDX[1:0]=11b	2.295	2.55	2.805	V
			VLCDX[1:0]=10b	2.52	2.8	3.08	
			VLCDX[1:0]=01b	2.745	3.05	3.355	
			VLCDX[1:0]=00b	2.97	3.3	3.63	
Z_{LCD}	Output impedance with LCD buffer	f_{LCD} =128Hz,VLCD=3.05V			10		kΩ

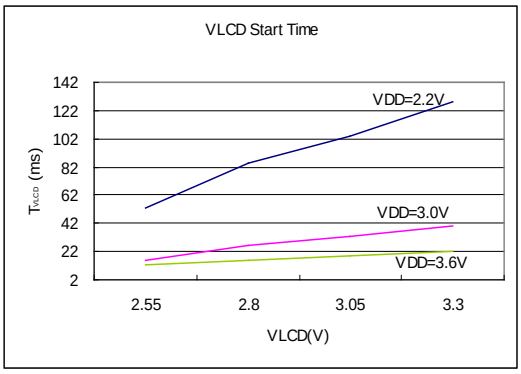


圖 6.7-1 LCD start time

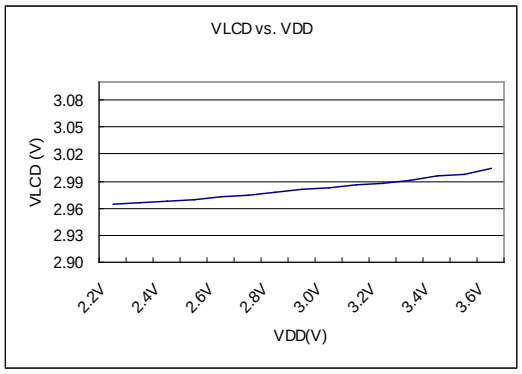


圖 6.7-2 VLCD vs. VDD

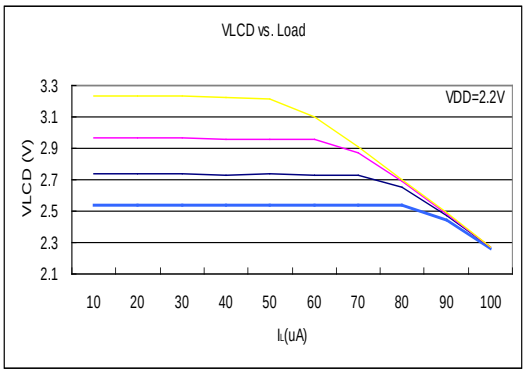


圖 6.7-3 VLCD vs. I_L @VDD=2.2V

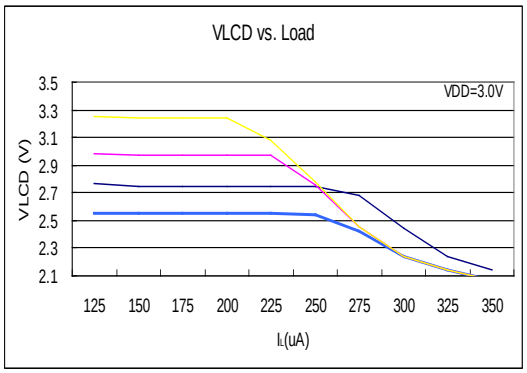


圖 6.7-4 VLCD vs. I_L @VDD=3.0V

6.8. Low Noise OPAMP

T_A = 25℃,V_{DD} = 3.0V, VDDA=2.4V,unless otherwise noted

Sym.	Parameter	Test Conditions		Min.	Typ.	Max.	unit
V_{LNOP}	Supply voltage at VDDA	ENVDDA[0]=0		2.4		3.6	V
I_{LNOP}	Operation supply current		OPM[1:0]=xxb		200		uA
V_{OS-OP}	Input offset voltage without chopper.		OPM[1:0]=1xb	-2		2	mV
	Input offset voltage with chopper		OPM[1:0]=0xb		20		uV
	Input offset voltage temperature drift.	OPM[1:0]=00b	T_A=-40℃~85℃		0.1		uV/℃
		OPM[1:0]=10			2		
V_{OLR}	Unit gain load regulation	V_O=1.2V, VDDA=2.4V	I_L=+1mA		0.1		%V_O
			I_L=-1mA				
CMVR	Common-mode voltage input range		OPM[1:0]=xxb	0.1		VDDA-1.1	V
CMRR	Common-mode rejection ratio		OPM[1:0]=xxb		90		dB

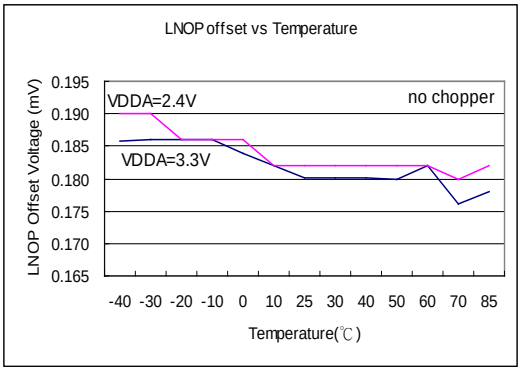


圖 6.8-1 LNOP Offset Temperature

6.9. SD18,Power Supply and recommended operating conditions

T_A = 25℃,V_{DD} = 3.0V, VDDA=2.4V,unless otherwise noted

Sym.	Parameter	Test Conditions		Min.	Typ.	Max.	unit
V_{SD18}	Supply Voltage at VDDA	ENVDDA[0]=0		2.4		3.6	V
f_{SD18}	Modulator sample frequency, ADC_CK			25	250	300	KHz
	Over Sample Ratio, OSR			256		32768	
I_{SD18}	Operation supply current without PGA	ENADC[0]=1 INBUF[0]=1,VRBUF[0]=0	GAIN =4, ADC_CK=250KHz		168		uA
		ENADC[0]=1 INBUF[0]=0,VRBUF[0]=1			150		
		ENADC[0]=1 INBUF[0]=0,VRBUF[0]=0			120		

6.9.1. PGA,Power Supply and recommended operating conditions

T_A = 25℃,V_{DD} = 3.0V, VDDA=2.4V,unless otherwise noted

Sym.	Parameter	Test Conditions		Min.	Typ.	Max.	unit
V_{PGA}	Supply Voltage at VDDA	ENVDDA[0]=0		2.4		3.6	V
I_{PGA}	Operation supply current	PGAGN[1:0]=<01>or<1x>			320		uA
G_{PGA}	Gain temperature drift	T_A = -40℃~ 85℃	GAIN=128		5		ppm/℃

6.9.2. SD18,performance Ⅱ（fSD18=250KHz）

T_A = 25℃,V_{DD} = 3.0V, VDDA=2.9V,V_{VR}=1.0V,GAIN=1 without PGA, unless otherwise noted

Sym.	Parameter	Test Conditions		Min.	Typ.	Max.	unit
INL	Integral Nonlinearity(INL)	VDDA=2.4V,V_{VR}=1.0V,ΔSI=±200mV			±0.003	±0.01	%FSR
		VDDA=2.4V,V_{VR}=1.0V,ΔSI=±450mV					
	No Missing Codes[3]	ADC_CK=250KHz,OSR[2:0]=010b		23			Bits
G_{SD18}	Temperature drift **Gain 1~x16 (INBUF[0]=0b,)** **Gain 1~x4 (INBUF[0]=1b,)**	INBUF[0]=0b,VRBUF[0]=0b	T_A = -40℃~ 85℃		2		ppm/℃
		INBUF[0]=1b,VRBUF[0]=0b					
		INBUF[0]=0b,VRBUF[0]=1b					
		INBUF[0]=1b,VRBUF[0]=1b					
E_{OS}	Offset error of Full Scale Rang input voltage range with Chopper and Buffer(INBUF,VRBUF) without PGA	ΔAI=0V ΔVR=0.9V DCSET[2:0]=<000> *ΔAI is external short	Gain=2			1	%FSR
	Offset error of Full Scale Rang input voltage range with Chopper without PGA and Buffer(INBUF,VRBUF)		Gain=2			1	
	Offset temperature drift with chopper without PGA and Buffer (INBUF,VRBUF).		GAIN=1		2		uV/℃
			GAIN=2		1		
			GAIN=4		0.5		
			GAIN=16		0.15		
	Offset temperature drift with chopper and Buffer (INBUF,VRBUF) without PGA.		GAIN=1		2		
			GAIN=2		1		
			GAIN=4		0.5		
	Offset temperature drift with chopper without Buffer (INBUF,VRBUF).		GAIN=128		0.02		
CM_{SD18}	Common-mode rejection	V_{CM}=0.7V to 1.7V, V_{VR}=1.0V,without PGA	V_{SI}=0V, GAIN=1		90		dB
		V_{CM}=0.7V to 1.7V, V_{VR}=1.0V, without PGA	V_{SI}=0V, GAIN=16		75		
PSRR	DC power supply rejection	VDDA=3.0V,ΔVDDA=±100mV,V_{VR}=1.0V, V_{SI}=1.2V,V_{SI-}=1.2V,	GAIN=1 PGA=off		75		dB
			GAIN=16 PGA=8				

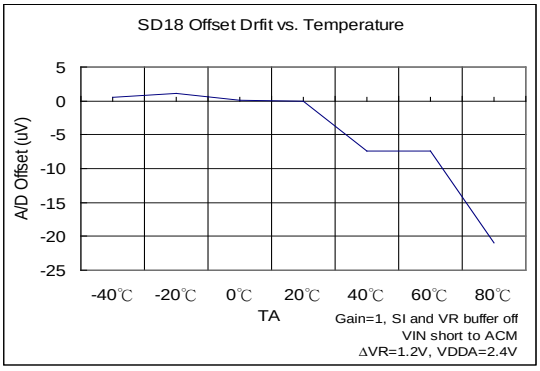


圖 6.9-1(a) SD18 Offset Temperature drift

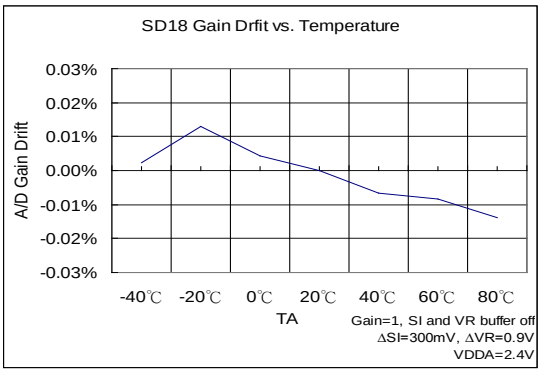


圖 6.9-2(a) SD18 Gain drift with temperature

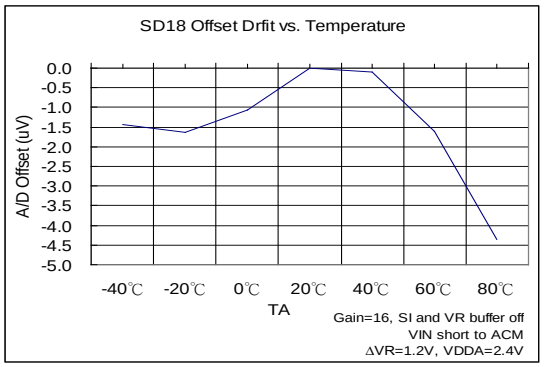


圖 6.9-1(b) SD18 Offset Temperature drift

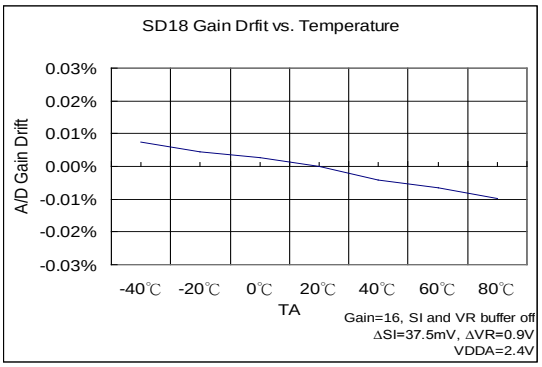


圖 6.9-2(b) SD18 Gain drift with temperature

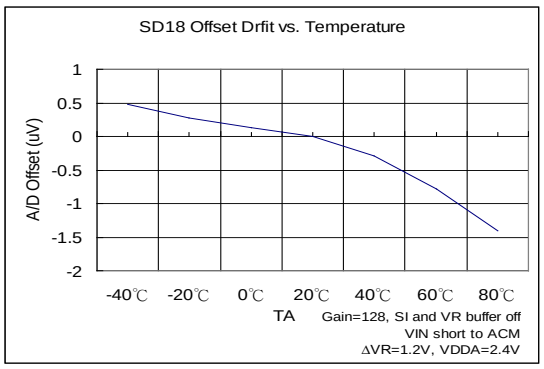


圖 6.9-1(c) SD18 Offset Temperature drift

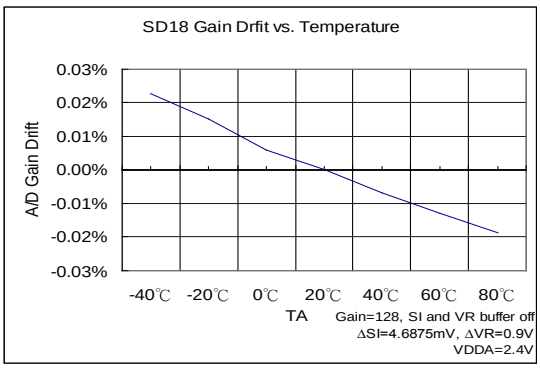


圖 6.9-2(c) SD18 Gain drift with temperature

6.9.3. SD18,Temperature sensor

T_A = 25℃,V_{DD} = 3.0V, VDDA=2.4V,unless otherwise noted

Sym.	Parameter	Test Conditions	Min.	Typ.	Max.	unit
TC_S	Sensor temperature drift	ΔVR=2.4V,VRGN[0]=1,		178		uV/℃
KT	Absolute Temperature Scale 0°K	INBUF[0]=1		-289		℃
TC_{ERR}	One point calibrate error temperature	Calibration at 25℃ of -40℃~ 85℃		±2		℃

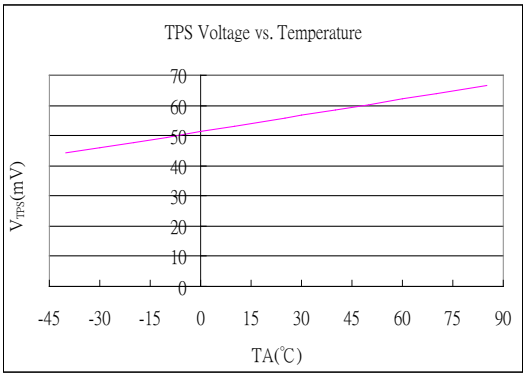


圖 6.9-3 TPS output voltage vs. temperature drift

6.9.4. SD18 Noise Performance

T_A = 25℃,V_{DD} = 3.0V, VDDA=2.4V,unless otherwise noted

HY11P13 針對 SD18 提供了重要的輸入雜訊規格。表 6.9-4(a), 表 6.9-4(b) 列出典型的雜訊規格表與 Gain, Output rate, 及單端最大輸入電壓等關係。測試條件設定在外部輸入訊號短路，參考電壓為 1.2V，取樣 1024 筆資料。

ENOB(RMS) with OSR/GAIN at A/D Clock=250Khz, VDDA=2.4V, VREF=1.2V													
Max. Vin(mV) =0.9*VREF (1)	**OSR**					**256**	**512**	**1024**	**2048**	**4096**	**8192**	**16384**	**32768**
	Output rate(HZ)					**977**	**488**	**244**	**122**	**61**	**31**	**15**	**8**
	Gain	**=**	**PGA**	**×**	**ADGN**								
±2400	**0.25**	**=**	**1**	**×**	**0.25**	16.3	17.4	17.9	18.5	19.0	19.5	20.0	20.4
±2160	**0.5**	**=**	**1**	**×**	**0.5**	16.3	17.3	17.9	18.4	18.9	19.4	19.8	20.2
±1080	**1**	**=**	**1**	**×**	**1**	16.2	17.2	17.8	18.3	18.8	19.3	19.7	20.1
±540	**2**	**=**	**1**	**×**	**2**	16.1	17.1	17.6	18.2	18.7	19.2	19.6	20.0
±270	**4**	**=**	**1**	**×**	**4**	16.0	16.9	17.5	18.0	18.5	18.9	19.4	19.8
±135	**8**	**=**	**1**	**×**	**8**	15.9	16.6	17.2	17.7	18.2	18.7	19.2	19.6
±68	**16**	**=**	**1**	**×**	**16**	15.6	16.3	16.8	17.3	17.7	18.3	18.8	19.3
±34	**32**	**=**	**2**	**×**	**16**	14.8	15.3	15.9	16.4	16.9	17.4	17.8	18.3
±17	**64**	**=**	**4**	**×**	**16**	14.5	15.0	15.5	16.0	16.5	17.0	17.5	18.0
±8	**128**	**=**	**8**	**×**	**16**	14.0	14.6	15.1	15.6	16.0	16.6	17.0	17.5

(1) Max.Vin (mV) is the max. input voltage of single end to ground (VSS).

表 6.9-4(a) SD18 ENOB Table

RMS Noise(uV) with OSR/GAIN at A/D Clock=250Khz, VDDA=2.4V, VREF=1.2V													
Max. Vin(mV) =0.9*VREF	**OSR**					**256**	**512**	**1024**	**2048**	**4096**	**8192**	**16384**	**32768**
	Output rate(HZ)					**977**	**488**	**244**	**122**	**61**	**31**	**15**	**8**
	Gain	**=**	**PGA**	**×**	**ADGN**								
±2400	**0.25**	**=**	**1**	**×**	**0.25**	121.08	57.40	38.74	26.66	18.39	13.21	9.49	6.98
±2160	**0.5**	**=**	**1**	**×**	**0.5**	61.63	29.23	19.21	13.51	9.78	7.02	5.12	3.91
±1080	**1**	**=**	**1**	**×**	**1**	32.21	15.70	10.25	7.31	5.19	3.77	2.80	2.13
±540	**2**	**=**	**1**	**×**	**2**	16.59	8.54	5.91	4.06	2.86	2.06	1.48	1.12
±270	**4**	**=**	**1**	**×**	**4**	9.00	4.84	3.33	2.37	1.67	1.19	0.87	0.65
±135	**8**	**=**	**1**	**×**	**8**	5.04	2.97	2.02	1.44	1.01	0.73	0.51	0.39
±68	**16**	**=**	**1**	**×**	**16**	3.03	1.84	1.29	0.92	0.70	0.46	0.33	0.24
±34	**32**	**=**	**2**	**×**	**16**	2.61	1.81	1.27	0.89	0.62	0.45	0.32	0.23
±17	**64**	**=**	**4**	**×**	**16**	1.66	1.13	0.80	0.56	0.41	0.29	0.20	0.14
±8	**128**	**=**	**8**	**×**	**16**	1.13	0.77	0.55	0.38	0.28	0.19	0.14	0.10

表 6.9-4(b) SD18 RMS Noise Table

The RMS noise are referred to the input. The Effective Number of Bits (ENOB(RMS Bit)) is defined as：

$$ENOB(RMS) = \ln\left(\frac{FSR}{RMS\ Noise}\right) \Big/ \ln(2)$$

$$RMS\ Noise = \left(2 \times VREF \times \sqrt{\sum_{k=1}^{1024}(ADO[k] - Average)^2}\right) \Big/ 2^{23}$$

$$Where\ FSR\ (Full-Scale\ Range) = 2 \times VREF/Gain.$$

$$Average = \frac{\sum_{k=1}^{1024}(ADO[k])}{1024}$$

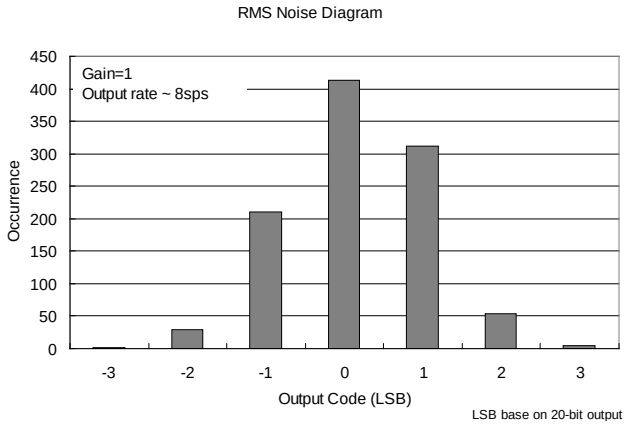


圖 6.9-4(a) RMS Noise Diagram

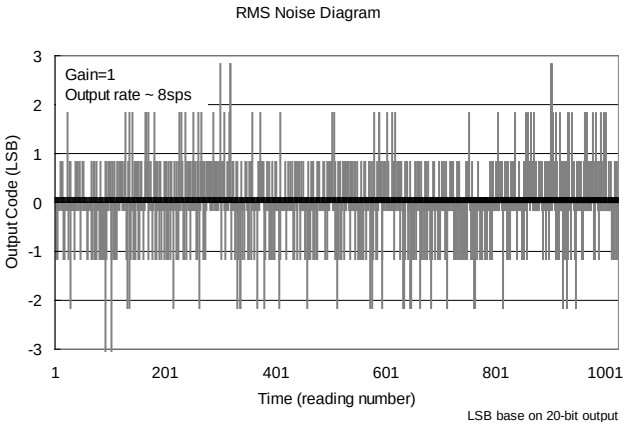


圖 6.9-4(b) Output Code Diagram

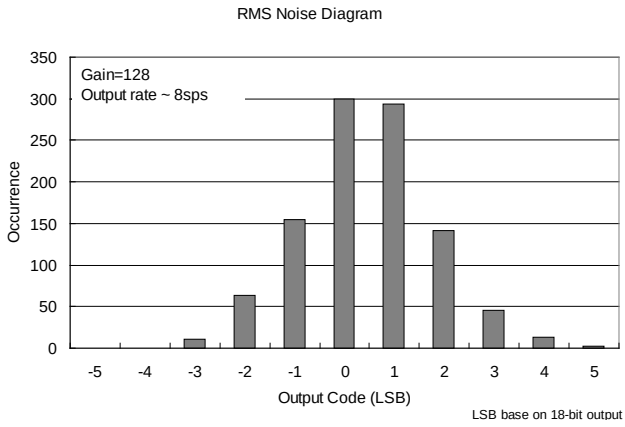


圖 6.9-4(c) RMS Noise Diagram

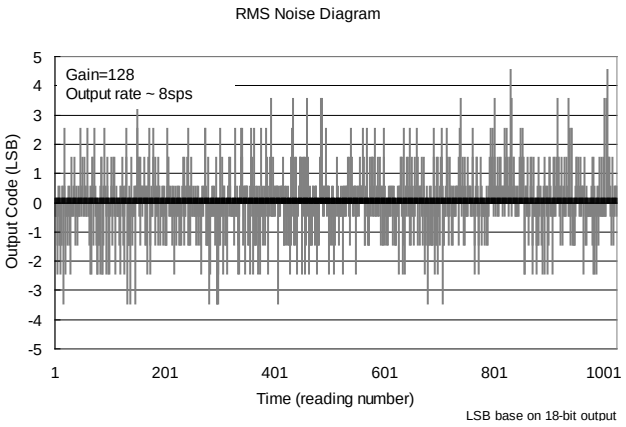


圖 6.9-4(d) Output Code Diagram

7. 訂貨資訊

下單品名[1]	封裝型式	引腳數	封裝型式描述方式		程式碼編號[2]	出貨包裝形式	個裝數量	材料組成	MSL[3]
HY11P13-D000	Die	-	D	000	000	-	100	Green[4]	-
HY11P13-L064	LQFP	64	L	064	000	Tray	160	Green[4]	MSL-3
HY11P13-LS64	LQFP	64	L	S64	000	Tray	250	Green[4]	MSL-3

[1] 產品名稱 – 封裝型式描述方式 – 程式碼編號（空白片 / 標準品 / 代客燒錄碼）

例如：您的代客燒錄服務申請的程式碼編號為 008，且需要的產品是裸片出貨。則下單品名為 HY11P13-D000-008

例如：您的需求是不帶程式碼的空白片且需要的產品是裸片出貨。則下單品名為 HY11P13-D000

例如：您的需求是不帶程式碼的空白片且需要的產品是封裝片LQFP64 (10x10)出貨，則下單品名為HY11P13-L064，且需以 Tray出貨，則除下單品名外，請特別註明出貨包裝形式為 Tray

例如：您的代客燒錄服務申請的程式碼編號為 009，而需求的產品是封裝片LQFP64 (7x7)出貨，則下單品名為HY11P13-LS64-009，且需以 Tray出貨，則除下單品名外，請特別註明出貨包裝形式為 Tray

[2] 程式碼編號

“001”~“999” 為標準品或代客燒錄申請的程式碼編號，而空白晶片不帶此碼。

[3] **MSL**

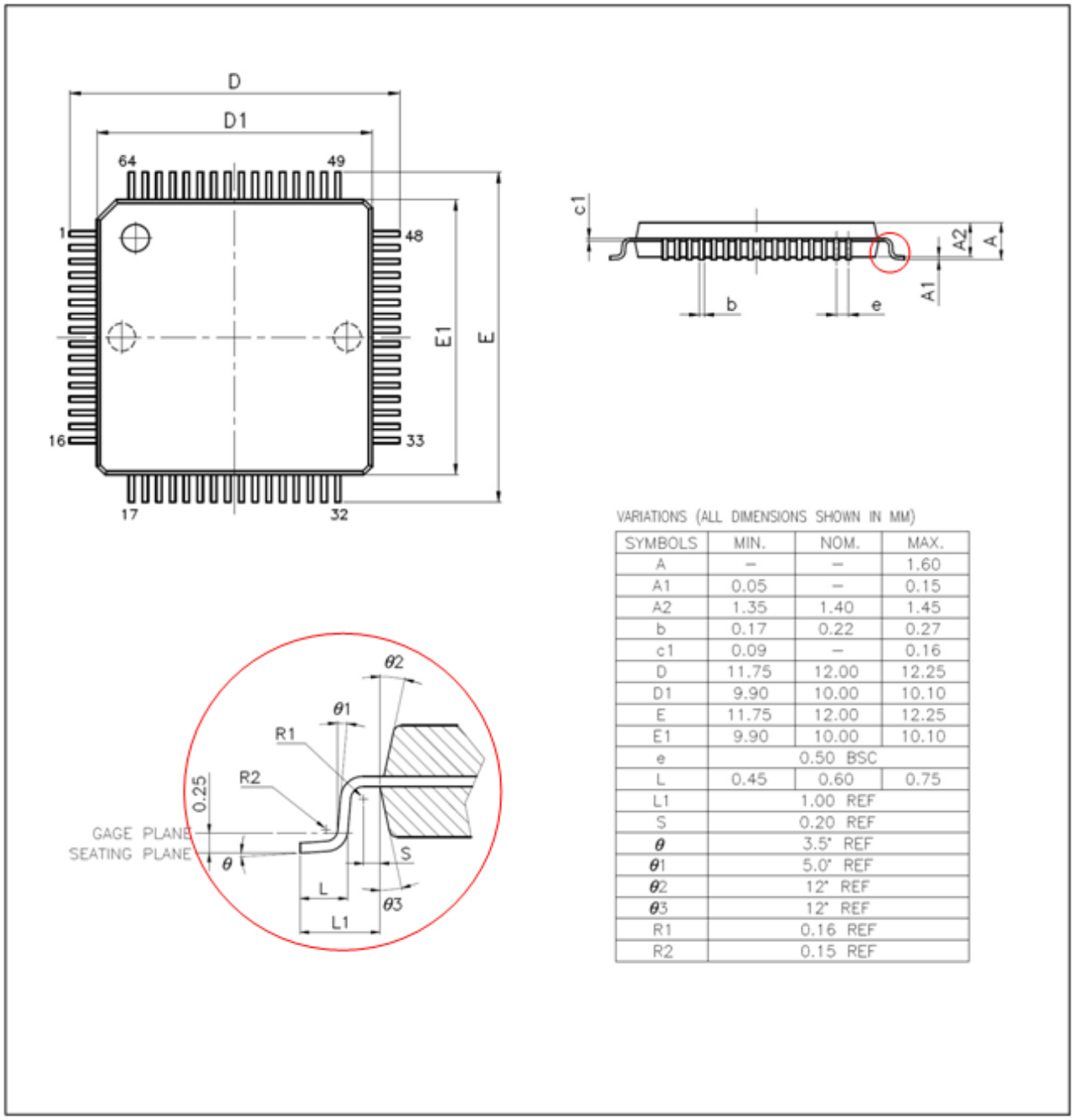
濕度敏感性等級係依據 IPC/JEDEC J-STD-020 的規範加以試驗分級，並參考 IPC/JEDEC J-STD-033 的標準處理、包裝、運輸與使用。

[4] **Green (RoHS & no Cl/Br)**

HYCON 產品皆為 Green Product，符合 RoHS 指令，REACH 高關注物質(SVHC)以及無鹵素相關規定。

8. 封裝型式資訊

8.1. LQFP64(L064)

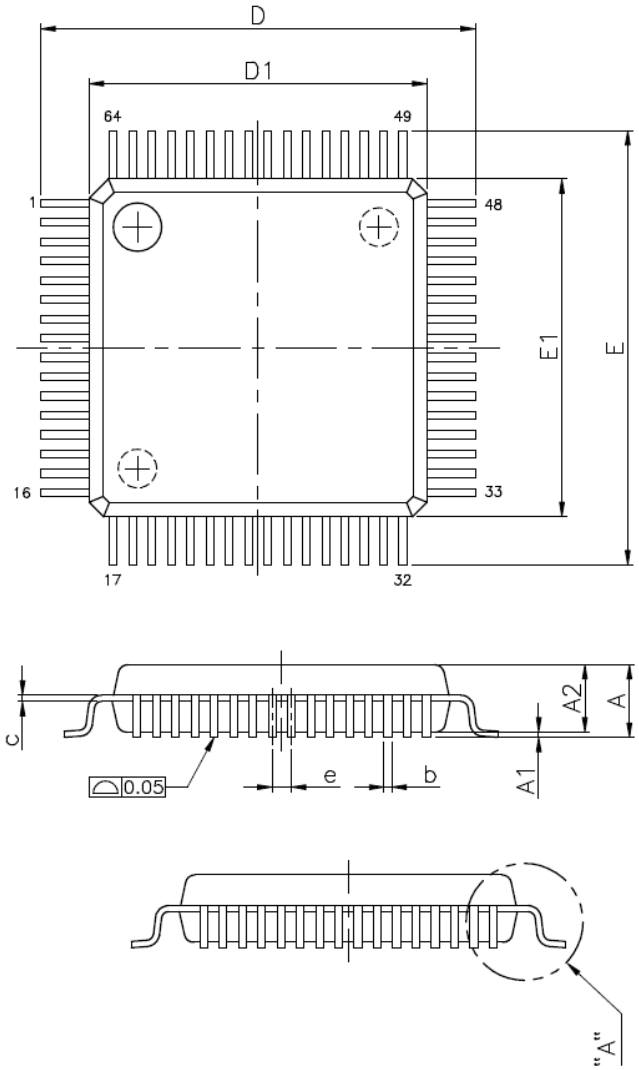


VARIATIONS (ALL DIMENSIONS SHOWN IN MM)

SYMBOLS	MIN.	NOM.	MAX.
A	–	–	1.60
A1	0.05	–	0.15
A2	1.35	1.40	1.45
b	0.17	0.22	0.27
c1	0.09	–	0.16
D	11.75	12.00	12.25
D1	9.90	10.00	10.10
E	11.75	12.00	12.25
E1	9.90	10.00	10.10
e	0.50 BSC		
L	0.45	0.60	0.75
L1	1.00 REF		
S	0.20 REF		
θ	3.5° REF		
θ1	5.0° REF		
θ2	12° REF		
θ3	12° REF		
R1	0.16 REF		
R2	0.15 REF		

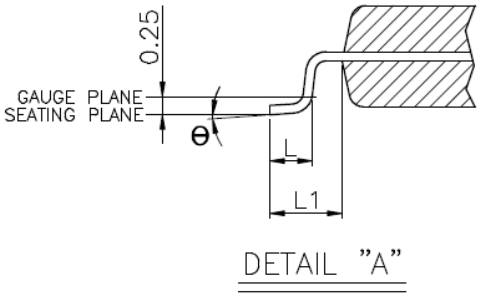
JEDEC MS-026 compliant

8.2. LQFP64(LS64)



VARIATIONS (ALL DIMENSIONS SHOWN IN MM)

SYMBOLS	MIN.	NOM.	MAX.
A	—	—	1.60
A1	0.05	—	0.15
A2	1.35	1.40	1.45
b	0.13	0.18	0.23
c	0.09	—	0.20
D	9.00 BSC		
D1	7.00 BSC		
e	0.40 BSC		
E	9.00 BSC		
E1	7.00 BSC		
L	0.45	0.60	0.75
L1	1.00 REF		
θ	0°	3.5°	7°



JEDEC MS-026 compliant

9. 修訂記錄

以下描述本檔差異較大的地方，而標點符號與字形的改變不在此描述範圍。

文件版次	頁次	摘要
V01	ALL	初版發行
V02	ALL	全面變更內容
V03	ALL	全面變更內容
V04	30	修訂 7 章節；轉為中文資訊且編修欄位與內容
	32	新增 8.2 章節；文件修訂記錄
V05	4	修訂 68 個指令成 67 個指令，特點內容修改
	6, 8	文字內容修改
	26	Input offset voltage temperature drift.規格修改
	27	增加G_{SD18}Temperature Drift內容說明
V06	6~7	修訂章節內容
	8~13	修訂電路圖內容
	24~25	修訂章節內容
	28~30	修訂章節內容
V07	15~16	修訂章節內容
V08	4	修訂特點內容
	9~11	修訂應用電路內容
	24~25	修訂章節內容
V09	1	修訂封面格式
	4	修訂特點內容，刪除 1/2bias 說明
	5	增加註 3 內容說明
	9~13	修訂應用電路圖，增加 RST 的 RC 電路
V10	15	增加 SD18 Network 章節
	25	修訂 Power System 溫飄規格
	32~33	增加 SD18 Noise Performance 章節
V11	4	修改 1.特點內容
	10	修改圖 3-2 內容
	11	修改圖 3-3 內容
	18	修改 6.電氣特性內容
	34	修改 RMS Noise Diagram
V12	4	修改格式
	15	修改圖 4-2 INH/INL
	27	降低 LCD 電流規格
	35	增加訂貨資訊

	37	增加封裝型式資訊
V13	14	修改開發工具相關使用說明書編號
	35	增加訂貨資訊內容
V14	16	增加 Low Noise OPAMP Network
V15	5	新增功能列表
	10	新增封裝型式與正印說明
	38	更新 Green (RoHS & no Cl/Br)